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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70q20b-cnt

7.8 Fast Startup

The SAM E70/S70/V70/V71 allows the processor to restart in a few microseconds while the processor is in Wait mode or in Sleep mode. A fast startup can occur upon detection of a low level on any of the following wakeup sources:

- WKUP0 to WKUP13 pins
- Supply Monitor
- RTC alarm
- RTT alarm
- USBHS interrupt line (WAKEUP)
- Processor debug request (CDBGPWRUPREQ)
- GMAC wake on LAN event

Note: CAN wakeup requires the use of any WKUP0–13 pin.

The fast restart circuitry is fully asynchronous and provides a fast startup signal to the Power Management Controller. As soon as the fast startup signal is asserted, the PMC automatically restarts the Main RC oscillator, switches the Master clock on this clock and re-enables the processor clock.

Offset	Name	Bit Pos.								
		31:24								
0x2C	MATRIX_MCFG11	7:0						ULBT[2:0]		
		15:8								
		23:16								
		31:24								
0x30	MATRIX_MCFG12	7:0						ULBT[2:0]		
		15:8								
		23:16								
		31:24								
0x34 ... 0x3F	Reserved									
0x40	MATRIX_SCFG0	7:0	SLOT_CYCLE[6:0]							
		15:8							SLOT_CYCLE[8:7]	
		23:16			FIXED_DEFMSTR[3:0]				DEFMSTR_TYPE[1:0]	
		31:24								
0x44	MATRIX_SCFG1	7:0	SLOT_CYCLE[6:0]							
		15:8							SLOT_CYCLE[8:7]	
		23:16			FIXED_DEFMSTR[3:0]				DEFMSTR_TYPE[1:0]	
		31:24								
0x48	MATRIX_SCFG2	7:0	SLOT_CYCLE[6:0]							
		15:8							SLOT_CYCLE[8:7]	
		23:16			FIXED_DEFMSTR[3:0]				DEFMSTR_TYPE[1:0]	
		31:24								
0x4C	MATRIX_SCFG3	7:0	SLOT_CYCLE[6:0]							
		15:8							SLOT_CYCLE[8:7]	
		23:16			FIXED_DEFMSTR[3:0]				DEFMSTR_TYPE[1:0]	
		31:24								
0x50	MATRIX_SCFG4	7:0	SLOT_CYCLE[6:0]							
		15:8							SLOT_CYCLE[8:7]	
		23:16			FIXED_DEFMSTR[3:0]				DEFMSTR_TYPE[1:0]	
		31:24								
0x54	MATRIX_SCFG5	7:0	SLOT_CYCLE[6:0]							
		15:8							SLOT_CYCLE[8:7]	
		23:16			FIXED_DEFMSTR[3:0]				DEFMSTR_TYPE[1:0]	
		31:24								
0x58	MATRIX_SCFG6	7:0	SLOT_CYCLE[6:0]							
		15:8							SLOT_CYCLE[8:7]	
		23:16			FIXED_DEFMSTR[3:0]				DEFMSTR_TYPE[1:0]	
		31:24								
0x5C	MATRIX_SCFG7	7:0	SLOT_CYCLE[6:0]							
		15:8							SLOT_CYCLE[8:7]	
		23:16			FIXED_DEFMSTR[3:0]				DEFMSTR_TYPE[1:0]	
		31:24								
0x60	MATRIX_SCFG8	7:0	SLOT_CYCLE[6:0]							
		15:8							SLOT_CYCLE[8:7]	

29. General Purpose Backup Registers (GPBR)

29.1 Description

The System Controller embeds 128 bits of General Purpose Backup registers organized as 8 32-bit registers.

It is possible to generate an immediate clear of the content of General Purpose Backup registers 0 to 3 (first half) if a Low-power Debounce event is detected on one of the wakeup pins, WKUP0 or WKUP1. The content of the other General Purpose Backup registers (second half) remains unchanged.

The Supply Controller module must be programmed accordingly. In the register SUPC_WUMR in the Supply Controller module, LPDBCCLR, LPDBCEN0 and/or LPDBCEN1 bit must be configured to 1 and LPDBC must be other than 0.

If a Tamper event has been detected, it is not possible to write to the General Purpose Backup registers while the LPDBCS0 or LPDBCS1 flags are not cleared in the Supply Controller Status Register (SUPC_SR).

29.2 Embedded Characteristics

- 128 bits of General Purpose Backup Registers
- Immediate Clear on Tamper Event

Parameter	Reset Value	Definition
WRITE_MODE	1	Write is controlled with NWE.
READ_MODE	1	Read is controlled with NRD.

35.9.8 Usage Restriction

The SMC does not check the validity of the user-programmed parameters. If the sum of SETUP and PULSE parameters is larger than the corresponding CYCLE parameter, this leads to unpredictable behavior of the SMC.

- For read operations:
  Null but positive setup and hold of address and NRD and/or NCS can not be guaranteed at the memory interface because of the propagation delay of theses signals through external logic and pads. If positive setup and hold values must be verified, then it is strictly recommended to program non-null values so as to cover possible skews between address, NCS and NRD signals.
- For write operations:
  If a null hold value is programmed on NWE, the SMC can guarantee a positive hold of address and NCS signal after the rising edge of NWE. This is true for SMC_MODE.WRITE_MODE = 1 only. See ”Early Read Wait State”.
- For read and write operations:
  A null value for pulse parameters is forbidden and may lead to unpredictable behavior.

  In read and write cycles, the setup and hold time parameters are defined in reference to the address bus. For external devices that require setup and hold time between NCS and NRD signals (read), or between NCS and NWE signals (write), these setup and hold times must be converted into setup and hold times in reference to the address bus.

35.10 Scrambling/Unscrambling Function

The external data bus can be scrambled to prevent recovery of intellectual property data located in off-chip memories by means of data analysis at the package pin level of either the microcontroller or the memory device.

The scrambling and unscrambling are performed on-the-fly without additional wait states.

The scrambling/unscrambling function can be enabled or disabled by configuring the CSxSE bits in the SMC Off-Chip Memory Scrambling Register (SMC_OCMS).

When multiple chip selects are handled, the scrambling function per chip select is configurable using the CSxSE bits in the SMC_OCMS register.

The scrambling method depends on two user-configurable key registers, SMC_KEY1 and SMC_KEY2 plus a random value depending on device processing characteristics. These key registers cannot be read. They can be written once after a system reset.

The scrambling user key or the seed for key generation must be securely stored in a reliable non-volatile memory in order to recover data from the off-chip memory. Any data scrambled with a given key cannot be recovered if the key is lost.

37.6.12 ISI Interrupt Enable Register

Name: ISI_IER
Offset: 0x2C
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
					FR_OVR	CRC_ERR	C_OVR	P_OVR
Access					W	W	W	W
Reset					–	–	–	–

Bit	23	22	21	20	19	18	17	16
							CXFR_DONE	PXFR_DONE
Access							W	W
Reset							–	–

Bit	15	14	13	12	11	10	9	8
						VSYNC		
Access						W		
Reset						–		

Bit	7	6	5	4	3	2	1	0
						SRST	DIS_DONE	
Access						W	W	
Reset						–	–	

Bit 27 – FR_OVR Frame Rate Overflow Interrupt Enable

Value	Description
0	No effect.
1	Enables the corresponding interrupt.

Bit 26 – CRC_ERR Embedded Synchronization CRC Error Interrupt Enable

Value	Description
0	No effect.
1	Enables the corresponding interrupt.

Bit 25 – C_OVR Codec Datapath Overflow Interrupt Enable

Value	Description
0	No effect.
1	Enables the corresponding interrupt.

Bit 24 – P_OVR Preview Datapath Overflow Interrupt Enable

Value	Description
0	No effect.
1	Enables the corresponding interrupt.

37.6.23 DMA Codec Descriptor Address Register

Name: ISI_DMA_C_DSCR
Offset: 0x58
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	C_DSCR[29:22]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	C_DSCR[21:14]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	C_DSCR[13:6]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	C_DSCR[5:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bits 31:2 – C_DSCR[29:0] Codec Descriptor Base Address
This address is word-aligned.

38.8.79 GMAC Receive Overruns Register

Name: GMAC_ROE
Offset: 0x1A4
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							RXOVR[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	RXOVR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – RXOVR[9:0] Receive Overruns
This bit field counts the number of frames that are address recognized but were not copied to memory due to a receive overrun.

39.6.38 Host Frame Number Register

Name: USBHS_HSTFNUM
Offset: 0x0420
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	FLENHIGH[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
			FNUM[10:5]					
Access								
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FNUM[4:0]					MFNUM[2:0]		
Access								
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – FLENHIGH[7:0] Frame Length
In High-speed mode, this field contains the 8 high-order bits of the 16-bit internal frame counter (at 30 MHz, the counter length is 3750 to ensure a SOF generation every 125 µs).

Bits 13:3 – FNUM[10:0] Frame Number
This field contains the current SOF number.

This field can be written. In this case, the MFNUM field is reset to zero.

Bits 2:0 – MFNUM[2:0] Micro Frame Number
This field contains the current microframe number (can vary from 0 to 7), updated every 125 µs.

When operating in Full-speed mode, this field is tied to zero.

Bit 1 – SPIDIS SPI Disable
All pins are set in Input mode after completion of the transmission in progress, if any.

If a transfer is in progress when SPIDIS is set, the SPI completes the transmission of the shifter register and does not start any new transfer, even if SPI_THR is loaded.

If both SPIEN and SPIDIS are equal to one when SPI_CR is written, the SPI is disabled.

Value	Description
0	No effect.
1	Disables the SPI.

Bit 0 – SPIEN SPI Enable

Value	Description
0	No effect.
1	Enables the SPI to transfer and receive data.

Detection on TF/RF input/output is done by the field FSOS of the Transmit/Receive Frame Mode Register (SSC_TFMR/SSC_RFMR).

Figure 44-13. Transmit Start Mode

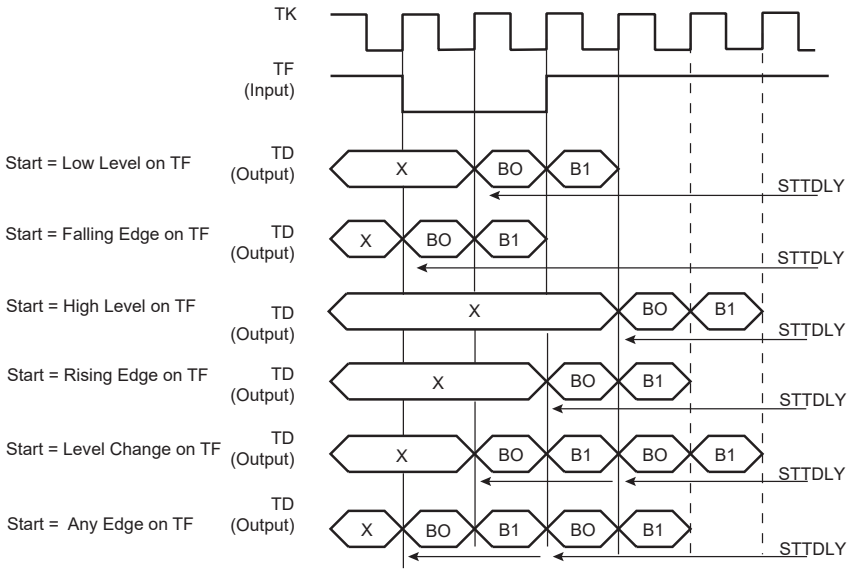
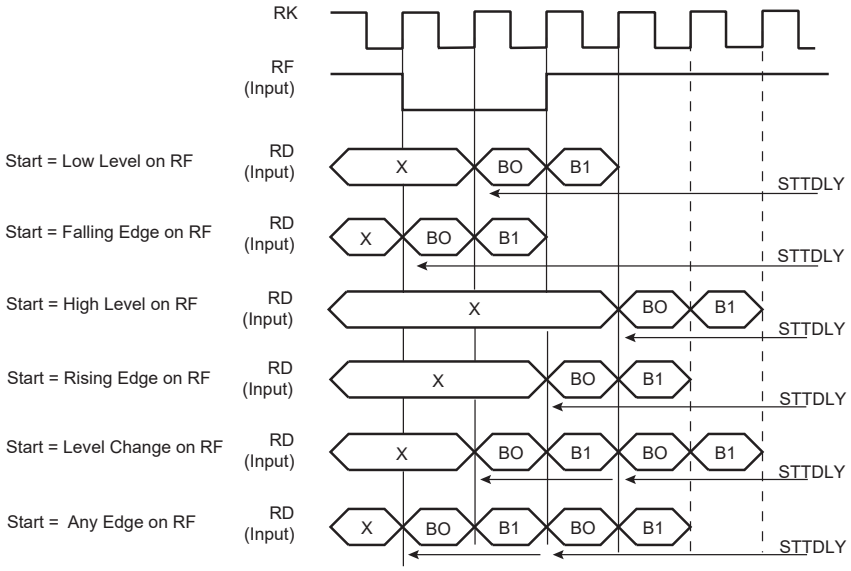


Figure 44-14. Receive Pulse/Edge Start Modes



44.8.5 Frame Synchronization

The Transmit and Receive Frame Sync pins, TF and RF, can be programmed to generate different kinds of Frame Sync signals. The Frame Sync Output Selection (FSOS) field in the Receive Frame Mode Register (SSC_RFMR) and in the Transmit Frame Mode Register (SSC_TFMR) are used to select the required waveform.

- Programmable low or high levels during data transfer are supported.
- Programmable high levels before the start of data transfers or toggling are also supported.

If a pulse waveform is selected, the Frame Sync Length (FSLEN) field in SSC_RFMR and SSC_TFMR programs the length of the pulse, from 1 bit time up to 256 bit times.

The periodicity of the Receive and Transmit Frame Sync pulse output can be programmed through the Period Divider Selection (PERIOD) field in SSC_RCMR and SSC_TCMR.

44.8.5.1 Frame Sync Data

Frame Sync Data transmits or receives a specific tag during the Frame Sync signal.

During the Frame Sync signal, the receiver can sample the RD line and store the data in the Receive Sync Holding Register and the transmitter can transfer Transmit Sync Holding Register in the shift register. The data length to be sampled/shifted out during the Frame Sync signal is programmed by the FSLEN field in SSC_RFMR/SSC_TFMR and has a maximum value of 256.

Concerning the Receive Frame Sync Data operation, if the Frame Sync Length is equal to or lower than the delay between the start event and the current data reception, the data sampling operation is performed in the Receive Sync Holding Register through the receive shift register.

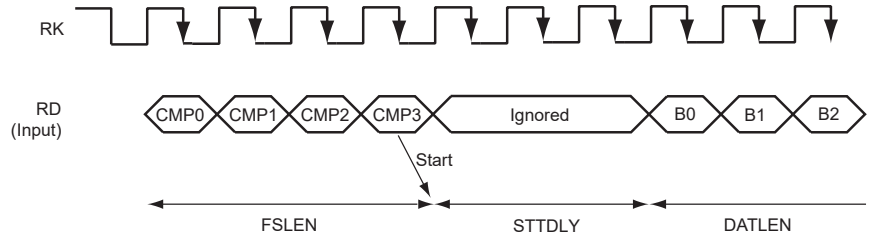
The Transmit Frame Sync Operation is performed by the transmitter only if the bit Frame Sync Data Enable (FSDEN) in SSC_TFMR is set. If the Frame Sync length is equal to or lower than the delay between the start event and the current data transmission, the normal transmission has priority and the data contained in the Transmit Sync Holding Register is transferred in the Transmit Register, then shifted out.

44.8.5.2 Frame Sync Edge Detection

The Frame Sync Edge detection is programmed by the FSEDGE field in SSC_RFMR/SSC_TFMR. This sets the corresponding flags RXSYN/TXSYN in the SSC Status Register (SSC_SR) on Frame Sync Edge detection (signals RF/TF).

44.8.6 Receive Compare Modes

Figure 44-15. Receive Compare Modes



44.8.6.1 Compare Functions

The length of the comparison patterns (Compare 0, Compare 1) and thus the number of bits they are compared to is defined by FSLEN, but with a maximum value of 256 bits. Comparison is always done by comparing the last bits received with the comparison pattern. Compare 0 can be one start event of the receiver. In this case, the receiver compares at each new sample the last bits received at the Compare 0 pattern contained in the Compare 0 Register (SSC_RC0R). When this start event is selected, the user can program the receiver to start a new data transfer either by writing a new Compare 0, or by receiving continuously until Compare 1 occurs. This selection is done with the STOP bit in the SSC_RCMR.

44.8.7 Data Format

The data framing format of both the transmitter and the receiver are programmable through the Transmitter Frame Mode Register (SSC_TFMR) and the Receive Frame Mode Register (SSC_RFMR). In either case, the user can independently select the following parameters:

- Event that starts the data transfer (START)
- Delay in number of bit periods between the start event and the first data bit (STTDLY)

Value	Description
0	Logic zero is coded as a zero-to-one transition, Logic one is coded as a one-to-zero transition.
1	Logic zero is coded as a one-to-zero transition, Logic one is coded as a zero-to-one transition.

Bits 25:24 – RX_PP[1:0] Receiver Preamble Pattern detected
The following values assume that RX_MPOL field is not set:

Value	Name	Description
00	ALL_ONE	The preamble is composed of ‘1’s
01	ALL_ZERO	The preamble is composed of ‘0’s
10	ZERO_ONE	The preamble is composed of ‘01’s
11	ONE_ZERO	The preamble is composed of ‘10’s

Bits 19:16 – RX_PL[3:0] Receiver Preamble Length

Value	Description
0	The receiver preamble pattern detection is disabled
1–15	The detected preamble length is RX_PL × Bit Period

Bit 12 – TX_MPOL Transmitter Manchester Polarity

Value	Description
0	Logic zero is coded as a zero-to-one transition, Logic one is coded as a one-to-zero transition.
1	Logic zero is coded as a one-to-zero transition, Logic one is coded as a zero-to-one transition.

Bits 9:8 – TX_PP[1:0] Transmitter Preamble Pattern
The following values assume that TX_MPOL field is not set:

Value	Name	Description
0	ALL_ONE	The preamble is composed of ‘1’s
1	ALL_ZERO	The preamble is composed of ‘0’s
2	ZERO_ONE	The preamble is composed of ‘01’s
3	ONE_ZERO	The preamble is composed of ‘10’s

Bits 3:0 – TX_PL[3:0] Transmitter Preamble Length

Value	Description
0	The transmitter preamble pattern generation is disabled
1–15	The preamble length is TX_PL × Bit Period

49.6.33 MCAN Receive FIFO 1 Acknowledge

Name: MCAN_RXF1A
Offset: 0xB8
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			F1AI[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – F1AI[5:0] Receive FIFO 1 Acknowledge Index
After the processor has read a message or a sequence of messages from Receive FIFO 1 it has to write the buffer index of the last element read from Receive FIFO 1 to F1AI. This will set the Receive FIFO 1 Get Index MCAN_RXF1S.F1GI to F1AI + 1 and update the FIFO 1 Fill Level MCAN_RXF1S.F1FL.

49.6.39 MCAN Transmit Buffer Add Request

Name: MCAN_TXBAR
Offset: 0xD0
Reset: 0x00000000
Property: Read/Write

If an add request is applied for a Transmit Buffer with pending transmission request (corresponding MCAN_TXBRP bit already set), this Add Request is ignored.

Bit	31	30	29	28	27	26	25	24
	AR31	AR30	AR29	AR28	AR27	AR26	AR25	AR24
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	AR23	AR22	AR21	AR20	AR19	AR18	AR17	AR16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	AR15	AR14	AR13	AR12	AR11	AR10	AR9	AR8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – ARx Add Request for Transmit Buffer x
Each Transmit Buffer has its own Add Request bit. Writing a ‘1’ will set the corresponding Add Request bit; writing a ‘0’ has no impact. This enables the processor to set transmission requests for multiple Transmit Buffers with one write to MCAN_TXBAR. MCAN_TXBAR bits are set only for those Transmit Buffers configured via TXBC. When no Transmit scan is running, the bits are reset immediately, else the bits remain set until the Transmit scan process has completed.

Value	Description
0	No transmission request added.
1	Transmission requested added.

51.7.42 PWM Channel Duty Cycle Update Register

Name: PWM_CDTYUPDx
Offset: 0x0208 + x*0x20 [x=0..3]
Reset: –
Property: Write-only

This register acts as a double buffer for the CDTY value. This prevents an unexpected waveform when modifying the waveform duty-cycle.

Only the first 16 bits (channel counter size) are significant.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CDTYUPD[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CDTYUPD[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CDTYUPD[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bits 23:0 – CDTYUPD[23:0] Channel Duty-Cycle Update
Defines the waveform duty-cycle. This value must be defined between 0 and CPRD (PWM_CPRDx).

Figure 58-22. SPI Slave Mode with (CPOL=0 and NCPHA=1) or (CPOL=1 and NCPHA=0)

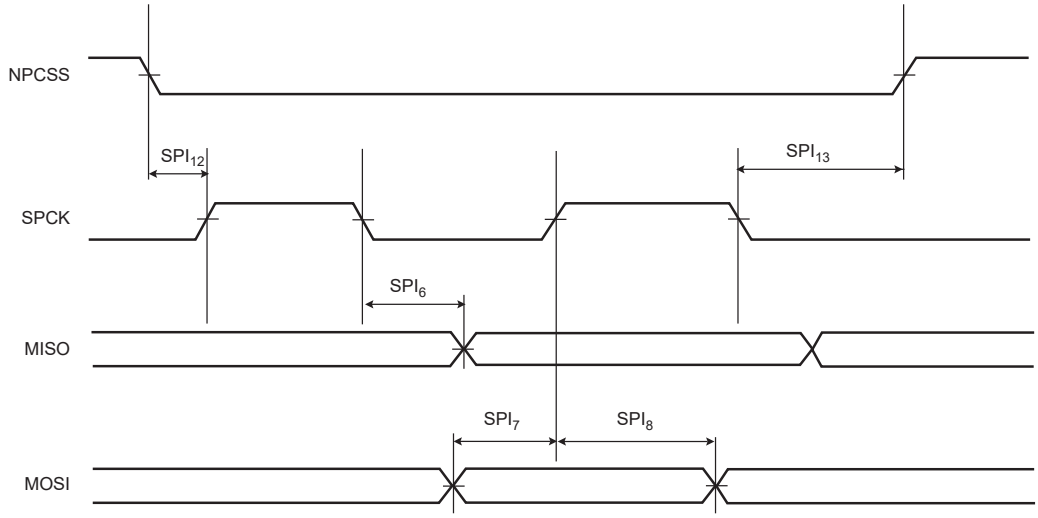
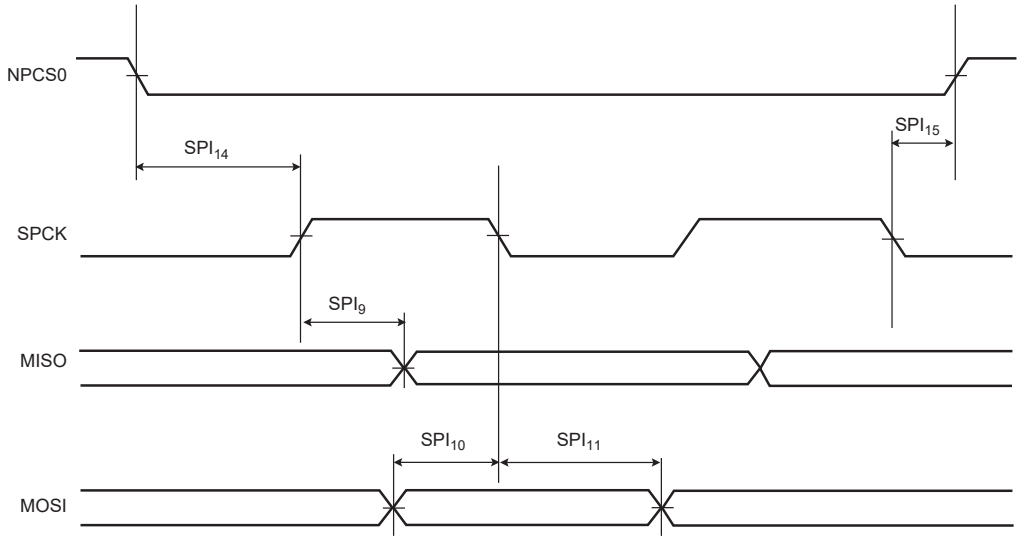


Figure 58-23. SPI Slave Mode with (CPOL = NCPHA = 0) or (CPOL= NCPHA= 1)



58.13.1.6.1 Maximum SPI Frequency

The following formulas give maximum SPI frequency in Master read and write modes and in Slave read and write modes.

$$f_{SPCK}\max = \frac{1}{SPI_0(\text{or } SPI_3) + t_{valid}}$$

t_{valid} is the slave time response to output data after detecting an SPCK edge.

For a nonvolatile memory with t_{valid} (or t_v) = 5 ns, f_{SPCK}max = 57 MHz at V_{DDIO} = 3.3V.

$$f_{SPCK}\max = \frac{1}{2x(SPI_{6max}(\text{or } SPI_{9max}) + t_{setup})}$$

t_{setup} is the setup time from the master before sampling data.

Master Write Mode

The SPI sends data to a slave device only, e.g. an LCD. The limit is given by SPI_2 (or SPI_5) timing. Since it gives a maximum frequency above the maximum pad speed (see I/O Characteristics), the max SPI frequency is the one from the pad.

Symbol	Parameter	Condition	Min	Max	Unit
SSC_3	TF hold time after TK edge (TK output)	–	0	–	ns
SSC_4	TK edge to TF/TD (TK output, TF input)	–	-5.7[(1)]	3.1[(1)]	ns
		STTDLY = 0 START = 4, 5 or 7	-5.7 + (2 × t_{CPMCK})[(1)]	3.1 + (2 × t_{CPMCK})[(1)]	
SSC_5	TF setup time before TK edge (TK input)	–	0	–	ns
SSC_6	TF hold time after TK edge (TK input)	–	t_{CPMCK}	–	ns
SSC_7	TK edge to TF/TD (TK input, TF input)	–	3.6[(1)]	14.7[(1)]	ns
		STTDLY = 0 START = 4, 5 or 7	3.6 + (3 × t_{CPMCK})[(1)]	14.7 + (3 × t_{CPMCK})[(1)]	
Receiver					
SSC_8	RF/RD setup time before RK edge (RK input)	–	0	–	ns
SSC_9	RF/RD hold time after RK edge (RK input)	–	t_{CPMCK}	–	ns
SSC_{10}	RK edge to RF (RK input)	–	3.5[(1)]	12.1[(1)]	ns
SSC_{11}	RF/RD setup time before RK edge (RK output)	–	13.5 - t_{CPMCK}	–	ns
SSC_{12}	RF/RD hold time after RK edge (RK output)	–	t_{CPMCK} - 2.9	–	ns
SSC_{13}	RK edge to RF (RK output)	–	-2.8[(1)]	2.6[(1)]	ns

Note: Note: 1. For output signals (TF, TD, RF), min and max access times are defined. The min access time is the time between the TK (or RK) edge and the signal change. The max access timing is the time between the TK edge and the signal stabilization. The figure below illustrates min and max accesses for SSC0. The same applies for SSC1, SSC4, and SSC7, SSC10 and SSC13.

Table 59-47. Static Performance Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
INL	Integral Non-linearity (see **Note 1**)	No R_{LOAD}	-10	±2	10	LSB
		C_{LOAD} = 50 pF				
		DACC_ACR.IBTLCHx = 3				
DNL	Differential Non-linearity (see **Note 1**)	No R_{LOAD}	-4	±2	4	LSB
		C_{LOAD} = 50 pF				
		DACC_ACR.IBTLCHx = 3				
E_O	Offset Error (see **Note 2**)	–	-8	1	8	mV
E_G	Gain Error	No R_{LOAD}	-1	–	1	%.FSR
		C_{LOAD} = 50 pF				
		DACC_ACR.IBTLCHx = 3				

Note:

1. Best-fit Curve from 0x080 to 0xF7F.
2. Difference between DACx at 0x800 and V_{VREFP}/2.

Table 59-48. Dynamic Performance Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{START}	Startup Time	From DAC on (CHER.CHx) to DAC ready to convert (CHSR.DACRDYx)	–	10	–	µs
t_S	Settling Time Code to Code; i.e., code(n-1) to code(n) ± 0.5 LSB	R_{LOAD} = 5 Kohm C_{LOAD} = 50 pF	–	0.5	–	µs
	Settling Time Full-scale; i.e., 0x000 to 0xFFF ±0.5 LSB	DACC_ACR.IBCTLCHx = 3 FS = 1 MSps	–	1	–	µs
Slew Rate		–	3	–	V/µs	

Table 59-49. Analog Outputs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{LOAD}	Output Resistor Load	Output load resistor	5	–	–	kOhm
C_{LOAD}	Output Capacitor Load	Output load capacitor	–	–	50	pF
V_{DACx_MIN}	Minimum Output Voltage on DACx	Code = 0x000 No R_{LOAD}, C_{LOAD} = 50 pF, DACC_ACR.IBCTLCHx =3	–	0.1	0.5	%. V_{VREFP}

Signal Name	Recommended Pin Connection	Description
		Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop. Supply ripple must not exceed 20 mVrms for 10 kHz to 20 MHz range. **WARNING** Powerup and powerdown sequences given in the "Power Considerations" chapter must be respected.
VDDPLL	Decoupling/filtering capacitors ferrite beads (100 nF and 470 Ohm @ 100 MHz) (1) (2)	Powers the PLLA and the fast RC oscillator. The VDDPLL power supply pin draws small current, but it is noise sensitive. Care must be taken in VDDPLL power supply routing, decoupling and also on bypass capacitors. Supply ripple must not exceed 20 mVrms for 10 kHz to 10 MHz range and 10 mVrms for higher frequencies.
VDDUTMIC	Decoupling/filtering capacitors ferrite beads (100 nF and 470 Ohm @ 100 MHz) (1) (2)	Powers the USB transceiver core. Must always be connected even if the USB is not used. Decoupling/filtering capacitors/ferrite beads must be added to improve startup stability and reduce source voltage drop. Supply ripple must not exceed 10 mVrms for 10 kHz to 10 MHz range.
GND	Voltage Regulator, Core Chip and Peripheral I/O lines ground	GND pins are common to VDDIN, VDDCORE and VDDIO pins. GND pins should be connected as shortly as possible to the system ground plane.
GNDUTMI	UDPHS and UHPHS UTMI+ Core and interface ground	GNDUTMI pins are common to VDDUTMII and VDDUTMIC pins. GNDUTMI pins should be connected as shortly as possible to the system ground plane.
GNDPLL	PLLA cell and Main Oscillator ground	GNDPLL pin is provided for VDDPLL pin. GNDPLL pin should be connected as shortly as possible to the system ground plane.
GNDANA	Analog ground	GNDANA pins are common to AFE, DAC and ACC supplied by VDDIN pin. GNDANA pins should be connected as shortly as possible to the system ground plane.
GNDPLLUSB	USB PLL ground	GNDPLLUSB pin is provided for VDDPLLUSB pin. GNDPLLUSB pin should be connected as shortly as possible to the system ground plane.

Date	Changes
	Section 42.7.9 “QSPI Serial Clock Register”: updated equations. Section 42.7.12 “QSPI Instruction Frame Register”: updated INSTEN bit description.
	Section 43. “Two-wire Interface (TWIHS)” Section 43.6.3.4 “Master Transmitter Mode” and “Read Sequence”: added sentence on clearing TXRDY flag. Section 43.6.5.7 “High-Speed Slave Mode”: updated 11-MHz limit information. Updated Section 43.6.7 “Register Write Protection”. Updated Section 43.7.1 “TWIHS Control Register”: added bit FIFODIS, FIFOEN, LOCKCLR and THRCLR.
	Added Section 45. “Inter-IC Sound Controller (I2SC)”.
08-Feb-16	Section 46. “Universal Synchronous Asynchronous Receiver Transceiver (USART)” Added descriptions of Modem mode and ISO7816 mode throughout. Updated Section 46.1 “Description” and Section 46.2 “Embedded Characteristics”. Table 46-1 “I/O Line Description“ updated and added lines RI, DSR, DCD, and DTR. Section 46.6.1 “Baud Rate Generator”: corrected value in “The frequency of the signal provided on SCK must be at least...” Updated Figure 46-2, “Baud Rate Generator”. “Baud Rate Calculation Example”, corrected formula. Section 46.6.1.2 “Fractional Baud Rate in Asynchronous Mode” and Section 46.7.23 “USART Baud Rate Generator Register”: added warning “When the value of field FP is greater than 0...” Updated Figure 46-3, “Fractional Baud Rate Generator”. Section 46.6.1.3 “Baud Rate in Synchronous Mode or SPI Mode”: corrected formula. Corrected external clock frequency. Corrected SCK maximum frequency. Added Section 46.6.4 ”ISO7816 Mode”. Inserted new Figure 46-27, “RTS Line Software Control when USART_MR.USART_MODE = 2”. Section 46.6.3.4 “Manchester Decoder”: corrected “MANE flag” with “MANERR” flag. Added Section 46.6.7 “Modem Mode”. Section 46.6.8.5 “Character Transmission”: added content to 1st paragraph. Corrected occurrences of RTSEN to RCS, RTSDIS to FCS. Section 46.6.9.8 “Slave Node Synchronization”: updated bullet on oversampling. Updated Figure 46-42, “Slave Node Synchronization”. Section 46.7.1 “USART Control Register”: added bits/fields RSTIT, RSTNACK, DTREN and DTRDIS. Updated RTSDIS bit description.