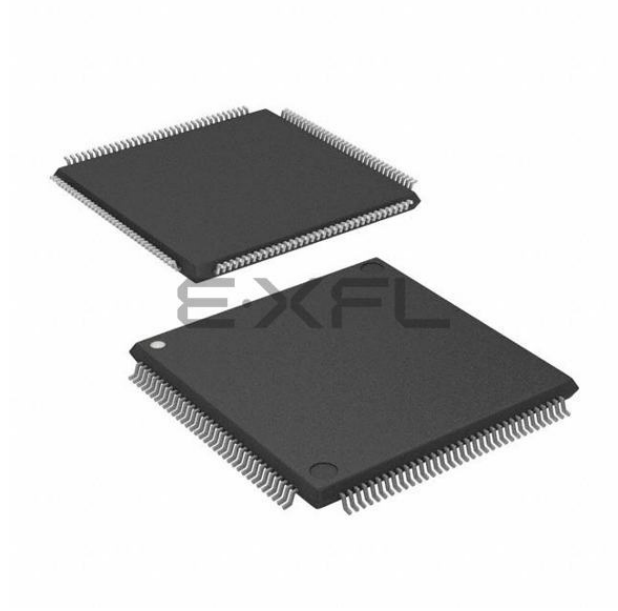

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70q21a-ant

23.5 Register Summary

Offset	Name	Bit Pos.								
0x00	SUPC_CR	7:0					XTALSEL	VROFF		
		15:8								
		23:16								
		31:24	KEY[7:0]							
0x04	SUPC_SMMR	7:0					SMTH[3:0]			
		15:8			SMIEN	SMRSTEN		SMSMPL[2:0]		
		23:16								
		31:24								
0x08	SUPC_MR	7:0								
		15:8		ONREG	BODDIS	BODRSTEN				
		23:16				OSCBYPASS			BKUPRETON	
		31:24	KEY[7:0]							
0x0C	SUPC_WUMR	7:0	LPDBCCLR	LPDBCEN1	LPDBCEN0		RTCEN	RTTEN	SMEN	
		15:8		WKUPDBC[2:0]						
		23:16						LPDBC[2:0]		
		31:24								
0x10	SUPC_WUIR	7:0	WKUPEN[7:0]							
		15:8			WKUPEN[13:8]					
		23:16	WKUPT[7:0]							
		31:24			WKUPT[13:8]					
0x14	SUPC_SR	7:0	OSCSEL	SMOS	SMS	SMRSTS	BODRSTS	SMWS	WKUPS	
		15:8		LPDBCS1	LPDBCS0					
		23:16	WKUPIS[7:0]							
		31:24			WKUPIS[13:8]					
0x18 ... 0xD3	Reserved									
0xD4	SYSC_WPMR	7:0								WPEN
		15:8	WPKEY[7:0]							
		23:16	WPKEY[15:8]							
		31:24	WPKEY[23:16]							

Bit 1 – ALRDIS Alarm Interrupt Disable

Value	Description
0	No effect.
1	The alarm interrupt is disabled.

Bit 0 – ACKDIS Acknowledge Update Interrupt Disable

Value	Description
0	No effect.
1	The acknowledge for update interrupt is disabled.

32.6.1.43 PIO Rising Edge/High-Level Select Register

Name: PIO_REHLSR
Offset: 0x00D4
Property: Write-only

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Rising Edge/High-Level Interrupt Selection

Value	Description
0	No effect.
1	The interrupt source is set to a rising edge detection or high-level detection event, depending on PIO_ELSR.

This field defines the delay between a Precharge Command and another Command in number of cycles. Number of cycles is between 0 and 15.

Bits 15:12 – TRC_TRFC[3:0] Row Cycle Delay and Row Refresh Cycle
Reset value is seven cycles.

This field defines two timings:

- the delay (t_{RFC}) between two Refresh commands and between a Refresh command and an Activate command
- the delay (t_{RC}) between two Active commands in number of cycles.

The number of cycles is between 0 and 15. The end user must program max {t_{RC}, t_{RFC}}.

Bits 11:8 – TWR[3:0] Write Recovery Delay
Reset value is two cycles.

This field defines the Write Recovery Time in number of cycles. Number of cycles is between 0 and 15.

Bit 7 – DBW Data Bus Width
Reset value is 16 bits.

This bit defines the Data Bus Width, which is 16 bits. It must be set to 1.

Value	Description
0	Data bus width is 32 bits.
1	Data bus width is 16 bits.

Bits 6:5 – CAS[1:0] CAS Latency
Reset value is two cycles. In the SDRAMC, only a CAS latency of two and three cycles is managed.

Value	Name	Description
0	Reserved	–
1	Reserved	–
1	LATENCY1	1 cycle latency
2	LATENCY2	2 cycle latency
3	LATENCY3	3 cycle latency

Bit 4 – NB Number of Banks
Reset value is two banks.

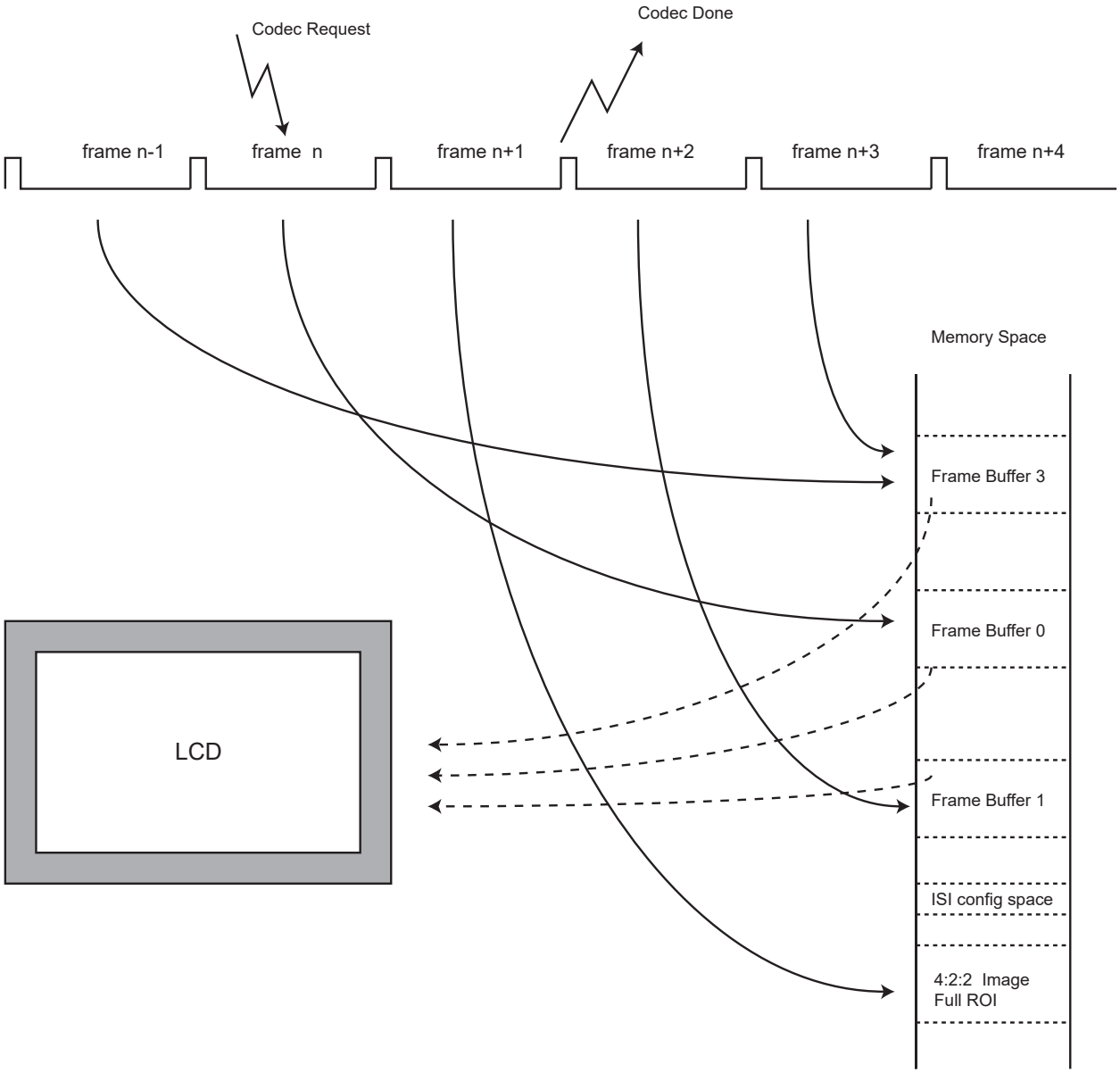
Value	Name	Description
0	BANK2	2 banks
1	BANK4	4 banks

Bits 3:2 – NR[1:0] Number of Row Bits
Reset value is 11 row bits.

Value	Name	Description
0	ROW11	11 bits to define the row number, up to 2048 rows
1	ROW12	12 bits to define the row number, up to 4096 rows
2	ROW13	13 bits to define the row number, up to 8192 rows
3	Reserved	

Using this technique, several frame buffers can be configured through the linked list. The following figure illustrates a typical three-frame buffer application. Frame n is mapped to frame buffer 0, frame n+1 is mapped to frame buffer 1, frame n+2 is mapped to frame buffer 2 and further frames wrap. A codec request occurs, and the full-size 4:2:2 encoded frame is stored in a dedicated memory space.

Figure 37-6. Three Frame Buffers Application and Memory Mapping



37.5.5 Codec Path

37.5.5.1 Color Space Conversion

Depending on user selection, this module can be bypassed so that input YCrCb stream is directly connected to the format converter module. If the RGB input stream is selected, this module converts RGB to YCrCb color space with the formulas given below:

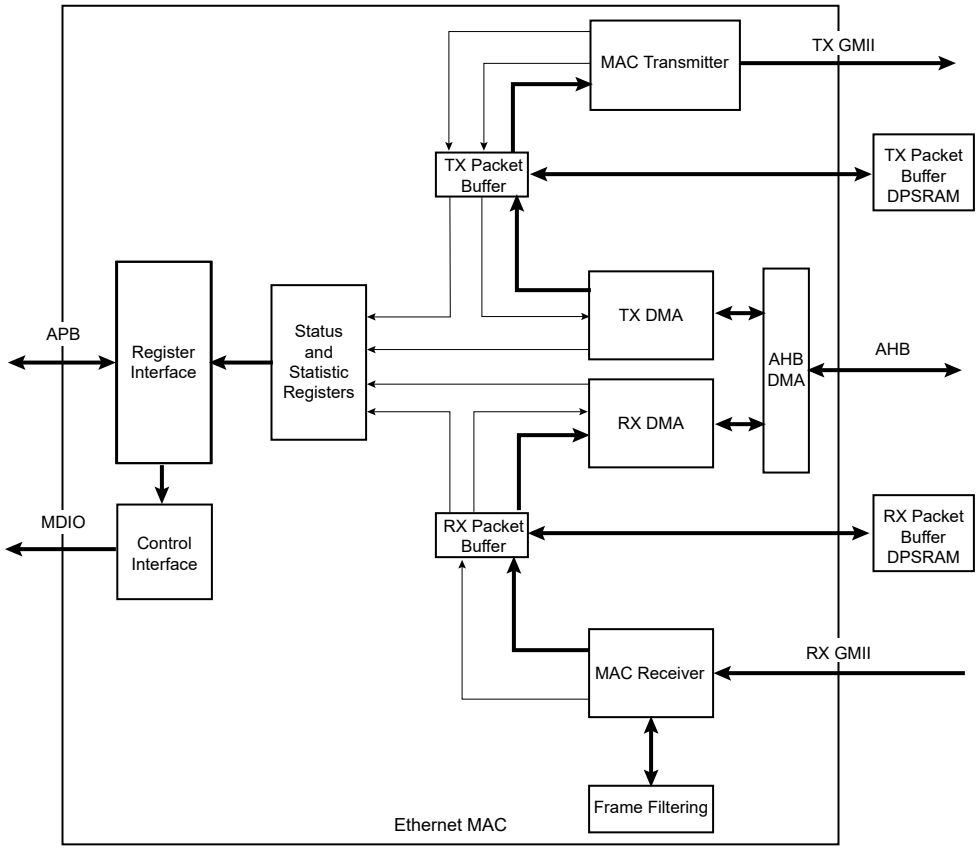
As described above, the DMA can be programmed into a low latency mode, known as Partial Store and Forward. For further details of this mode, see the related Links.

When the DMA is in full store and forward mode, full packets are buffered which provides the possibility to:

- Discard packets with error on the receive path before they are partially written out of the DMA, thus saving AHB bus bandwidth and driver processing overhead,
- Retry collided transmit frames from the buffer, thus saving AHB bus bandwidth,
- Implement transmit IP/TCP/UDP checksum generation offload.

With the packet buffers included, the structure of the GMAC data paths is shown in this image:

Figure 38-2. Data Paths with Packet Buffers Included



38.6.3.7 Transmit Packet Buffer

The transmitter packet buffer will continue attempting to fetch frame data from the AHB system memory until the packet buffer itself is full, at which point it will attempt to maintain its full level.

To accommodate the status and statistics associated with each frame, three words per packet (or two if the GMAC is configured in 64-bit data path mode) are reserved at the end of the packet data. If the packet is bad and requires to be dropped, the status and statistics are the only information held on that packet. Storing the status in the DPRAM is required in order to decouple the DMA interface of the buffer from the MAC interface, to update the MAC status/statistics and to generate interrupts in the order in which the packets that they represent were fetched from the AHB memory.

If any errors occur on the AHB while reading the transmit frame, the fetching of packet data from AHB memory is halted. The MAC transmitter will continue to fetch packet data, thereby emptying the packet

39.6.33 Host Global Interrupt Clear Register

Name: USBHS_HSTICR
Offset: 0x0408
Property: Write-only

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Clears the corresponding bit in USBHS_HSTISR.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		HWUPIC	HSOFIC	RXRSMIC	RSMEDIC	RSTIC	DDISCIC	DCONNIC
Access								
Reset								

Bit 6 – HWUPIC Host Wakeup Interrupt Clear

Bit 5 – HSOFIC Host Start of Frame Interrupt Clear

Bit 4 – RXRSMIC Upstream Resume Received Interrupt Clear

Bit 3 – RSMEDIC Downstream Resume Sent Interrupt Clear

Bit 2 – RSTIC USB Reset Sent Interrupt Clear

Bit 1 – DDISCIC Device Disconnection Interrupt Clear

Bit 0 – DCONNIC Device Connection Interrupt Clear

40.14.20 HSMCI FIFOx Memory Aperture

Name: HSMCI_FIFOx [x=0..255]
Offset: 0x00
Reset: 0
Property: R/W

Bit	31	30	29	28	27	26	25	24
	DATA[31:24]							
Access								
Reset	0	0	0	0	0	0	0	0

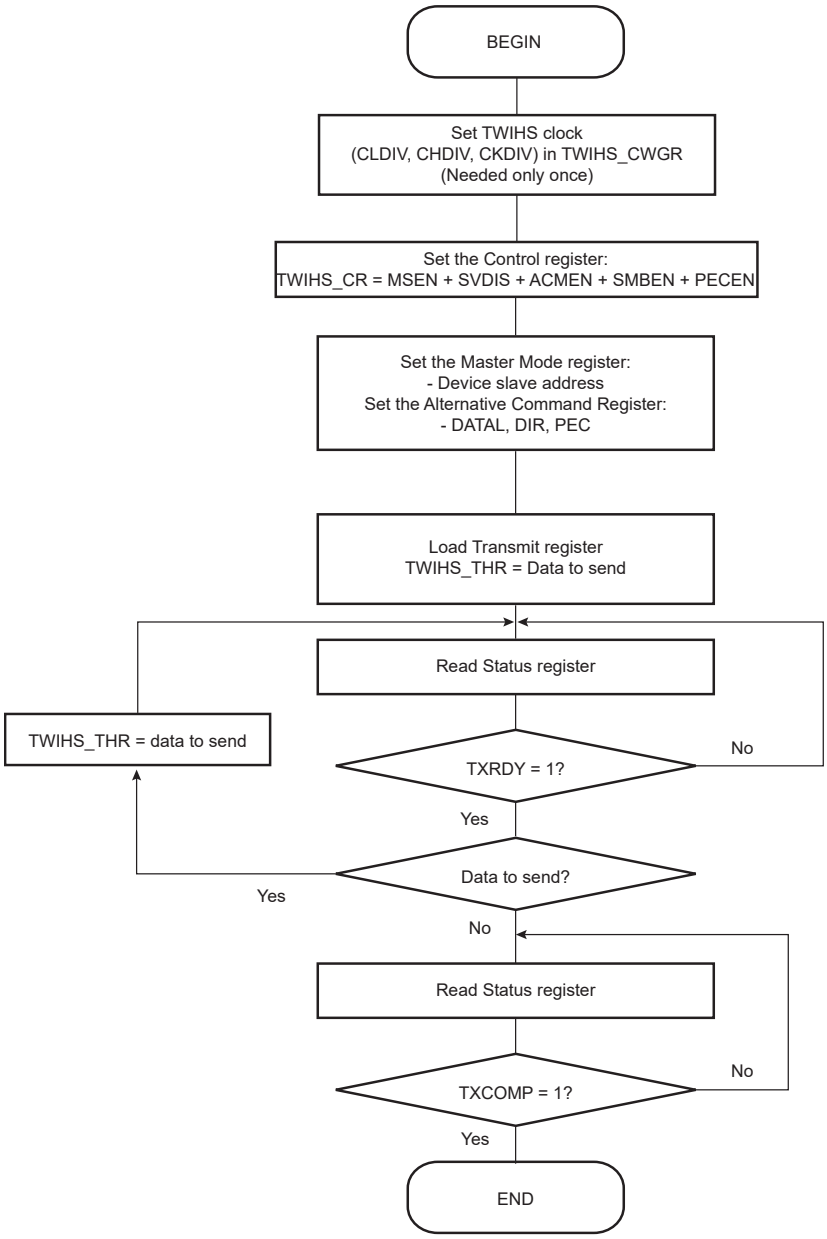
Bit	23	22	21	20	19	18	17	16
	DATA[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DATA[31:0] Data to Read or Data to Write

Figure 43-18. SMBus Write Operation with Multiple Data Bytes with PEC and Alternative Command Mode



1: When both holding register and internal shifter are empty and STOP condition has been sent.

TXCOMP behavior in Master mode can be seen in Master Write with One-Byte Internal Address and Multiple Data Bytes and in Master Read with Multiple Data Bytes.

- TXCOMP used in Slave mode:

0: As soon as a START is detected.

1: After a STOP or a REPEATED START + an address different from SADR is detected.

TXCOMP behavior in Slave mode can be seen in Clock Stretching in Read Mode, Clock Stretching in Write Mode, Repeated Start and Reversal from Read Mode to Write Mode and Repeated Start and Reversal from Write Mode to Read Mode.

48.7.10 HBI Channel Mask 1 Register

Name: MLB_HCMR1
Offset: 0x08C
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	CHM: Bitwise Channel Mask Bit [63[31:24]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CHM: Bitwise Channel Mask Bit [63[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CHM: Bitwise Channel Mask Bit [63[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CHM: Bitwise Channel Mask Bit [63[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CHM: Bitwise Channel Mask Bit [63[31:0] 32]
CHM[n] = 1 indicates that channel n can generate an interrupt.

48.7.23 MIF Control Register

Name: MLB_MCTL
Offset: 0x0E0
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								XCMP
Access								
Reset								0

Bit 0 – XCMP Transfer Complete (Write 0 to Clear)

0: Received frame matching filter index FIDX.

1: Received frame did not match any Rx filter element.

• R1 Bits 30:24 FIDX[6:0]: Filter Index

0-127: Index of matching Rx acceptance filter element (invalid if ANMF = '1').
Range is 0 to MCAN_SIDFC.LSS - 1 resp. MCAN_XIDFC.LSE - 1.

• R1 Bit 21 FDF: FD Format

0: Standard frame format.

1: CAN FD frame format (new DLC-coding and CRC).

• R1 Bit 20 BRS: Bit Rate Switch

0: Frame received without bit rate switching.

1: Frame received with bit rate switching.

Note:
Bits ESI, FDF, and BRS are only evaluated when CAN FD operation is enabled (MCAN_CCCR.FDOE = 1). Bit BRS is only evaluated when in addition MCAN_CCCR.BRSE = 1.

• R1 Bits 19:16 DLC[3:0]: Data Length Code

0-8: CAN + CAN FD: received frame has 0-8 data bytes.

9-15: CAN: received frame has 8 data bytes.

9-15: CAN FD: received frame has 12/16/20/24/32/48/64 data bytes.

• R1 Bits 15:0 RXTS[15:0]: Rx Timestamp

Timestamp Counter value captured on start of frame reception. Resolution depending on configuration of the Timestamp Counter Prescaler MCAN_TSCC.TCP.

• R2 Bits 31:24 DB3[7:0]: Data Byte 3

• R2 Bits 23:16 DB2[7:0]: Data Byte 2

• R2 Bits 15:8 DB1[7:0]: Data Byte 1

• R2 Bits 7:0 DB0[7:0]: Data Byte 0

• R3 Bits 31:24 DB7[7:0]: Data Byte 7

• R3 Bits 23:16 DB6[7:0]: Data Byte 6

• R3 Bits 15:8 DB5[7:0]: Data Byte 5

• R3 Bits 7:0 DB4[7:0]: Data Byte 4

... ...

• Rn Bits 31:24 DBm[7:0]: Data Byte m

• Rn Bits 23:16 DBm-1[7:0]: Data Byte m-1

• Rn Bits 15:8 DBm-2[7:0]: Data Byte m-2

• Rn Bits 7:0 DBm-3[7:0]: Data Byte m-3

Note: Depending on the configuration of the element size (MCAN_RXESC), between two and sixteen 32-bit words (Rn = 3 ..17) are used for storage of a CAN message's data field.

SFID2[10:9] decides whether the received message is stored into an Rx Buffer or treated as message A, B, or C of the debug message sequence.

0: Store message in a Rx buffer

1: Debug Message A

2: Debug Message B

3: Debug Message C

SFID2[5:0] defines the index of the dedicated Rx Buffer element to which a matching message is stored.

49.5.7.6 Extended Message ID Filter Element

Up to 64 filter elements can be configured for 29-bit extended IDs. When accessing an Extended Message ID Filter element, its address is the Filter List Extended Start Address MCAN_XIDFC.FLESA plus two times the index of the filter element (0…63).

Table 49-11. Extended Message ID Filter Element

	31			24	23	16	15	8	7	0
F0	EFEC [2:0]			EFID1[28:0]						
F1	EFT[1:0]		–	EFID2[28:0]						

• F0 Bit 31:29 EFEC[2:0]: Extended Filter Element Configuration

All enabled filter elements are used for acceptance filtering of extended frames. Acceptance filtering stops at the first matching enabled filter element or when the end of the filter list is reached. If EFEC = “100”, “101”, or “110”, a match sets the interrupt flag MCAN_IR.HPM and, if enabled, an interrupt is generated. In this case, register MCAN_HPMS is updated with the status of the priority match.

0: Disable filter element

1: Store in Rx FIFO 0 if filter matches

2: Store in Rx FIFO 1 if filter matches

3: Reject ID if filter matches

4: Set priority if filter matches

5: Set priority and store in FIFO 0 if filter matches

6: Set priority and store in FIFO 1 if filter matches

7: Store into Rx Buffer or as debug message, configuration of EFT[1:0] ignored

• F0 Bits 28:0 EFID1[28:0]: Extended Filter ID 1

First ID of extended ID filter element.

When filtering for Rx Buffers or for debug messages this field defines the ID of an extended message to be stored. The received identifiers must match exactly, only MCAN_XIDAM masking mechanism (see Extended Message ID Filtering) is used.

• F1 Bits 31:30 EFT[1:0]: Extended Filter Type

0: Range filter from EF1ID to EF2ID (EF2ID ≥ EF1ID)

Offset	Name	Bit Pos.								
		31:24								
0x8C	TC_RAB2	7:0	RAB[7:0]							
		15:8	RAB[15:8]							
		23:16	RAB[23:16]							
		31:24	RAB[31:24]							
0x90	TC_CV2	7:0	CV[7:0]							
		15:8	CV[15:8]							
		23:16	CV[23:16]							
		31:24	CV[31:24]							
0x94	TC_RA2	7:0	RA[7:0]							
		15:8	RA[15:8]							
		23:16	RA[23:16]							
		31:24	RA[31:24]							
0x98	TC_RB2	7:0	RB[7:0]							
		15:8	RB[15:8]							
		23:16	RB[23:16]							
		31:24	RB[31:24]							
0x9C	TC_RC2	7:0	RC[7:0]							
		15:8	RC[15:8]							
		23:16	RC[23:16]							
		31:24	RC[31:24]							
0xA0	TC_SR2	7:0	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
		15:8								
		23:16						MTIOB	MTIOA	CLKSTA
		31:24								
0xA4	TC_IER2	7:0	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
		15:8								
		23:16								
		31:24								
0xA8	TC_IDR2	7:0	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
		15:8								
		23:16								
		31:24								
0xAC	TC_IMR2	7:0	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
		15:8								
		23:16								
		31:24								
0xB0	TC_EMR2	7:0			TRIGSRCB[1:0]				TRIGSRCA[1:0]	
		15:8								NODIVCLK
		23:16								
		31:24								
0xB4 ... 0xBF	Reserved									
0xC0	TC_BCR	7:0								SYNC
		15:8								

Value	Name	Description
0	UP	UP mode without automatic trigger on RC Compare
1	UPDOWN	UPDOWN mode without automatic trigger on RC Compare
2	UP_RC	UP mode with automatic trigger on RC Compare
3	UPDOWN_RC	UPDOWN mode with automatic trigger on RC Compare

Bit 12 – ENETRG External Event Trigger Enable
Whatever the value programmed in ENETRG, the selected external event only controls the TIOAx output and TIOBx if not used as input (trigger event input or other input used).

Value	Description
0	The external event has no effect on the counter and its clock.
1	The external event resets the counter and starts the counter clock.

Bits 11:10 – EEVT[1:0] External Event Selection
Signal selected as external event.

Value	Name	Description	TIOB Direction
0	TIOB	TIOB	Input
1	XC0	XC0	Output
2	XC1	XC1	Output
3	XC2	XC2	Output

Note: If TIOB is chosen as the external event signal, it is configured as an input and no longer generates waveforms and subsequently no IRQs.

Bits 9:8 – EEVTEDG[1:0] External Event Edge Selection

Value	Name	Description
0	NONE	None
1	RISING	Rising edge
2	FALLING	Falling edge
3	EDGE	Each edge

Bit 7 – CPCDIS Counter Clock Disable with RC Compare

Value	Description
0	Counter clock is not disabled when counter reaches RC.
1	Counter clock is disabled when counter reaches RC.

Bit 6 – CPCSTOP Counter Clock Stopped with RC Compare

Value	Description
0	Counter clock is not stopped when counter reaches RC.
1	Counter clock is stopped when counter reaches RC.

Bits 5:4 – BURST[1:0] Burst Signal Selection

50.7.14 TC Extended Mode Register

Name: TC_EMRx
Offset: 0x30 + x*0x40 [x=0..2]
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the TC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit 8 – NODIVCLK No Divided Clock

Value	Description
0	The selected clock is defined by field TCCLKS in TC_CMRx.
1	The selected clock is peripheral clock and TCCLKS field (TC_CMRx) has no effect.

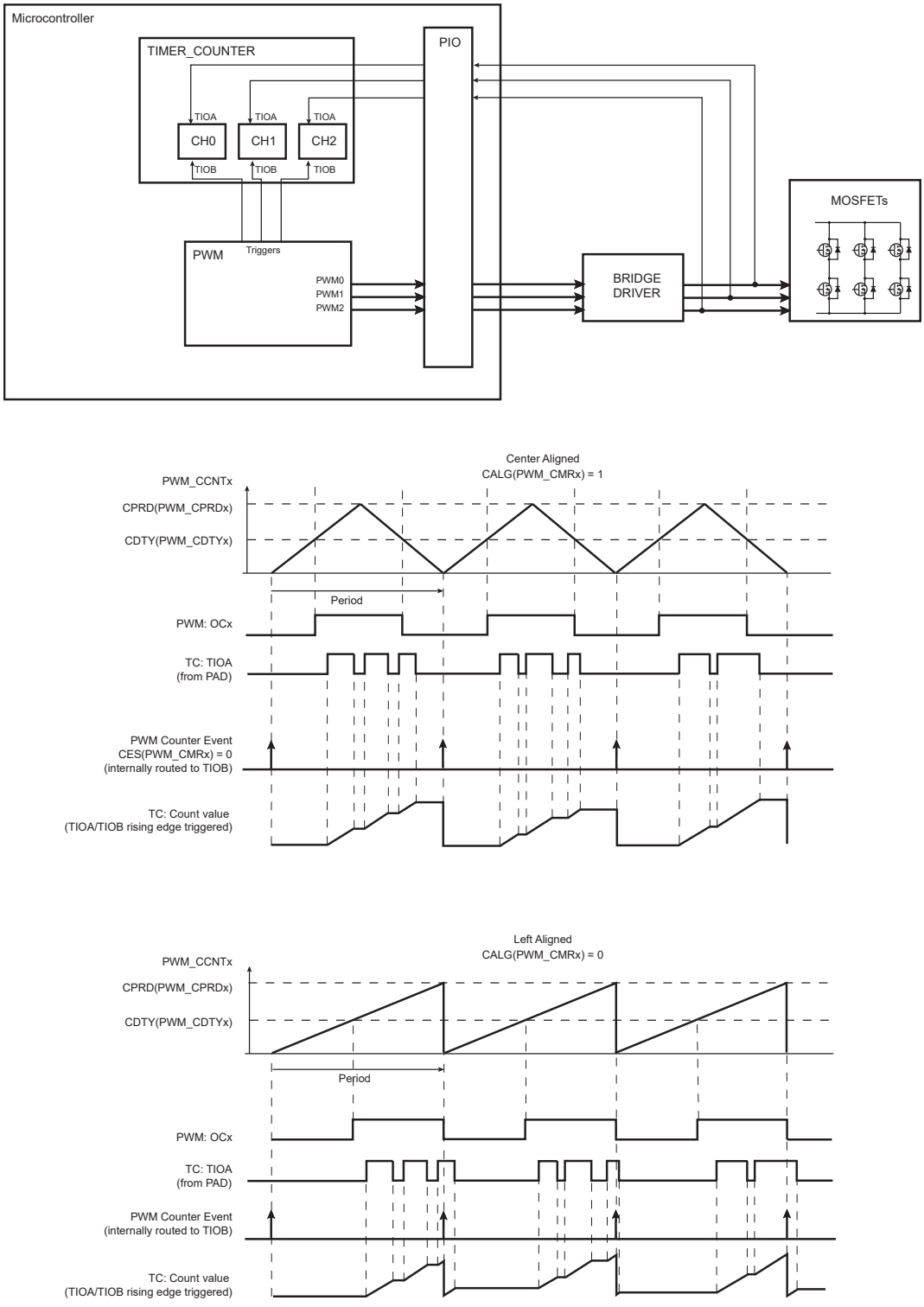
Bits 5:4 – TRIGSRCB[1:0] Trigger Source for Input B

Value	Name	Description
0	EXTERNAL_TIOBx	The trigger/capture input B is driven by external pin TIOBx
1	PWMx	For TC0 to TC10: The trigger/capture input B is driven internally by the comparator output (see Synchronization with PWM) of the PWMx. For TC11: The trigger/capture input B is driven internally by the GTSUCOMP signal of the Ethernet MAC (GMAC).

Bits 1:0 – TRIGSRCA[1:0] Trigger Source for Input A

Value	Name	Description
0	EXTERNAL_TIOAx	The trigger/capture input A is driven by external pin TIOAx
1	PWMx	The trigger/capture input A is driven internally by PWMx

Figure 51-7. Triggering the TC: Cumulated "ON" Time Measurement



51.6.2.4 2-bit Gray Up/Down Counter for Stepper Motor

A pair of channels may provide a 2-bit gray count waveform on two outputs. Dead-time generator and other downstream logic can be configured on these channels.

Up or Down Count mode can be configured on-the-fly by means of PWM_SMMR configuration registers.

51.7.5 PWM Interrupt Enable Register 1

Name: PWM_IER1
Offset: 0x10
Reset: –
Property: Write-only

This register can only be written if bits WPSWS1 and WPHWS1 are cleared in the PWM Write Protection Status Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					FCHID3	FCHID2	FCHID1	FCHID0
Access					W	W	W	W
Reset					0	0	0	–

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					CHID3	CHID2	CHID1	CHID0
Access					W	W	W	W
Reset					0	0	0	–

Bits 16, 17, 18, 19 – FCHIDx Fault Protection Trigger on Channel x Interrupt Enable

Bits 0, 1, 2, 3 – CHIDx Counter Event on Channel x Interrupt Enable

57.5.3 AES Interrupt Enable Register

Name: AES_IER
Offset: 0x10
Reset: –
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
								TAGRDY
Access								W
Reset								–

Bit	15	14	13	12	11	10	9	8
								URAD
Access								W
Reset								–

Bit	7	6	5	4	3	2	1	0
								DATRDY
Access								W
Reset								–

Bit 16 – TAGRDY GCM Tag Ready Interrupt Enable

Bit 8 – URAD Unspecified Register Access Detection Interrupt Enable

Bit 0 – DATRDY Data Ready Interrupt Enable