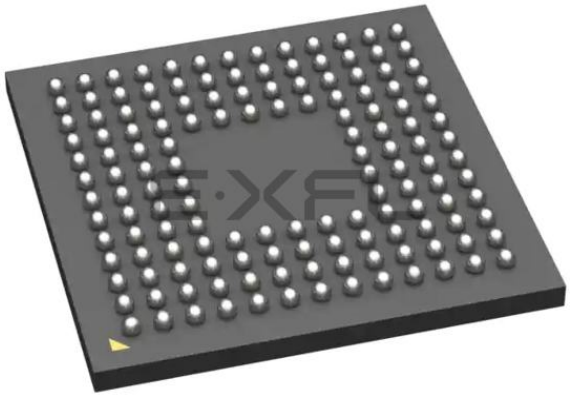

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70q21a-cfnt

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Description
67	GMAC	Q2	–	GMAC Queue 2 Interrupt signal toggled on a DMA write to the first word of each DMA data buffer associated with queue 2
66	–	–	–	Reserved
67	–	–	–	Reserved
68	ARM	IXC	–	Floating Point Unit Interrupt IXC associated with FPU cumulative exception bit
69	I2SC0	X	X	Inter-IC Sound Controller
70	I2SC1	X	X	Inter-IC Sound Controller
71	GMAC	Q3	–	GMAC Queue 3 Interrupt signal toggled on a DMA write to the first word of each DMA data buffer associated with queue 3
72	GMAC	Q4	–	GMAC Queue 4 Interrupt signal toggled on a DMA write to the first word of each DMA data buffer associated with queue 4
73	GMAC	Q5	–	GMAC Queue 5 Interrupt signal toggled on a DMA write to the first word of each DMA data buffer associated with queue 5

14.2 Peripheral Signal Multiplexing on I/O Lines

The SAM E70/S70/V70/V71 features

- Two PIO controllers on 64-pin versions (PIOA and PIOB)
- Three PIO controllers on the 100-pin version (PIOA, PIOB and PIOD)
- Five PIO controllers on the 144-pin version (PIOA, PIOB, PIOC, PIOD and PIOE), that multiplex the I/O lines of the peripheral set.

The SAM E70/S70/V70/V71 PIO Controllers control up to 32 lines and each line can be assigned to one of four peripheral functions: A, B, C or D.

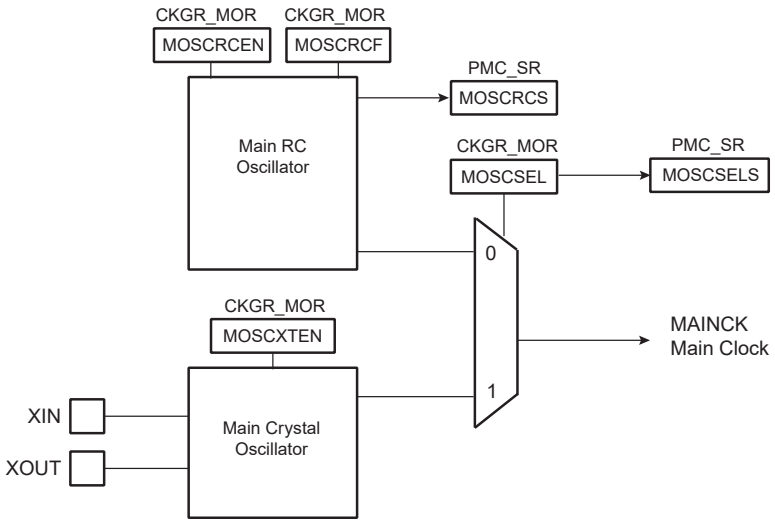
For more information on multiplexed signals, refer to the “Package and Pinout” chapter.

22.5.2 EEFC Flash Command Register

Name: EEFC_FCR
Offset: 0x04
Property: Write-only

GETD, GLB, GGPB, STUI, SPUI, GCALB, WUS, EUS, STUS, SPUS, EA	Commands requiring no argument, including Erase all command	FARG is meaningless, must be written with 0
ES	Erase sector command	FARG must be written with any page number within the sector to be erased
EPA	Erase pages command	FARG[1:0] defines the number of pages to be erased The start page must be written in FARG[15:2]. FARG[1:0] = 0: Four pages to be erased. FARG[15:2] = Page_Number / 4 FARG[1:0] = 1: Eight pages to be erased. FARG[15:3] = Page_Number / 8, FARG[2]=0 FARG[1:0] = 2: Sixteen pages to be erased. FARG[15:4] = Page_Number / 16, FARG[3:2]=0 FARG[1:0] = 3: Thirty-two pages to be erased. FARG[15:5] = Page_Number / 32, FARG[4:2]=0 Refer to “EEFC_FCR.FARG Field for EPA Command”.
WP, WPL, EWP, EWPL	Programming commands	FARG must be written with the page number to be programmed
SLB, CLB	Lock bit commands	FARG defines the page number to be locked or unlocked
SGPB, CGPB	GPNVM commands	FARG defines the GPNVM number to be programmed

Figure 30-2. Main Clock (MAINCK) Block Diagram



30.5.1 Main RC Oscillator

After reset, the Main RC oscillator is enabled with the 12 MHz frequency selected. This oscillator is selected as the source of MAINCK. MAINCK is the default clock selected to start the system.

Only the 8/12 MHz RC oscillator frequencies are calibrated in production. Refer to the section “Electrical Characteristics”.

The software can disable or enable the Main RC oscillator with the MOSCRCEN bit in the Clock Generator Main Oscillator Register (CKGR_MOR).

The output frequency of the Main RC oscillator can be selected among 4, 8 or 12 MHz. Selection is done by configuring the field MOSCRCF in CKGR_MOR. When changing the frequency selection, the MOSCRCS bit in the Power Management Controller Status Register (PMC_SR) is automatically cleared and MAINCK is stopped until the oscillator is stabilized. Once the oscillator is stabilized, MAINCK restarts and PMC_SR.MOSCRCS is set. Note that enabling the Main RC oscillator (MOSCRCEN = 1) and changing its frequency (MOSCRCF) at the same time is not allowed.

This oscillator must be enabled first and its frequency changed in a second step.

When disabling the Main RC oscillator by clearing the CKGR_MOR.MOSCRCEN bit, the PMC_SR.MOSCRCS bit is automatically cleared, indicating that the oscillator is OFF.

Setting the MOSCRCS bit in the Power Management Controller Interrupt Enable Register (PMC_IER) triggers an interrupt to the processor.

Related Links

58. Electrical Characteristics for SAM V70/V71
59. Electrical Characteristics for SAM E70/S70

30.5.2 Main RC Oscillator Frequency Adjustment

The 8 MHz and 12 MHz frequencies are factory-centered to the typical values by using Flash calibration bits (refer to the “Electrical Characteristics” chapter).

The Flash calibration bits setting the Main RC oscillator frequency to 8 MHz and 12 MHz vary from device to device. To get a starting point when changing the CAL8 or CAL12 fields, it is recommended to first read their corresponding Flash calibration bits in the Flash Controller.

Specific Address 1 Bottom register (GMAC_SAB1) (Address 0x088) 0x87654321

Specific Address 1 Top register (GMAC_SAT1) (Address 0x08C) 0x0000CBA9

For a successful match to the type ID, the following Type ID Match 1 register must be set up:

Type ID Match 1 register (GMAC_TIDM1) (Address 0x0A8) 0x80004321

38.6.8 Broadcast Address

Frames with the broadcast address of 0xFFFFFFFFFFFF are stored to memory only if the 'no broadcast' bit in the Network Configuration register is set to zero.

38.6.9 Hash Addressing

The hash address register is 64 bits long and takes up two locations in the memory map. The least significant bits are stored in Hash Register Bottom and the most significant bits in Hash Register Top.

The unicast hash enable and the multicast hash enable bits in the Network Configuration register enable the reception of hash matched frames. The destination address is reduced to a 6-bit index into the 64-bit Hash register using the following hash function: The hash function is an XOR of every sixth bit of the destination address.

hash_index[05] = da[05] ^ da[11] ^ da[17] ^ da[23] ^ da[29] ^ da[35] ^ da[41] ^ da[47]

hash_index[04] = da[04] ^ da[10] ^ da[16] ^ da[22] ^ da[28] ^ da[34] ^ da[40] ^ da[46]

hash_index[03] = da[03] ^ da[09] ^ da[15] ^ da[21] ^ da[27] ^ da[33] ^ da[39] ^ da[45]

hash_index[02] = da[02] ^ da[08] ^ da[14] ^ da[20] ^ da[26] ^ da[32] ^ da[38] ^ da[44]

hash_index[01] = da[01] ^ da[07] ^ da[13] ^ da[19] ^ da[25] ^ da[31] ^ da[37] ^ da[43]

hash_index[00] = da[00] ^ da[06] ^ da[12] ^ da[18] ^ da[24] ^ da[30] ^ da[36] ^ da[42]

da[0] represents the least significant bit of the first byte received, that is, the multicast/unicast indicator, and da[47] represents the most significant bit of the last byte received.

If the hash index points to a bit that is set in the Hash register then the frame will be matched according to whether the frame is multicast or unicast.

A multicast match will be signaled if the multicast hash enable bit is set, da[0] is logic 1 and the hash index points to a bit set in the Hash register.

A unicast match will be signaled if the unicast hash enable bit is set, da[0] is logic 0 and the hash index points to a bit set in the Hash register.

To receive all multicast frames, the Hash register should be set with all ones and the multicast hash enable bit should be set in the Network Configuration register.

38.6.10 Copy all Frames (Promiscuous Mode)

If the Copy All Frames bit is set in the Network Configuration register then all frames (except those that are too long, too short, have FCS errors or have GRXER asserted during reception) will be copied to memory. Frames with FCS errors will be copied if bit 26 is set in the Network Configuration register.

38.6.11 Disable Copy of Pause Frames

Pause frames can be prevented from being written to memory by setting the disable copying of pause frames control bit 23 in the Network Configuration register. When set, pause frames are not copied to memory regardless of the Copy All Frames bit, whether a hash match is found, a type ID match is identified or if a destination address match is found.

38.8.48 GMAC 512 to 1023 Byte Frames Transmitted Register

Name: GMAC_TBFT1023
Offset: 0x128
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	NFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFTX[31:0] 512 to 1023 Byte Frames Transmitted without Error
This register counts the number of 512 to 1023 byte frames successfully transmitted without error, i.e., no underrun and not too many retries.

Bit 6 – STALLEDEC STALLed Interrupt Clear

Bit 5 – OVERFEC Overflow Interrupt Clear

Bit 4 – NAKINEC NAKed IN Interrupt Clear

Bit 3 – NAKOUTEC NAKed OUT Interrupt Clear

Bit 2 – RXSTPEC Received SETUP Interrupt Clear

Bit 1 – RXOUTEC Received OUT Data Interrupt Clear

Bit 0 – TXINEC Transmitted IN Interrupt Clear

39.6.24 Device Endpoint Interrupt Disable Register (Isochronous Endpoints)

Name: USBHS_DEVEPTIDRx (ISOENPT)
Offset: 0x0220 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

This register view is relevant only if EPTYPE = 0x1 in "Device Endpoint x Configuration Register".

For additional information, see "Device Endpoint x Mask Register (Isochronous Endpoints)".

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Clears the corresponding bit in USBHS_DEVEPTIMRx.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
								EPDISHDMAC
Access								
Reset								0

Bit	15	14	13	12	11	10	9	8
		FIFOCONC		NBUSYBKEC		ERRORTRANSEC	DATAXEC	MDATEC
Access								
Reset		0		0		0	0	0

Bit	7	6	5	4	3	2	1	0
	SHORTPACKETEC	CRCERREC	OVERFEC	HBISOFLUSHEC	HBISOINERREC	UNDERFEC	RXOUTEC	TXINEC
Access								
Reset	0	0	0	0	0	0	0	0

Bit 16 – EPDISHDMAC Endpoint Interrupts Disable HDMA Request Clear

Bit 14 – FIFOCONC FIFO Control Clear

Bit 12 – NBUSYBKEC Number of Busy Banks Interrupt Clear

Bit 10 – ERRORTRANSEC Transaction Error Interrupt Clear

Bit 9 – DATAXEC DataX Interrupt Clear

Bit 8 – MDATEC MData Interrupt Clear

39.6.64 Host Pipe x Error Register

Name: USBHS_HSTPIPERRx
Offset: 0x0680 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

Writing a zero in a bit/field in this register clears the bit/field. Writing a one has no effect.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
Access								
Reset		0	0	0	0	0	0	0

Bits 6:5 – COUNTER[1:0] Error Counter
This field is incremented each time an error occurs (CRC16, TIMEOUT, PID, DATAPID or DATATGL).

This field is cleared when receiving a USB packet free of error.

When this field reaches 3 (i.e., 3 consecutive errors), this pipe is automatically frozen (USBHS_HSTPIPIMRx.PFREEZE is set).

Bit 4 – CRC16 CRC16 Error

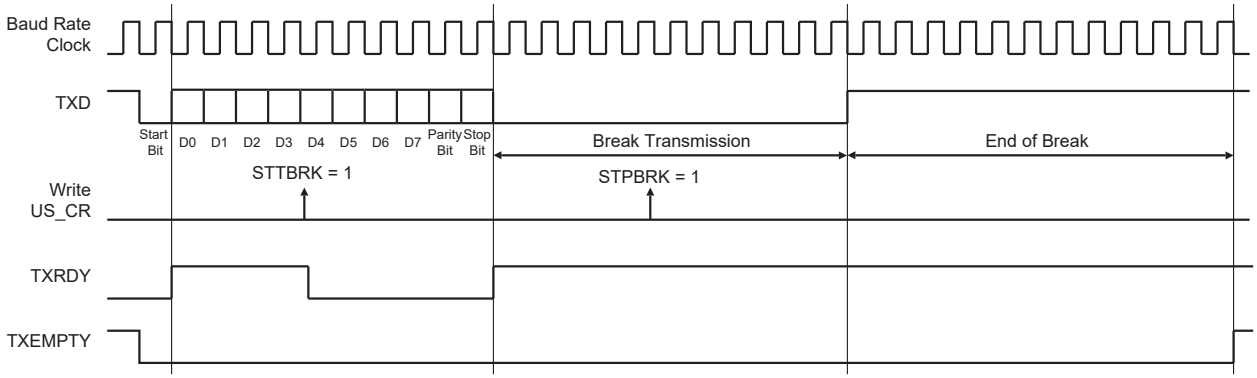
Value	Description
0	No CRC16 error occurred since last clear of this bit.
1	This bit is automatically set when a CRC16 error has been detected.

Bit 3 – TIMEOUT Time-Out Error

Value	Description
0	No Time-Out error occurred since last clear of this bit.
1	This bit is automatically set when a Time-Out error has been detected.

Bit 2 – PID PID Error

Figure 46-25. Break Transmission



46.6.3.14 Receive Break

The receiver detects a break condition when all data, parity and stop bits are low. This corresponds to detecting a framing error with data to 0x00, but FRAME remains low.

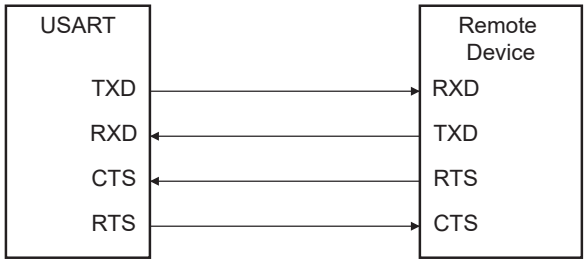
When the low stop bit is detected, the receiver asserts US_CSR.RXBRK. This bit may be cleared by writing a ‘1’ to US_CR.RSTSTA.

An end of receive break is detected by a high level for at least 2/16 of a bit period in Asynchronous operating mode or one sample at high level in Synchronous operating mode. The end of break detection also asserts US_CSR.RXBRK bit.

46.6.3.15 Hardware Handshaking

The USART features a hardware handshaking out-of-band flow control. The RTS and CTS pins are used to connect with the remote device, as shown in the following figure.

Figure 46-26. Connection with a Remote Device for Hardware Handshaking



Setting the USART to operate with hardware handshaking is performed by writing the value 0x2 to US_MR.USART_MODE.

When hardware handshaking is enabled, the USART displays similar behavior as in standard Synchronous or Asynchronous modes, with the difference that the receiver drives the RTS pin and the level on the CTS pin modifies the behavior of the transmitter, as shown in the following figures. The transmitter can handle hardware handshaking in any case.

Figure 46-27. RTS Line Software Control when US_MR.USART_MODE = 2

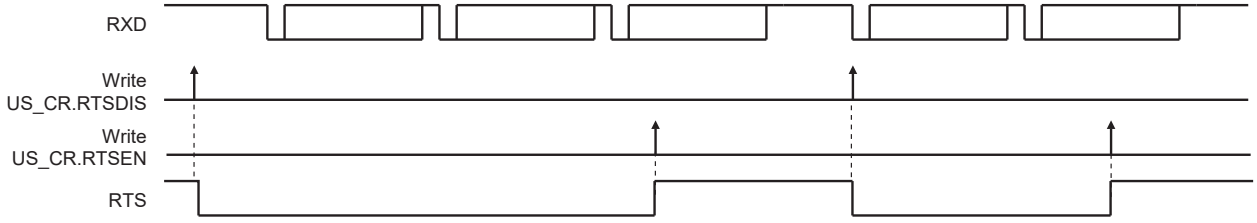
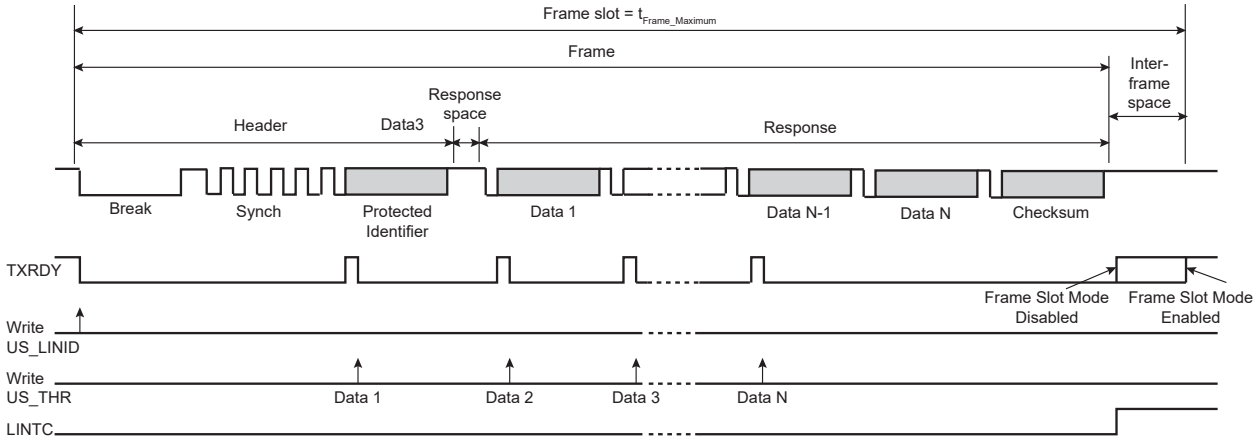


Figure 46-44. Frame Slot Mode



46.6.9.14 LIN Errors

46.6.9.14.1 Bit Error

This error is generated in master of slave node configuration, when the USART is transmitting and if the transmitted value on the Tx line is different from the value sampled on the Rx line. If a bit error is detected, the transmission is aborted at the next byte border.

This error is reported by flag US_CSR.LINBE.

46.6.9.14.2 Inconsistent Synch Field Error

This error is generated in slave node configuration, if the Synch Field character received is other than 0x55.

This error is reported by flag US_CSR.LINISFE.

46.6.9.14.3 Identifier Parity Error

This error is generated in slave node configuration, if the parity of the identifier is wrong. This error can be generated only if the parity feature is enabled (PARDIS = 0).

This error is reported by flag US_CSR.LINIPE.

46.6.9.14.4 Checksum Error

This error is generated in master of slave node configuration, if the received checksum is wrong. This flag can be set to 1 only if the checksum feature is enabled (CHKDIS = 0).

This error is reported by flag US_CSR.LINCE.

46.6.9.14.5 Slave Not Responding Error

This error is generated in master of slave node configuration, when the USART expects a response from another node (NACT = SUBSCRIBE) but no valid message appears on the bus within the time given by the maximum length of the message frame, $t_{Frame\_Maximum}$ (see Frame Slot Mode). This error is disabled if the USART does not expect any message (NACT = PUBLISH or NACT = IGNORE).

This error is reported by flag US_CSR.LINSNRE.

46.6.9.14.6 Synch Tolerance Error

This error is generated in slave node configuration if, after the clock synchronization procedure, it appears that the computed baudrate deviation compared to the initial baudrate is superior to the maximum tolerance FTol_Unsynch (±15%).

This error is reported by flag US_CSR.LINSTE.

46.7.6 USART Interrupt Enable Register (SPI_MODE)

Name: US_IER (SPI_MODE)
Offset: 0x0008
Property: Write-only

This configuration is relevant only if USART_MODE = 0xE or 0xF in the USART Mode Register.

The following configuration values are valid for all listed bit names of this register:

0: No effect

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset					NSSE			

Bit	15	14	13	12	11	10	9	8
Access								
Reset						UNRE	TXEMPTY	

Bit	7	6	5	4	3	2	1	0
Access								
Reset			OVRE				TXRDY	RXRDY

Bit 19 – NSSE NSS Line (Driving CTS Pin) Rising or Falling Edge Event Interrupt Enable

Bit 10 – UNRE SPI Underrun Error Interrupt Enable

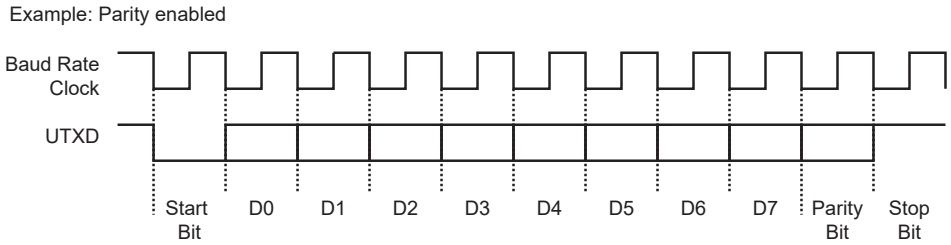
Bit 9 – TXEMPTY TXEMPTY Interrupt Enable

Bit 5 – OVRE Overrun Error Interrupt Enable

Bit 1 – TXRDY TXRDY Interrupt Enable

Bit 0 – RXRDY RXRDY Interrupt Enable

Figure 47-9. Character Transmission

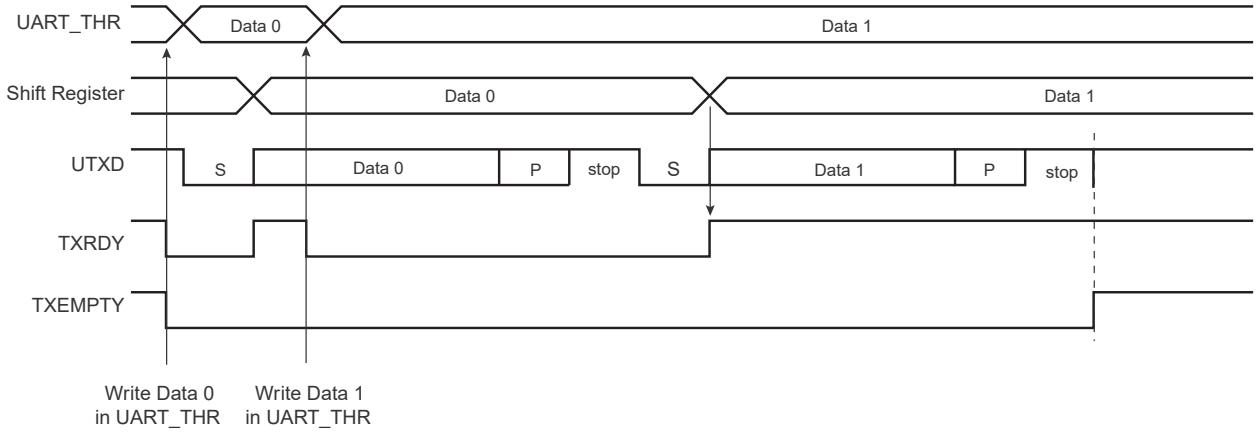


47.5.3.3 Transmitter Control

When the transmitter is enabled, the bit TXRDY (Transmitter Ready) is set in UART_SR. The transmission starts when the programmer writes in the UART_THR, and after the written character is transferred from UART_THR to the internal shift register. The TXRDY bit remains high until a second character is written in UART_THR. As soon as the first character is completed, the last character written in UART_THR is transferred into the internal shift register and TXRDY rises again, showing that the holding register is empty.

When both the internal shift register and UART_THR are empty, i.e., all the characters written in UART_THR have been processed, the TXEMPTY bit rises after the last stop bit has been completed.

Figure 47-10. Transmitter Control



47.5.4 DMA Support

Both the receiver and the transmitter of the UART are connected to a DMA Controller (DMAC) channel.

The DMA Controller channels are programmed via registers that are mapped within the DMAC user interface.

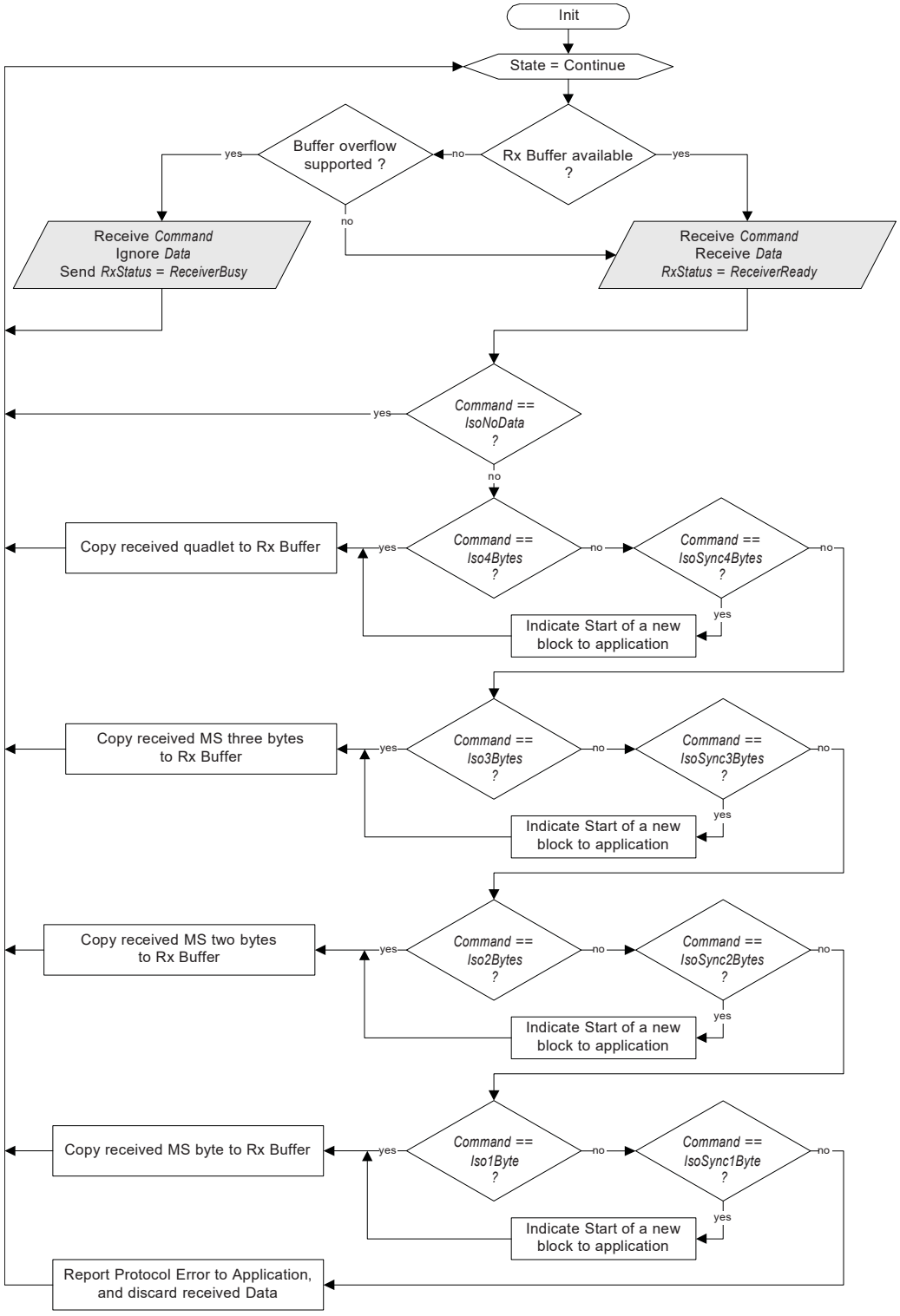
47.5.5 Comparison Function on Received Character

When a comparison is performed on a received character, the result of the comparison is reported on the CMP flag in UART_SR when UART_RHR is loaded with the new received character. The CMP flag is cleared by writing a one to the RSTSTA bit in UART_CR.

UART_CMPR (see UART Comparison Register) can be programmed to provide different comparison methods. These are listed below:

- If VAL1 equals VAL2, then the comparison is performed on a single value and the flag is set to 1 if the received character equals VAL1.
- If VAL1 is strictly lower than VAL2, then any value between VAL1 and VAL2 sets the CMP flag.

Figure 48-15. Isochronous Data Rx Device Protocol



48.6.2 Compliance

The MediaLB specification is targeted towards many levels of chip complexity and native intelligence. Therefore, different levels of implementation are allowed to support MediaLB and still remain compliant to this specification. The Physical Layer portion of this specification must be met by all Devices for

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
96	RSTS[4]	WSTS[4]	rsvd		BD[11:0]											
112	Reserved		BA[13:0]													

Table 48-19. Asynchronous/Control CDT Entry Field Definitions

Field	Description	Details	Accessibility
BA	Buffer Base Address	- BA can start at any byte in the 16k DBR	r,w
BD	Buffer Depth	- BD = size of buffer in bytes - 1 - Buffer end address = BA + BD - BD ≥ max packet length - 1	r,w
RPC	Read Packet Count	- Software initializes to zero, hardware updates - Used in conjunction with WPC, RPTR and WPTR to determine if the buffer is empty or full	r,w,u (1)
WPC	Write Packet Count	- Software initializes to zero, hardware updates - Used in conjunction with RPC, RPTR and WPTR to determine if the buffer is empty or full	r,w,u (1)
RPTR	Read Pointer	- Software initializes to zero, hardware updates - Counts the read address offset within a buffer - DMA read address = BA + RPTR	r,w,u (1)
WPTR	Write Pointer	- Software initializes to zero, hardware updates - Counts the write address offset within a buffer - DMA read address = BA + WPTR	r,w,u (1)
RSTS	Read Status	- Software initializes to zero, hardware updates - Status states:(2) x0x00 = idle xx1xx = ReceiverProtocolError response received from Rx Device 1xxxx = ReceiverBreak command received from Rx Device	r,w,u (1)
WSTS	Write Status	- Software initializes to zero, hardware updates - Status states:(2) x0x00 = idle xx1xx = command protocol error detected	r,w,u (1)

Offset	Name	Bit Pos.								
0x2C	DACC_IMR	7:0			EOC1	EOC0			TXRDY1	TXRDY0
		15:8								
		23:16								
		31:24								
0x30	DACC_ISR	7:0			EOC1	EOC0			TXRDY1	TXRDY0
		15:8								
		23:16								
		31:24								
0x34 ... 0x93	Reserved									
0x94	DACC_ACR	7:0					IBCTLCH1[1:0]		IBCTLCH0[1:0]	
		15:8								
		23:16								
		31:24								
0x98 ... 0xE3	Reserved									
0xE4	DACC_WPMR	7:0								WPEN
		15:8	WPKEY[7:0]							
		23:16	WPKEY[15:8]							
		31:24	WPKEY[23:16]							
0xE8	DACC_WPSR	7:0								WPVS
		15:8	WPVSRC[7:0]							
		23:16								
		31:24								

For the other resolution defined by RES, the code C_i is extended to the corresponding resolution.

The table below is a computation example for the above formula, where V_{VREFP} = 3V:

Table 58-33. Input Voltage Values in Single-ended Mode

C_i		Gain		
Signed	**Nonsigned**	**1**	**2**	**4**
-2048	0	0	0.75	1.125
0	2047	1.5	1.5	1.5
2047	4095	3	2.25	1.875

58.8.4.3 Example of LSB Computation

The LSB is relative to the analog scale V_{VREFP}.

The term LSB expresses the quantization step in volts, also used for one AFE code variation.

- Single-ended (SE) (ex: V_{VREFP} = 3.0V)
  - Gain = 1, LSB = (3.0V / 4096) = 732 µV
  - Gain = 2, LSB = (1.5V / 4096) = 366 µV
  - Gain = 4, LSB = (750 mV / 4096) = 183 µV
- Differential (DIFF) (ex: V_{VREFP} = 3.0V)
  - Gain = 0.5, LSB = (6.0V / 4096) = 1465 µV
  - Gain = 1, LSB = (3.0V / 4096) = 732 µV
  - Gain = 2, LSB = (1.5V / 4096) = 366 µV

The data include the AFE performances, as the PGA and AFE core cannot be separated. The temperature and voltage dependency are given as separate parameters.

58.8.4.4 Gain and Offset Errors

For:

- a given gain error: E_G (%)
- a given ideal code (C_i)
- a given offset error: E_O (LSB of 12 bits)

in 12-bit mode, the actual code (C_A) is calculated using the following formula

$$C_A = \left(1 + \frac{E_G}{100}\right) \times (C_i - 2047) + 2047 + E_O$$

For higher resolutions, the code can be extended to the corresponding resolution defined by RES.

58.8.4.4.1 Differential Mode

In Differential mode, the offset is defined when the differential input voltage is zero.

Symbol	VDDIO Supply	1.8V Domain	3.3V Domain	1.8V Domain	3.3V Domain	Unit
	Parameter	Min		Max		
SMC_{18}	NCS low before NWE high	(NWE_SETUP - NCS_RD_SETUP + NWE_PULSE) × t_{CPMCK} - 3.2	(NWE_SETUP - NCS_RD_SETUP + NWE_PULSE) × t_{CPMCK} - 2.2	–	–	ns
HOLD Settings (NWE_HOLD ≠ 0)						
SMC_{19}	NWE High to Data OUT, NBS0/A0 NBS1, A1, A2–A25 change	NWE_HOLD × t_{CPMCK} - 4.6	NWE_HOLD × t_{CPMCK} - 3.9	–	–	ns
SMC_{20}	NWE High to NCS Inactive (1)	(NWE_HOLD - NCS_WR_HOLD) × t_{CPMCK} - 3.9	(NWE_HOLD - NCS_WR_HOLD) × t_{CPMCK} - 3.6	–	–	ns
NO HOLD Settings (NWE_HOLD = 0)						
SMC_{21}	NWE High to Data OUT, NBS0/A0 NBS1, A1, A2–A25, NCS change(1)	2.1	1.5	–	–	ns

Note:
Hold length = total cycle duration - setup duration - pulse duration. “hold length” is for “NCS_WR_HOLD length” or “NWE_HOLD length”

Table 58-63. SMC Write NCS Controlled (WRITE_MODE = 0)

Symbol	VDDIO Supply	1.8V Domain	3.3V Domain	1.8V Domain	3.3V Domain	Unit
	Parameter	Min		Max		
SMC_{22}	Data Out Valid before NCS High	NCS_WR_PULSE × t_{CPMCK} - 2.8	NCS_WR_PULSE × t_{CPMCK} - 3.9	—	—	ns
SMC_{23}	NCS Pulse Width	NCS_WR_PULSE × t_{CPMCK} - 0.9	NCS_WR_PULSE × t_{CPMCK} - 0.2	—	—	ns
SMC_{24}	A0–A22 valid before NCS low	NCS_WR_SETUP × t_{CPMCK} - 4.0	NCS_WR_SETUP × t_{CPMCK} - 4.6	—	—	ns
SMC_{25}	NWE low before NCS high	(NCS_WR_SETUP - NWE_SETUP + NCS pulse) × t_{CPMCK} - 4.6	(NCS_WR_SETUP - NWE_SETUP + NCS pulse) × t_{CPMCK} - 4.6	—	—	ns

59.13.1.5 QSPI Characteristics

Figure 59-17. QSPI Master Mode with (CPOL= NCPHA = 0) or (CPOL= NCPHA= 1)

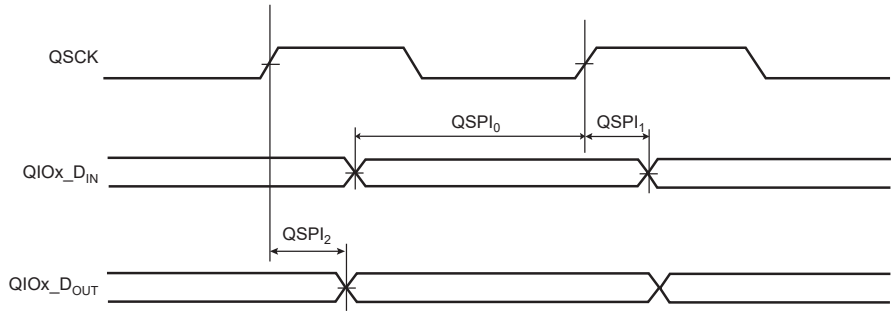
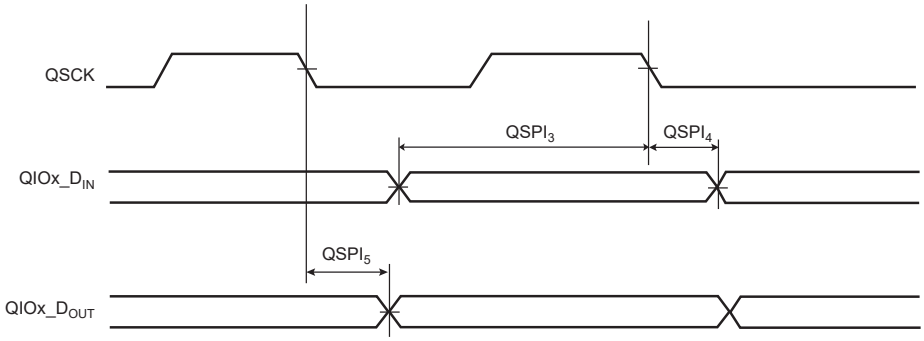


Figure 59-18. QSPI Master Mode with (CPOL = 0 and NCPHA=1) or (CPOL=1 and NCPHA= 0)



59.13.1.5.1 Maximum QSPI Frequency

The following formulas give maximum QSPI frequency in Master read and write modes.

$$f_{\mathrm{QSCK}}\mathrm{max} = \frac{1}{QSPI_0(\mathrm{or}\ QSPI_3) + t_{\mathrm{VALID}}}$$

t_{valid} is the slave time response to output data after detecting a QSCK edge.

For a QSPI slave device with t_{VALID} (or t_V) = 12 ns, f_{QSCK}max = 66 MHz at VDDIO = 3.3V.

For a QSPI Flash memory device with t_{VALID} (or t_V) = 6 ns, the formula returns a value of 112 MHz. In worst case conditions, this exceeds 66 MHz, which is the maximum allowed frequency of the QSPI master. In this case, the limitation is due to the controller and not the slave.

Master Write Mode

The QSPI sends data to a slave device only, e.g. an LCD. The limit is given by $QSPI_2$ (or $QSPI_5$) timing. Since it gives a maximum frequency above the maximum pad speed (see I/O Characteristics), the max QSPI frequency is the one from the pad.

Master Read Mode

59.13.1.5.2 QSPI Timings

Timings are given in the following domains:

- 1.8V domain: VDDIO from 1.7V to 1.95V, maximum external capacitor = 20 pF
- 3.3V domain: VDDIO from 2.85V to 3.6V, maximum external capacitor = 40 pF.

Figure 59-20. SPI Master Mode with (CPOL= NCPHA = 0) or (CPOL= NCPHA= 1)

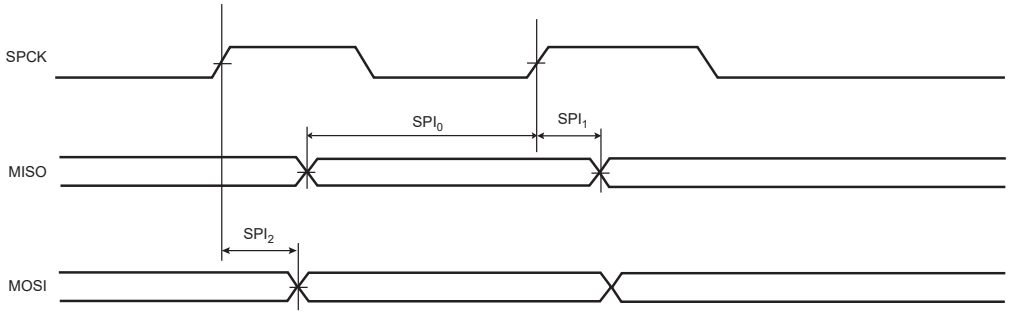


Figure 59-21. SPI Master Mode with (CPOL = 0 and NCPHA=1) or (CPOL=1 and NCPHA= 0)

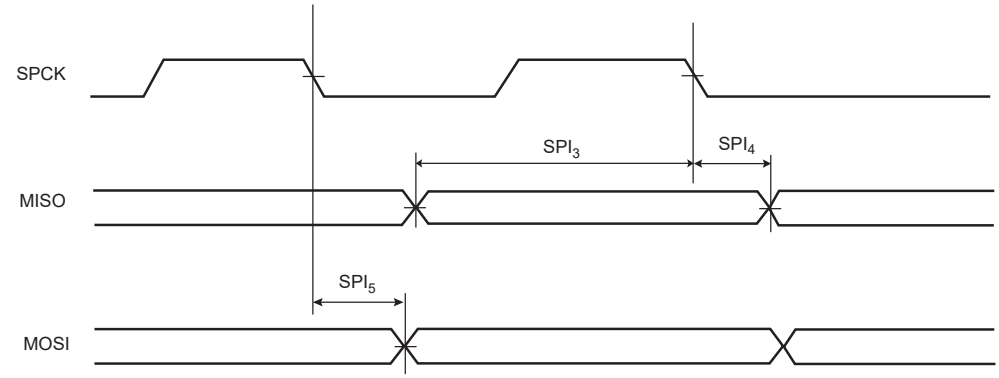


Figure 59-22. SPI Slave Mode with (CPOL=0 and NCPHA=1) or (CPOL=1 and NCPHA=0)

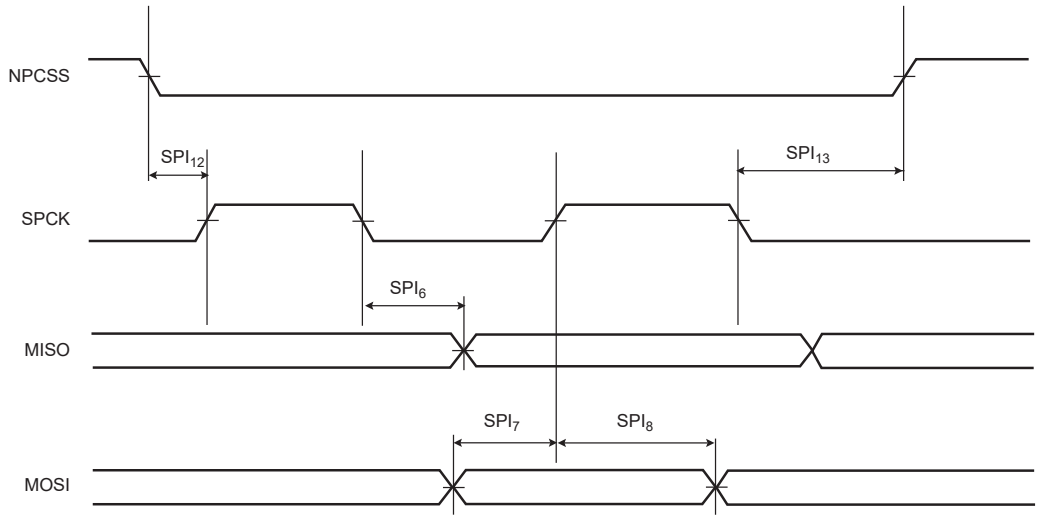
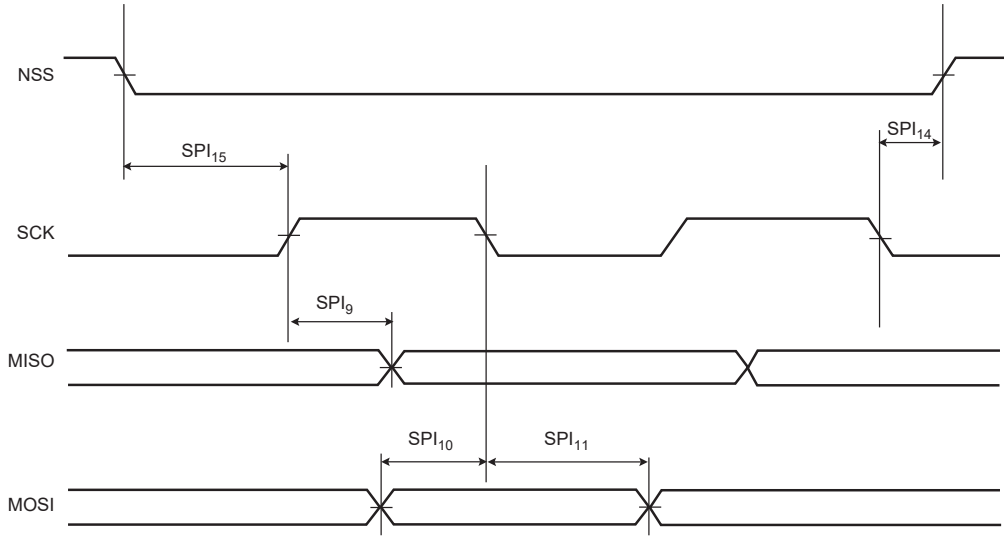


Figure 59-28. USART SPI Slave Mode (Mode 0 or 3)



59.13.1.11.1 USART SPI Timings

Timings are given in the following domains:

- 1.8V domain: VDDIO from 1.7V to 1.95V, maximum external capacitor = 20 pF
- 3.3V domain: VDDIO from 2.85V to 3.6V, maximum external capacitor = 40 pF

Table 59-66. USART SPI Timings

Symbol	Parameter	Conditions	Min	Max	Unit
Master Mode					
SPI_0	SCK Period	1.8V domain 3.3V domain	MCK/6	–	ns
SPI_1	Input Data Setup Time	1.8V domain 3.3V domain	2.8 2.5	–	ns
SPI_2	Input Data Hold Time	1.8V domain 3.3V domain	0.5 0.2	–	ns
SPI_3	Chip Select Active to Serial Clock	1.8V domain 3.3V domain	-1.1 -0.9	–	ns
SPI_4	Output Data Setup Time	1.8V domain 3.3V domain	-1.9 -1.9	10.9 10.4	ns
SPI_5	Serial Clock to Chip Select Inactive	1.8V domain 3.3V domain	-2.4 -2.4	-1.9 -1.9	ns
Slave Mode					
SPI_6	SCK falling to MISO	1.8V domain 3.3V domain	3.6 2.9	16.8 13.9	ns
SPI_7	MOSI Setup time before SCK rises	1.8V domain	2.4	–	ns