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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

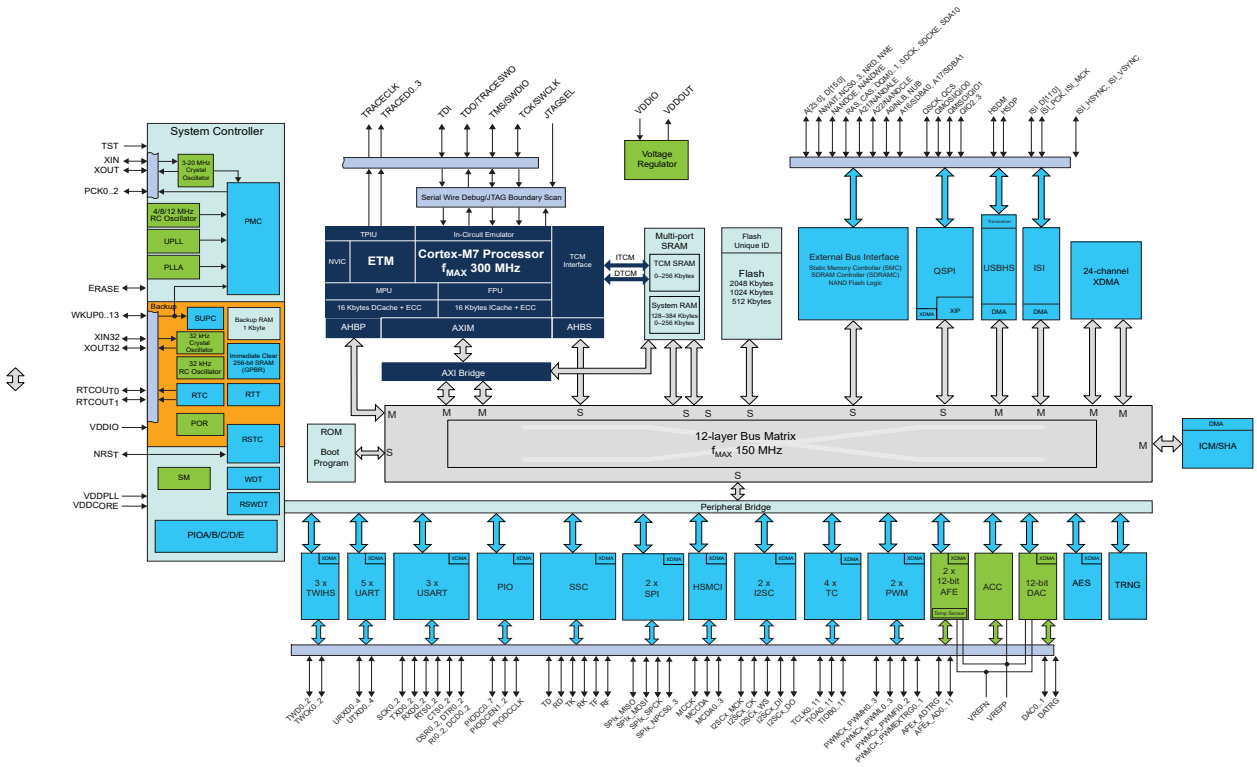
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70q21a-cn

3. Block Diagram

Refer to the table 1. Configuration Summary for detailed configurations of memory size, package and features of the SAM E70/S70/V70/V71 devices.

Figure 3-1. SAM S70 144-pin Block Diagram



All lock regions must be unlocked before the Full Erase command by using the CLB command. Otherwise, the erase command is aborted and no page is erased.

Table 18-8. Full Erase Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	EA
2	Write handshaking	DATA	0

18.3.5.4 Flash Lock Commands

Lock bits can be set using WPL or EWPL commands. They can also be set by using the Set Lock command (SLB). With this command, several lock bits can be activated. A Bit Mask is provided as argument to the command. When bit 0 of the bit mask is set, then the first lock bit is activated.

In the same way, the Clear Lock command (CLB) is used to clear lock bits.

Table 18-9. Set and Clear Lock Bit Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	SLB or CLB
2	Write handshaking	DATA	Bit Mask

Lock bits can be read using Get Lock Bit command (GLB). The n^{th} lock bit is active when the bit n of the bit mask is set.

Table 18-10. Get Lock Bit Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	GLB
2	Read handshaking	DATA	Lock Bit Mask Status 0 = Lock bit is cleared 1 = Lock bit is set

18.3.5.5 Flash General-purpose NVM Commands

General-purpose NVM bits (GP NVM bits) can be set using the Set GPNVM command (SGPB). This command also activates GP NVM bits. A bit mask is provided as argument to the command. When bit 0 of the bit mask is set, then the first GP NVM bit is activated.

In the same way, the Clear GPNVM command (CGPB) is used to clear general-purpose NVM bits. The general-purpose NVM bit is deactivated when the corresponding bit in the pattern value is set to 1.

Table 18-11. Set/Clear GP NVM Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	SGPB or CGPB
2	Write handshaking	DATA	GP NVM bit pattern value

General-purpose NVM bits can be read using the Get GPNVM Bit command (GGPB). The n^{th} GP NVM bit is active when bit n of the bit mask is set.

Value	Description
0	Flash ready does not generate an interrupt.
1	Flash ready (to accept a new command) generates an interrupt.

31.20.15 PMC Interrupt Disable Register

Name: PMC_IDR
Offset: 0x0064
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			XT32KERR			CFDEV	MOSCRCS	MOSCSELS
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
		PCKRDY6	PCKRDY5	PCKRDY4	PCKRDY3	PCKRDY2	PCKRDY1	PCKRDY0
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		LOCKU			MCKRDY		LOCKA	MOSCXTS
Access								
Reset								

Bit 21 – XT32KERR 32.768 kHz Crystal Oscillator Error Interrupt Disable

Bit 18 – CFDEV Clock Failure Detector Event Interrupt Disable

Bit 17 – MOSCRCS Main RC Status Interrupt Disable

Bit 16 – MOSCSELS Main Clock Source Oscillator Selection Status Interrupt Disable

Bits 8, 9, 10, 11, 12, 13, 14 – PCKRDY Programmable Clock Ready x Interrupt Disable

Bit 6 – LOCKU UTMI PLL Lock Interrupt Disable

Bit 3 – MCKRDY Master Clock Ready Interrupt Disable

Bit 1 – LOCKA PLLA Lock Interrupt Disable

Bit 0 – MOSCXTS Main Crystal Oscillator Status Interrupt Disable

34.7.6 SDRAMC Interrupt Disable Register

Name: SDRAMC_IDR
Offset: 0x18
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								W
Reset								RES

Bit 0 – RES Refresh Error Interrupt Disable

Value	Description
0	No effect.
1	Disables the refresh error interrupt.

38.8.11 GMAC Interrupt Enable Register

Name: GMAC_IER
Offset: 0x028
Reset: –
Property: Write-only

This register is write-only and will always return zero.

The following values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
Access			W	W	R	W	W	W
Reset			–	–	–	–	–	–

Bit	23	22	21	20	19	18	17	16
	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
Access	W	W	W	W	W	W		
Reset	–	–	–	–	–	–		

Bit	15	14	13	12	11	10	9	8
	EXINT	PFTR	PTZ	PFNZ	HRESP	ROVR		
Access	W	W	W	W	W	W		
Reset	–	–	–	–	–	–		

Bit	7	6	5	4	3	2	1	0
	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bit 29 – TSUTIMCMP TSU Timer Comparison

Bit 28 – WOL Wake On LAN

Bit 27 – RXLPISBC Receive LPI indication Status Bit Change
Receive LPI indication status bit change.

Cleared on read.

Bit 26 – SRI TSU Seconds Register Increment

Bit 25 – PDRSFT PDelay Response Frame Transmitted

Bit 24 – PDRQFT PDelay Request Frame Transmitted

Bit 23 – PDRSFR PDelay Response Frame Received

38.8.68 GMAC 512 to 1023 Byte Frames Received Register

Name: GMAC_TBFR1023
Offset: 0x178
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	NFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFRX[31:0] 512 to 1023 Byte Frames Received without Error
This bit field counts the number of 512 to 1023 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

Bit 5 – EORSM End of Resume Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.EORSMC bit is written to one to acknowledge the interrupt.
1	Set when the USBHS detects a valid “End of Resume” signal initiated by the host. This triggers a USB interrupt if USBHS_DEVIMR.EORSME = 1.

Bit 4 – WAKEUP Wakeup Interrupt
This interrupt is generated even if the clock is frozen by the USBHS_CTRL.FRZCLK bit.

Value	Description
0	Cleared when the USBHS_DEVICR.WAKEUPC bit is written to one to acknowledge the interrupt (USB clock inputs must be enabled before), or when the Suspend (SUSP) interrupt bit is set.
1	Set when the USBHS is reactivated by a filtered non-idle signal from the lines (not by an upstream resume). This triggers an interrupt if USBHS_DEVIMR.WAKEUPE = 1.

Bit 3 – EORST End of Reset Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.EORSTC bit is written to one to acknowledge the interrupt.
1	Set when a USB “End of Reset” has been detected. This triggers a USB interrupt if USBHS_DEVIMR.EORSTE = 1.

Bit 2 – SOF Start of Frame Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.SOFC bit is written to one to acknowledge the interrupt.
1	Set when a USB “Start of Frame” PID (SOF) has been detected (every 1 ms). This triggers a USB interrupt if SOFE = 1. The FNUM field is updated. In High-speed mode, the MFNUM field is cleared.

Bit 1 – MSOF Micro Start of Frame Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.MSOFC bit is written to one to acknowledge the interrupt.
1	Set in High-speed mode when a USB “Micro Start of Frame” PID (SOF) has been detected (every 125 µs). This triggers a USB interrupt if MSOFE = 1. The MFNUM field is updated. The FNUM field is unchanged.

Bit 0 – SUSP Suspend Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.SUSPC bit is written to one to acknowledge the interrupt, or when the Wakeup (WAKEUP) interrupt bit is set.
1	Set when a USB “Suspend” idle bus state has been detected for 3 frame periods (J state for 3 ms). This triggers a USB interrupt if USBHS_DEVIMR.SUSPE = 1.

Value	Description
	USBHS_DEVEPTIMRx) but not the endpoint configuration (USBHS_DEVEPTCFGx.ALLOC, USBHS_DEVEPTCFGx.EPBK, USBHS_DEVEPTCFGx.EPSIZE, USBHS_DEVEPTCFGx.EPDIR, USBHS_DEVEPTCFGx.EPTYPE).
1	Endpoint x is enabled.

Value	Description
0	Cleared when USBHS_HSTPIPICR.SHORTPACKETIC = 1.
1	Set when a short packet is received by the host controller (packet length inferior to the PSIZE programmed field).

Bit 6 – CRCERRI CRC Error Interrupt

Value	Description
0	Cleared when USBHS_HSTPIPICR.CRCERRIC = 1.
1	Set when a CRC error occurs on the current bank of the pipe. This triggers an interrupt if the USBHS_HSTPIPIMR.TXSTPE bit = 1.

Bit 5 – OVERFI Overflow Interrupt

Value	Description
0	Cleared when USBHS_HSTPIPICR.OVERFIC = 1.
1	Set when the current pipe has received more data than the maximum length of the current pipe. An interrupt is triggered if the USBHS_HSTPIPIMR.OVERFIE bit = 1.

Bit 4 – NAKEDI NAKed Interrupt

Value	Description
0	Cleared when USBHS_HSTPIPICR.NAKEDIC = 1.
1	Set when a NAK has been received on the current bank of the pipe. This triggers an interrupt if the USBHS_HSTPIPIMR.NAKEDE bit = 1.

Bit 3 – PERRI Pipe Error Interrupt

Value	Description
0	Cleared when the error source bit is cleared.
1	Set when an error occurs on the current bank of the pipe. This triggers an interrupt if the USBHS_HSTPIPIMR.PERRE bit is set. Refer to the USBHS_HSTPIPERRx register to determine the source of the error.

Bit 2 – UNDERFI Underflow Interrupt
This bit is set, for an isochronous and interrupt IN/OUT pipe, when an error flow occurs. This triggers an interrupt if the UNDERFIE bit = 1.

This bit is set, for an isochronous or interrupt OUT pipe, when a transaction underflow occurs in the current pipe (the pipe cannot send the OUT data packet in time because the current bank is not ready). A zero-length-packet (ZLP) is sent instead.

This bit is set, for an isochronous or interrupt IN pipe, when a transaction flow error occurs in the current pipe, i.e, the current bank of the pipe is not free while a new IN USB packet is received. This packet is not stored in the bank. For an interrupt pipe, the overflowed packet is ACKed to comply with the USB standard.

This bit is cleared when USBHS_HSTPIPICR.UNDERFIEC = 1.

Bit 1 – TXOUTI Transmitted OUT Data Interrupt

41.8.11 SPI Write Protection Status Register

Name: SPI_WPSR
Offset: 0xE8
Reset: 0x0
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	WPVSRC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
								WPVS
Access								R
Reset								0

Bits 15:8 – WPVSRC[7:0] Write Protection Violation Source
When WPVS = 1, WPVSRC indicates the register address offset at which a write access has been attempted.

Bit 0 – WPVS Write Protection Violation Status

Value	Description
0	No write protection violation has occurred since the last read of SPI_WPSR.
1	A write protection violation has occurred since the last read of SPI_WPSR. If this violation is an unauthorized attempt to write a protected register, the associated violation is reported into field WPVSRC.

43.7.4 TWIHS Internal Address Register

Name: TWIHS_IADR
Offset: 0x0C
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	IADR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	IADR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IADR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – IADR[23:0] Internal Address
0, 1, 2 or 3 bytes depending on IADRSZ.

NACT(slave1)=PUBLISH

NACT(slave2)=SUBSCRIBE

- Data transfer from the slave2 to the master and to the slave1:

NACT(master)=SUBSCRIBE

NACT(slave1)=SUBSCRIBE

NACT(slave2)=PUBLISH

46.6.9.11 Response Data Length

The LIN response data length is the number of data fields (bytes) of the response excluding the checksum.

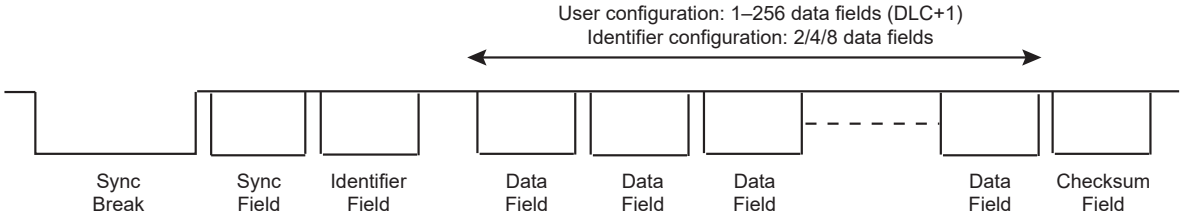
The response data length can either be configured by the user or be defined automatically by bits 4 and 5 of the Identifier (compatibility to LIN Specification 1.1). The user can choose between these two modes using the US_LINMR.DLM:

- DLM = 0: The response data length is configured by the user via US_LINMR.DLC. The response data length is equal to (DLC + 1) bytes. DLC can be programmed from 0 to 255, so the response can contain from 1 data byte up to 256 data bytes.
- DLM = 1: The response data length is defined by the Identifier (US_LINIR.IDCHR) according to the table below. The US_LINMR.DLC is discarded. The response can contain 2 or 4 or 8 data bytes.

Table 46-13. Response Data Length if DLM = 1

IDCHR[5]	IDCHR[4]	Response Data Length [Bytes]
0	0	2
0	1	2
1	0	4
1	1	8

Figure 46-43. Response Data Length



46.6.9.12 Checksum

The last field of a frame is the checksum. The checksum contains the inverted 8-bit sum with carry, over all data bytes or all data bytes and the protected identifier. Checksum calculation over the data bytes only is called classic checksum and it is used for communication with LIN 1.3 slaves. Checksum calculation over the data bytes and the protected identifier byte is called enhanced checksum and it is used for communication with LIN 2.0 slaves.

The USART can be configured to:

- Send/Check an Enhanced checksum automatically (CHKDIS = 0 & CHKTYP = 0)
- Send/Check a Classic checksum automatically (CHKDIS = 0 & CHKTYP = 1)

46.7.4 USART Mode Register (SPI_MODE)

Name: US_MR (SPI_MODE)
Offset: 0x0004
Reset: 0x0
Property: Read/Write

This configuration is relevant only if USART_MODE = 0xE or 0xF in the USART Mode Register.

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

– Applicable if USART operates in SPI mode (USART_MODE = 0xE or 0xF):

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
				WRDBT		CLKO		CPOL
Access								
Reset				0		0		0

Bit	15	14	13	12	11	10	9	8
								CPHA
Access								
Reset								0

Bit	7	6	5	4	3	2	1	0
	CHRL[1:0]		USCLKS[1:0]		USART_MODE[3:0]			
Access								
Reset	0	0	0	0	0	0	0	0

Bit 20 – WRDBT Wait Read Data Before Transfer

Value	Description
0	The character transmission starts as soon as a character is written into US_THR (assuming TXRDY was set).
1	The character transmission starts when a character is written and only if RXRDY flag is cleared (Receive Holding Register has been read).

Bit 18 – CLKO Clock Output Select

Value	Description
0	The USART does not drive the SCK pin.
1	The USART drives the SCK pin if USCLKS does not select the external clock SCK.

Bit 16 – CPOL SPI Clock Polarity
Applicable if USART operates in SPI mode (Slave or Master, USART_MODE = 0xE or 0xF):

CPOL is used to determine the inactive state value of the serial clock (SCK). It is used with CPHA to produce the required clock/data relationship between master and slave devices.

Bit 6 – LSFE LON Short Frame Error Interrupt Mask

Bit 5 – OVRE Overrun Error Interrupt Mask

Bit 1 – TXRDY TXRDY Interrupt Mask

Bit 0 – RXRDY RXRDY Interrupt Mask

48.7.28 AHB Channel Mask 0 Register

Name: MLB_ACMR0
Offset: 0x3D8
Reset: 0x00000000
Property: Read/Write

Using the AHB Channel Mask (ACMRn) register, the HC can control which channel(s) generate interrupts on ahb_int[1:0]. All ACMRn register bits default as ‘0’ (“masked”); therefore, the HC must initially write ACMRn to enable interrupts. Each bit of ACMRn is read/write accessible.

Bit	31	30	29	28	27	26	25	24
	CHM[31:24]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CHM[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CHM[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CHM[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CHM[31:0] Bitwise Channel Mask Bits 31 to 0
CHM[n] = 1 indicates that channel n can generate an interrupt.

51.7.25 PWM Fault Status Register

Name: PWM_FSR
Offset: 0x60
Reset: 0x00000000
Property: Read-only

Refer to Fault Inputs for details on fault generation.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	FS[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FIV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – FS[7:0] Fault Status
For each bit y of FS, where y is the fault input number:

0: The fault y is not currently active.

1: The fault y is currently active.

Bits 7:0 – FIV[7:0] Fault Input Value
For each bit y of FIV, where y is the fault input number:

0: The current sampled value of the fault input y is 0 (after filtering if enabled).

1: The current sampled value of the fault input y is 1 (after filtering if enabled).

55.5.2.3 ICM Region Control Structure Member

Name: ICM_RCTRL
Property: Read/Write

Register offset is calculated as ICM_DSCR+0x008+RID*(0x10).

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TRSIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	TRSIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 15:0 – TRSIZE[15:0] Transfer Size for the Current Chunk of Data
ICM performs a transfer of (TRSIZE + 1) blocks of 512 bits.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Settling Time	Overdrive > 100 mV (ACC_ACR.ISEL = 0)	–	–	1.5	µs
		Overdrive > 100 mV (ACC_ACR.ISEL = 1)	–	–	0.15	

59.10 Temperature Sensor

The temperature sensor is connected to channel 11 of the AFE0.

The temperature sensor provides an output voltage (V_{TEMP}) that is proportional to absolute temperature (PTAT).

Improvement of the raw performance of the temperature sensor acquisition can be achieved by performing a single temperature point calibration to remove the initial inaccuracies (V_{TEMP} and ADC offsets).

Table 59-42. Temperature Sensor Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{TEMP}	Output Voltage via AD11	T_A = 25°C	0.64	0.72	0.8	V
dV_{TEMP}/dT	Temperature Sensitivity (Slope Voltage versus Temperature)	–	2.06	2.33	2.60	mV/°C
t_S	VTEMP Settling Time	When V_{TEMP} is sampled by the AFEC, the required track-and-hold time to ensure 1°C accurate settling	–	–	1	µs
–	Temperature Accuracy	After offset calibration over T_A range [-40°C : +105°C]	-10	–	10	°C
t_{START}	Startup Time	–	–	–	30	µs
I_{VDDIN}	Current Consumption	–	–	130	270	µA

Note: AFE Gain Error and Offset error considered calibrated. This calibration at ambient temperature is not a feature of the product and is performed by the user's application.

59.11 12-bit DAC Characteristics

Table 59-43. Analog Power Supply Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VDDIN}	Current Consumption	Sleep mode (Clock OFF)	–	10	–	µA
		Normal mode with one output on, DACC_ACR.IBCTLCHx =3 (see **Note 1**) FS = 1 MSps, no R_{LOAD}, V_{DDIN} = 3.3V	–	200	800	

Signal Name	Recommended Pin Connection	Description
		WARNING Power up and power down sequences given in the "Power Considerations" chapter must be respected.
VDDIO	Decoupling/filtering capacitors (100 nF) (1, 2)	Powers the Peripheral I/O lines (Input/Output Buffers), backup part, 1 Kbytes of Backup SRAM, 32 kHz crystal oscillator, oscillator pads Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop. Supply ripple must not exceed 30 mVrms for 10 kHz to 10 MHz range. **WARNING** VDDIN and VDDIO must have the same level and must always be higher than VDDCORE. **WARNING** Powerup and powerdown sequences given in the "Power Considerations" chapter must be respected.
VDDUTMII	Decoupling capacitor (100 nF) (1) (2)	Powers the USB transceiver interface. Must be connected to VDDIO. For USB operations, VDDUTMII and VDDIO voltage ranges must be from 3.0V to 3.6V. Must always be connected even if the USB is not used. Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop. Supply ripple must not exceed 20 mVrms for 10 kHz to 10 MHz range.
VDDPLLUSB	Decoupling/filtering RLC circuit (1)	Powers the UTMI PLL and the 3 to 20 MHz oscillator. For USB operations, VDDPLLUSB should be between 3.0V and 3.6V. The VDDPLLUSB power supply pin draws small current, but it is noise sensitive. Care must be taken in VDDPLLUSB power supply routing, decoupling and also on bypass capacitors. Supply ripple must not exceed 10 mVrms for 10 kHz to 10 MHz range.
VDDOUT	Left unconnected	Voltage Regulator Output
VDDCORE	Decoupling capacitor (100 nF) (1) (2)	Powers the core, embedded memories and peripherals.