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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70q21a-cnt

Value	Description
0	Flash ready does not generate an interrupt.
1	Flash ready (to accept a new command) generates an interrupt.

Bit 17 – CXFR_DONE Codec DMA Transfer Done Interrupt Disable

Value	Description
0	No effect.
1	Disables the corresponding interrupt.

Bit 16 – PXFR_DONE Preview DMA Transfer Done Interrupt Disable

Value	Description
0	No effect.
1	Disables the corresponding interrupt.

Bit 10 – VSYNC Vertical Synchronization Interrupt Disable

Value	Description
0	No effect.
1	Disables the corresponding interrupt.

Bit 2 – SRST Software Reset Interrupt Disable

Value	Description
0	No effect.
1	Disables the corresponding interrupt.

Bit 1 – DIS_DONE Disable Done Interrupt Disable

Value	Description
0	No effect.
1	Disables the corresponding interrupt.

Offset	Name	Bit Pos.								
		23:16					PEPNUM[3:0]			
		31:24	INTFRQ[7:0]							
0x050C	USBHS_HSTPIPCFG3 (HSBOHSCP)	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16				PINGEN	PEPNUM[3:0]			
		31:24	BINTERVAL[7:0]							
0x0510	USBHS_HSTPIPCFG4	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16					PEPNUM[3:0]			
		31:24	INTFRQ[7:0]							
0x0510	USBHS_HSTPIPCFG4 (HSBOHSCP)	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16				PINGEN	PEPNUM[3:0]			
		31:24	BINTERVAL[7:0]							
0x0514	USBHS_HSTPIPCFG5	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16					PEPNUM[3:0]			
		31:24	INTFRQ[7:0]							
0x0514	USBHS_HSTPIPCFG5 (HSBOHSCP)	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16				PINGEN	PEPNUM[3:0]			
		31:24	BINTERVAL[7:0]							
0x0518	USBHS_HSTPIPCFG6	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16					PEPNUM[3:0]			
		31:24	INTFRQ[7:0]							
0x0518	USBHS_HSTPIPCFG6 (HSBOHSCP)	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16				PINGEN	PEPNUM[3:0]			
		31:24	BINTERVAL[7:0]							
0x051C	USBHS_HSTPIPCFG7	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16					PEPNUM[3:0]			
		31:24	INTFRQ[7:0]							
0x051C	USBHS_HSTPIPCFG7 (HSBOHSCP)	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16				PINGEN	PEPNUM[3:0]			
		31:24	BINTERVAL[7:0]							
0x0520	USBHS_HSTPIPCFG8	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16					PEPNUM[3:0]			
		31:24	INTFRQ[7:0]							
0x0520	USBHS_HSTPIPCFG8 (HSBOHSCP)	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16				PINGEN	PEPNUM[3:0]			
		31:24	BINTERVAL[7:0]							

The bank is really killed: USBHS_DEVEPTISRx.NBUSYBK is decremented.

The bank is not cleared but sent (IN transfer): USBHS_DEVEPTISRx.NBUSYBK is decremented.

The bank is not cleared because it was empty.

The user should wait for this bit to be cleared before trying to kill another packet.

This kill request is refused if at the same time an IN token is coming and the last bank is the current one being sent on the USB line. If at least two banks are ready to be sent, there is no problem to kill a packet even if an IN token is coming. Indeed, in this case, the current bank is sent (IN transfer) while the last bank is killed.

Bit 12 – NBUSYBKE Number of Busy Banks Interrupt

Value	Description
0	Cleared when USBHS_DEVEPTIDRx.NBUSYBKEC = 0. This disables the Number of Busy Banks interrupt (USBHS_DEVEPTISRx.NBUSYBK).
1	Set when the USBHS_DEVEPTIERx.NBUSYBKES = 1. This enables the Number of Busy Banks interrupt (USBHS_DEVEPTISRx.NBUSYBK).

Bit 7 – SHORTPACKETE Short Packet Interrupt
If this bit is set for non-control IN endpoints, a short packet transmission is guaranteed upon ending a DMA transfer, thus signaling an end of isochronous frame or a bulk or interrupt end of transfer, provided that the End of DMA Buffer Output Enable (END_B_EN) bit and the Automatic Switch (AUTOSW) = 1.

Value	Description
0	Cleared when USBHS_DEVEPTIDRx.SHORTPACKETEC = 1. This disables the Short Packet interrupt (USBHS_DEVEPTISRx.SHORTPACKET).
1	Set when USBHS_DEVEPTIERx.SHORTPACKETES = 1. This enables the Short Packet interrupt (USBHS_DEVEPTISRx.SHORTPACKET).

Bit 6 – STALLEDE STALLed Interrupt

Value	Description
0	Cleared when USBHS_DEVEPTIDRx.STALLEDEC = 1. This disables the STALLed interrupt (USBHS_DEVEPTISRx.STALLEDI).
1	Set when USBHS_DEVEPTIERx.STALLEDES = 1. This enables the STALLed interrupt (USBHS_DEVEPTISRx.STALLEDI).

Bit 5 – OVERFE Overflow Interrupt

Value	Description
0	Cleared when USBHS_DEVEPTIDRx.OVERFEC = 1. This disables the Overflow interrupt (USBHS_DEVEPTISRx.OVERFI).
1	Set when USBHS_DEVEPTIERx.OVERFES = 1. This enables the Overflow interrupt (USBHS_DEVEPTISRx.OVERFI).

Bit 4 – NAKINE NAKed IN Interrupt

Bit 7 – SHORTPACKETEC Shortpacket Interrupt Clear

Bit 6 – CRCERREC CRC Error Interrupt Clear

Bit 5 – OVERFEC Overflow Interrupt Clear

Bit 4 – HBISOFLUSHEC High Bandwidth Isochronous IN Flush Interrupt Clear

Bit 3 – HBISOINERREC High Bandwidth Isochronous IN Error Interrupt Clear

Bit 2 – UNDERFEC Underflow Interrupt Clear

Bit 1 – RXOUTEC Received OUT Data Interrupt Clear

Bit 0 – TXINEC Transmitted IN Interrupt Clear

Bit 5 – HSOFI Host Start of Frame Interrupt

Value	Description
0	Cleared when USBHS_HSTICR.HSOFIC = 1.
1	Set when a SOF is issued by the host controller. This triggers a USB interrupt when HSOFE = 1. When using the host controller in Low-speed mode, this bit is also set when a keep-alive is sent.

Bit 4 – RXRSMI Upstream Resume Received Interrupt

Value	Description
0	Cleared when USBHS_HSTICR.RXRSMIC = 1.
1	Set when an Upstream Resume has been received from the device.

Bit 3 – RSMEDI Downstream Resume Sent Interrupt

Value	Description
0	Cleared when USBHS_HSTICR.RSMEDIC = 1.
1	Set when a Downstream Resume has been sent to the device.

Bit 2 – RSTI USB Reset Sent Interrupt

Value	Description
0	Cleared when USBHS_HSTICR.RSTIC = 1.
1	Set when a USB Reset has been sent to the device.

Bit 1 – DDISCI Device Disconnection Interrupt

Value	Description
0	Cleared when USBHS_HSTICR.DDISCIC = 1.
1	Set when the device has been removed from the USB bus.

Bit 0 – DCONNI Device Connection Interrupt

Value	Description
0	Cleared when USBHS_HSTICR.DCONNIC = 1.
1	Set when a new device has been connected to the USB bus.

Value	Description
0	Cleared when USBHS_HSTPIPICR.TXOUTIC = 1.
1	Set when the current OUT bank is free and can be filled. This triggers an interrupt if USBHS_HSTPIPIMR.TXOUTE = 1.

Bit 0 – RXINI Received IN Data Interrupt

Value	Description
0	Cleared when USBHS_HSTPIPICR.RXINIC = 1.
1	Set when a new USB message is stored in the current bank of the pipe. This triggers an interrupt if the USBHS_HSTPIPIMR.RXINE bit = 1.

39.6.61 Host Pipe x Enable Register (Interrupt Pipes)

Name: USBHS_HSTPIPIERx (INTPIPES)
Offset: 0x05F0 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

This register view is relevant only if PTYPE = 0x3 in "Host Pipe x Configuration Register".

For additional information, see "Host Pipe x Mask Register (Interrupt Pipes)".

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Sets the corresponding bit in USBHS_HSTPIPIMRx.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
						RSTDTS	PFREEZES	PDISHDMAS
Access								
Reset						0	0	0

Bit	15	14	13	12	11	10	9	8
				NBUSYBKES				
Access								
Reset				0				

Bit	7	6	5	4	3	2	1	0
	SHORTPACKETIES	RXSTALLDES	OVERFIES	NAKEDES	PERRES	UNDERFIES	TXOUTES	RXINES
Access								
Reset	0	0	0	0	0	0	0	0

Bit 18 – RSTDTS Reset Data Toggle Enable

Bit 17 – PFREEZES Pipe Freeze Enable

Bit 16 – PDISHDMAS Pipe Interrupts Disable HDMA Request Enable

Bit 12 – NBUSYBKES Number of Busy Banks Enable

Bit 7 – SHORTPACKETIES Short Packet Interrupt Enable

Bit 6 – RXSTALLDES Received STALLed Interrupt Enable

41.8.10 SPI Write Protection Mode Register

Name: SPI_WPMR
Offset: 0xE4
Reset: 0x0
Property: Read/Write

See section Register Write Protection for the list of registers that can be write-protected.

Bit	31	30	29	28	27	26	25	24
	WPKEY[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	WPKEY[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	WPKEY[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
						WPCREN	WPITEN	WPEN
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 31:8 – WPKEY[23:0] Write Protection Key

Value	Name	Description
0x535049	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

Bit 2 – WPCREN Write Protection Control Register Enable

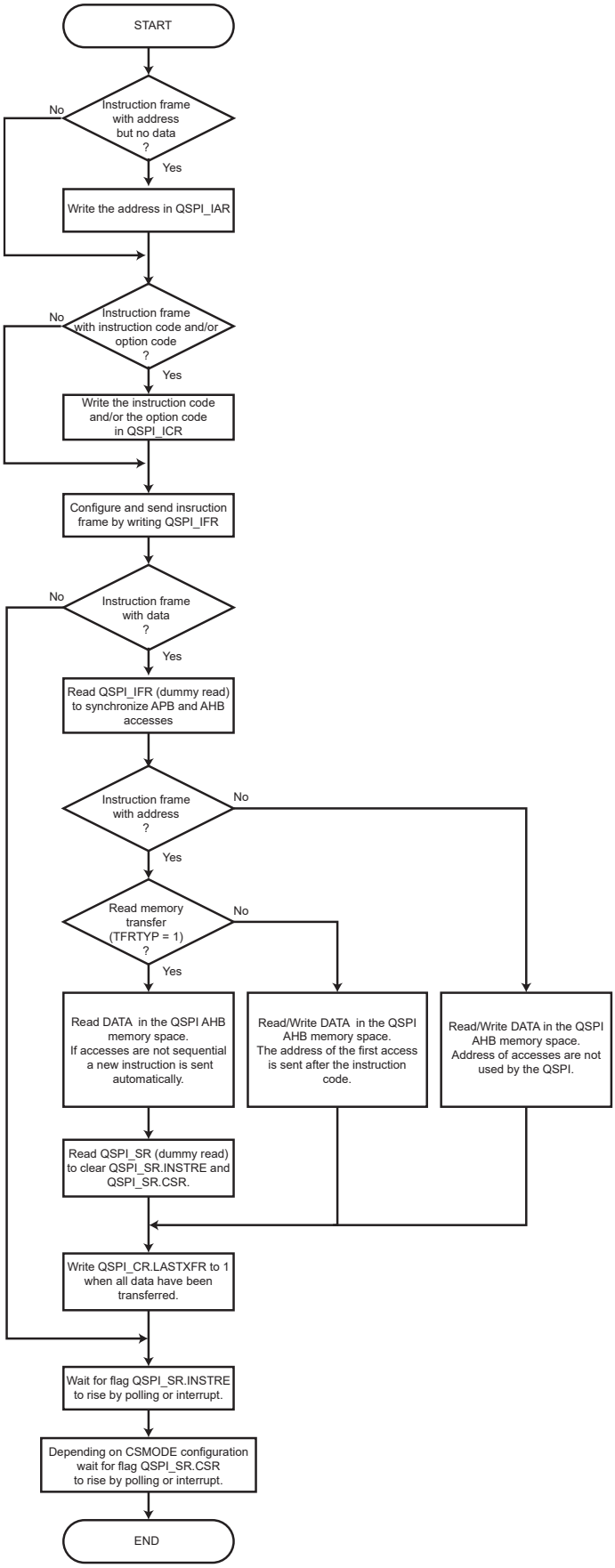
Value	Description
0	Disables the write protection on the Control register if WPKEY corresponds to 0x535049.
1	Enables the write protection on the Control register if WPKEY corresponds to 0x535049.

Bit 1 – WPITEN Write Protection Interrupt Enable

Value	Description
0	Disables the write protection on Interrupt registers if WPKEY corresponds to 0x535049.
1	Enables the write protection on Interrupt registers if WPKEY corresponds to 0x535049.

Bit 0 – WPEN Write Protection Enable

Figure 42-9. Instruction Transmission Flow Diagram



44.8.3 Receive Operations

A receive frame is triggered by a start event and can be followed by synchronization data before data transmission.

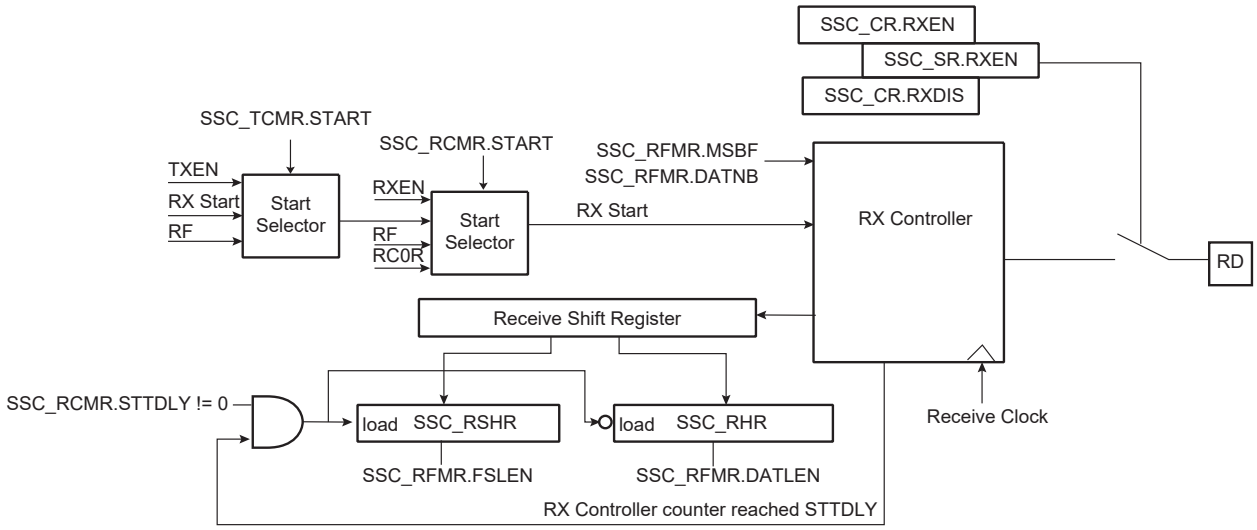
The start event is configured setting the Receive Clock Mode Register (SSC_RCMR). See Start.

The frame synchronization is configured by setting the Receive Frame Mode Register (SSC_RFMR). See Frame Synchronization.

The receiver uses a shift register clocked by the receive clock signal and the start mode selected in the SSC_RCMR. The data is transferred from the shift register depending on the data format selected.

When the receiver shift register is full, the SSC transfers this data in the holding register, the status flag RXRDY is set in the SSC_SR and the data can be read in the receiver holding register. If another transfer occurs before read of the Receive Holding Register (SSC_RHR), the status flag OVERUN is set in the SSC_SR and the receiver shift register is transferred in the SSC_RHR.

Figure 44-12. Receive Block Diagram



44.8.4 Start

The transmitter and receiver can both be programmed to start their operations when an event occurs, respectively in the Transmit Start Selection (START) field of SSC_TCMR and in the Receive Start Selection (START) field of SSC_RCMR.

Under the following conditions the start event is independently programmable:

- Continuous. In this case, the transmission starts as soon as a word is written in SSC_THR and the reception starts as soon as the receiver is enabled.
- Synchronously with the transmitter/receiver
- On detection of a falling/rising edge on TF/RF
- On detection of a low level/high level on TF/RF
- On detection of a level change or an edge on TF/RF

A start can be programmed in the same manner on either side of the Transmit/Receive Clock Register (SSC_RCMR/SSC_TCMR). Thus, the start could be on TF (Transmit) or RF (Receive).

Moreover, the receiver can start when data is detected in the bit stream with the Compare Functions.

46.7.3 USART Mode Register

Name: US_MR
Offset: 0x0004
Reset: 0x0
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

For SPI configuration, see "USART Mode Register (SPI_MODE)".

Bit	31	30	29	28	27	26	25	24
	ONEBIT	MODSYNC	MAN	FILTER		MAX_ITERATION[2:0]		
Access								
Reset	0	0	0	0		0	0	0

Bit	23	22	21	20	19	18	17	16
	INVDATA	VAR_SYNC	DSNACK	INACK	OVER	CLKO	MODE9	MSBF
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CHMODE[1:0]		NBSTOP[1:0]		PAR[2:0]			SYNC
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CHRL[1:0]		USCLKS[1:0]		USART_MODE[3:0]			
Access								
Reset	0	0	0	0	0	0	0	0

Bit 31 – ONEBIT Start Frame Delimiter Selector

Value	Description
0	Start frame delimiter is COMMAND or DATA SYNC.
1	Start frame delimiter is one bit.

Bit 30 – MODSYNC Manchester Synchronization Mode

Value	Description
0	The Manchester start bit is a 0 to 1 transition
1	The Manchester start bit is a 1 to 0 transition.

Bit 29 – MAN Manchester Encoder/Decoder Enable

Value	Description
0	Manchester encoder/decoder are disabled.
1	Manchester encoder/decoder are enabled.

Bit 28 – FILTER Receive Line Filter

46.7.32 USART LIN Mode Register

Name: US_LINMR
Offset: 0x0054
Reset: 0x0
Property: Read/Write

This register is relevant only if USART_MODE = 0xA or 0xB in the USART Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset							0	0

Bit	15	14	13	12	11	10	9	8
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset	0	0	0	0	0	0	0	0

Bit 17 – SYNCDIS Synchronization Disable

Value	Description
0	The synchronization procedure is performed in LIN slave node configuration.
1	The synchronization procedure is not performed in LIN slave node configuration.

Bit 16 – PDCM DMAC Mode

Value	Description
0	The LIN mode register US_LINMR is not written by the DMAC.
1	The LIN mode register US_LINMR (excepting that flag) is written by the DMAC.

Bits 15:8 – DLC[7:0] Data Length Control

Value	Description
0-255	Defines the response data length if DLM = 0,in that case the response data length is equal to DLC+1 bytes.

Bit 7 – WKUPTYP Wakeup Signal Type

47.6.10 UART Comparison Register

Name: UART_CMPR
Offset: 0x24
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	VAL2[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
		CMPPAR		CMPMODE				
Access		R/W		R/W				
Reset		0		0				

Bit	7	6	5	4	3	2	1	0
	VAL1[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – VAL2[7:0] Second Comparison Value for Received Character

Value	Description
0-255	The received character must be lower or equal to the value of VAL2 and higher or equal to VAL1 to set CMP flag in UART_SR. If asynchronous partial wake-up (SleepWalking) is enabled in PMC_SLPWK_ER, the UART requests a system wake-up if condition is met.

Bit 14 – CMPPAR Compare Parity

Value	Description
0	The parity is not checked and a bad parity cannot prevent from waking up the system.
1	The parity is checked and a matching condition on data can be cancelled by an error on parity bit, so no wake-up is performed.

Bit 12 – CMPMODE Comparison Mode

Value	Name	Description
0	FLAG_ONLY	Any character is received and comparison function drives CMP flag.
1	START_CONDITION	Comparison condition must be met to start reception.

Bits 7:0 – VAL1[7:0] First Comparison Value for Received Character

HBI Channel	CAT Address	CAT Offset
0x3E	0x8F	110
0x3F	0x8F	111

48.6.3.3 Routing Fabric Block

The Routing Fabric (RF) block manages the flow of data between the MediaLB Port and the HBI Port. Bus multiplexers and a bus arbiter are implemented in the RF block for accessing the channel table RAM (CTR) and data buffer RAM (DBR).

Each DMA controller in the routing fabric uses Channel Descriptors (stored in the CTR) to manage access to dynamic buffers in the DBR.

Data Buffer RAM

The MLB has an external data buffer RAM (DBR) that is 8-bit x 16k entries deep. The DBR provides dynamic circular buffering between the transmit and receive devices.

The size and location of each data buffer is defined by software in the channel descriptor table (CDT), which is located in the CTR.

Receive devices retain the write address pointer to the associated circular data buffer in the DBR, while transmit devices retain the read address pointer. The DMA controllers in the routing fabric are responsible for ensuring that the circular buffers do not overflow or underflow. Each channel type (e.g., synchronous, isochronous, asynchronous and control) has Full and Empty detection.

- Synchronous Channels
  For synchronous channels, two mechanisms prevent overflow and underflow of the data buffer:
  - Hardware aligns the read pointer (RPTR) to the write pointer (WPTR) to ensure an offset of two sub-buffers.
  - RPTR and WPTR are periodically synchronized to the start of the next sub-buffer (e.g. following a FRAMESYNC).
- Isochronous Channels
  For isochronous channels, hardware does not read from an empty data buffer or write to a full data buffer. The conditions used by hardware for detection include:

  Data buffer Empty condition: (RPTR = WPTR) AND (BF = 0), and

  Data buffer Full condition: (WPTR = RPTR) AND (BF = 1).
- Asynchronous and Control Channels
  For asynchronous and control channels, hardware does not read from an empty data buffer or write to a full data buffer. Hardware evaluates the DMA pointers (RPTR, WPTR) and packet count (RPC, WPC) to detect the data buffer condition, where:
  - Data buffer Empty condition: (RPTR = WPTR) AND (RPC = WPC), and
  - Data buffer Full condition: ((WPTR = RPTR) AND (WPC != RPC)) OR (WPC = (RPC - 1)).

Channel Table RAM

The MLB has an external Channel Table RAM (CTR) that is 128-bit x 144-entry. The CTR allows system software to dynamically configure channel routing and allocate data buffers in the DBR.

The CTR is logically divided into three sub-tables:

- Channel Descriptor Table (CDT)

49.6.1 MCAN Core Release Register

Name: MCAN_CREL
Offset: 0x00
Reset: 0xrrrddddd
Property: Read-only

Due to clock domain crossing, there is a delay between when a register bit or field is written and when the related status register bits are updated.

Bit	31	30	29	28	27	26	25	24
	REL[3:0]				STEP[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	23	22	21	20	19	18	17	16
	SUBSTEP[3:0]				YEAR[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	15	14	13	12	11	10	9	8
	MON[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bit	7	6	5	4	3	2	1	0
	DAY[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	x	x	x	x	x	x	x	x

Bits 31:28 – REL[3:0] Core Release
One digit, BCD-coded.

Bits 27:24 – STEP[3:0] Step of Core Release
One digit, BCD-coded.

Bits 23:20 – SUBSTEP[3:0] Sub-step of Core Release
One digit, BCD-coded.

Bits 19:16 – YEAR[3:0] Timestamp Year
One digit, BCD-coded. This field is set by generic parameter on MCAN synthesis.

Bits 15:8 – MON[7:0] Timestamp Month
Two digits, BCD-coded. This field is set by generic parameter on MCAN synthesis.

Bits 7:0 – DAY[7:0] Timestamp Day
Two digits, BCD-coded. This field is set by generic parameter on MCAN synthesis.

Offset	Name	Bit Pos.								
		31:24								CVM
0x0144	PWM_CMPVUPD1	7:0	CVUPD[7:0]							
		15:8	CVUPD[15:8]							
		23:16	CVUPD[23:16]							
		31:24								CVMUPD
0x0148	PWM_CMPM1	7:0	CTR[3:0]							CEN
		15:8	CPRCNT[3:0]				CPR[3:0]			
		23:16	CUPRCNT[3:0]				CUPR[3:0]			
		31:24								
0x014C	PWM_CMPMUPD1	7:0	CTRUPD[3:0]							CENUPD
		15:8					CPRUPD[3:0]			
		23:16					CUPRUPD[3:0]			
		31:24								
0x0150	PWM_CMPV2	7:0	CV[7:0]							
		15:8	CV[15:8]							
		23:16	CV[23:16]							
		31:24								CVM
0x0154	PWM_CMPVUPD2	7:0	CVUPD[7:0]							
		15:8	CVUPD[15:8]							
		23:16	CVUPD[23:16]							
		31:24								CVMUPD
0x0158	PWM_CMPM2	7:0	CTR[3:0]							CEN
		15:8	CPRCNT[3:0]				CPR[3:0]			
		23:16	CUPRCNT[3:0]				CUPR[3:0]			
		31:24								
0x015C	PWM_CMPMUPD2	7:0	CTRUPD[3:0]							CENUPD
		15:8					CPRUPD[3:0]			
		23:16					CUPRUPD[3:0]			
		31:24								
0x0160	PWM_CMPV3	7:0	CV[7:0]							
		15:8	CV[15:8]							
		23:16	CV[23:16]							
		31:24								CVM
0x0164	PWM_CMPVUPD3	7:0	CVUPD[7:0]							
		15:8	CVUPD[15:8]							
		23:16	CVUPD[23:16]							
		31:24								CVMUPD
0x0168	PWM_CMPM3	7:0	CTR[3:0]							CEN
		15:8	CPRCNT[3:0]				CPR[3:0]			
		23:16	CUPRCNT[3:0]				CUPR[3:0]			
		31:24								
0x016C	PWM_CMPMUPD3	7:0	CTRUPD[3:0]							CENUPD
		15:8					CPRUPD[3:0]			
		23:16					CUPRUPD[3:0]			
		31:24								
0x0170	PWM_CMPV4	7:0	CV[7:0]							

54.7.2 ACC Mode Register

Name: ACC_MR
Offset: 0x04
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the ACC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
		FE	SELFS	INV		EDGETYP[1:0]		ACEN
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
		SELPLUS[2:0]				SELMINUS[2:0]		
Access		R/W	R/W	R/W		R/W	R/W	R/W
Reset		0	0	0		0	0	0

Bit 14 – FE Fault Enable
0 (DIS): The FAULT output is tied to 0.

1 (EN): The FAULT output is driven by the signal defined by SELFS.

Bit 13 – SELFS Selection Of Fault Source
0 (CE): The CE flag is used to drive the FAULT output.

1 (OUTPUT): The output of the analog comparator flag is used to drive the FAULT output.

Bit 12 – INV Invert Comparator Output
0 (DIS): Analog comparator output is directly processed.

1 (EN): Analog comparator output is inverted prior to being processed.

Bits 10:9 – EDGETYP[1:0] Edge Type

Value	Name	Description
0	RISING	Only rising edge of comparator output
1	FALLING	Falling edge of comparator output
2	ANY	Any edge of comparator output

57.5.12 AES Plaintext/Ciphertext Length Register

Name: AES_CLENR
Offset: 0x74
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	CLEN[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CLEN[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CLEN[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CLEN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CLEN[31:0] Plaintext/Ciphertext Length
Length in bytes of the plaintext/ciphertext (C) data that is to be processed.

Note: The maximum byte length of the C portion of a message is limited to the 32-bit counter length.

58.7 USB Transceiver Characteristics

The device conforms to all voltage, power, and timing characteristics and specifications as set forth in the USB 2.0 Specification. Please refer to the USB 2.0 Specification for more information.

Table 58-28. USB Transceiver Dynamic Power Consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{BIAS}	Bias Current Consumption on VBG	–	–	–	12	mA
$I_{VDDUTMII}$	HS Transceiver Current Consumption	HS transmission	–	–	44	mA
	HS Transceiver Current Consumption	HS reception	–	–	24	mA
	LS / FS Transceiver Current Consumption	FS transmission 0m cable (see **Note 1**)	–	–	5	mA
	LS / FS Transceiver Current Consumption	FS transmission 5m cable (see **Note 1**)	–	–	30	mA
	LS / FS Transceiver Current Consumption	FS reception (see **Note 1**)	–	–	1	mA
$I_{VDDUTMIC}$	Core	–	–	–	10	mA

Note:

1. Including 1 mA due to pullup/pulldown current consumption.

58.8 AFE Characteristics

Electrical data are in accordance with an operating temperature range from -40°C to +105°C unless otherwise specified.

VREFP is the positive reference of the AFE. The VREFN pin must be connected to ground.

DAC1 and DAC0 provide an analog output voltage (V_{DAC}) in the range [0 : VREFP] with an accuracy equal to 10 bits. The DAC output voltage is single-ended and is used as a reference node by the sampling stage S/H0 and S/H1 (Sample-and-Hold PGA), relative to the single-ended input signal being sampled on the selected channel.

As a consequence, programming the DAC output voltage offers a capability to compensate for a DC offset on the input signal being sampled. DC offset compensation is effective in single-ended operation and is not effective in fully differential operation.

During fully differential operation, the DAC10 output voltage can be programmed at VREFP/2, by using the 10-bit code 512. The DAC value does not affect the AFE output code.

VREFP/2 on DAC0 and DAC1 is not automatically set and must be programed as the code 512 into the channel corresponding DAC0 and DAC1.

The following figures illustrate the architecture of the AFE in Single-ended and in Differential modes.