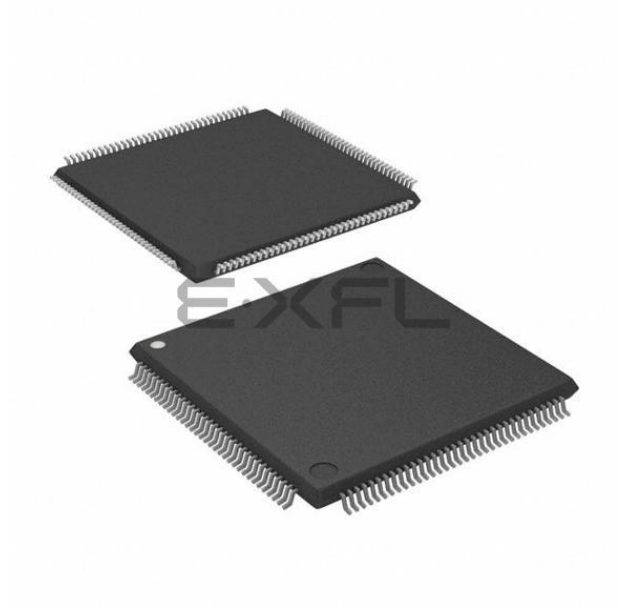

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70q21b-an

5. Automotive Quality Grade

The SAM V70 and SAM V71 devices have been developed and manufactured according to the most stringent requirements of the international standard ISO-TS-16949. This data sheet contains limit values extracted from the results of extensive characterization (temperature and voltage).

The quality and reliability of the SAM V70 and SAM V71 has been verified during regular product qualification as per AEC-Q100 grade 2 (–40°C to +105°C).

Table 5-1. Temperature Grade Identification for Automotive Products

Temperature (°C)	Temperature Identifier	Comments
–40°C to +105°C	B	AEC-Q100 Grade 2

Function	Application	Description	Event Source	Event Destination
	Motor control	Puts the PWM outputs in Safe mode (overspeed detection through timer quadrature decoder) (see **Notes 2, 6**)	TC0	PWM0
			TC1	PWM1
	General-purpose, motor control, power factor correction (PFC)	Puts the PWM outputs in Safe mode (general-purpose fault inputs) (see **Note 2**)	PIO PA9, PD8, PD9	PWM0
			PIO PA21, PA26, PA28	PWM1
Security	General-purpose	Immediate GPBR clear (asynchronous) on tamper detection through WKUP0/1 IO pins (see **Note 5**)	PIO WKUP0/1	GPBR
Measurement trigger	Power factor correction (DC-DC, lighting, etc.)	Duty cycle output waveform correction Trigger source selection in PWM (see **Notes 7, 8**)	ACC	PWM0
			PIO PA10, PA22	PWM0
			ACC	PWM1
			PIO PA30, PA18	PWM1
	General-purpose	Trigger source selection in AFEC (see **Note 9**)	PIO AFE0_ADTRG	AFEC0
			TC0 TIOA0	AFEC0
			TC0 TIOA1	AFEC0
			TC0 TIOA2	AFEC0
			ACC	AFEC0
	Motor control	ADC-PWM synchronization (see **Notes 12, 14**) Trigger source selection in AFEC (see **Note 9**)	PWM0 Event Line 0 and 1	AFEC0
	General-purpose	Trigger source selection in AFEC (see **Note 9**)	PIO AFE1_ADTRG	AFEC1
			TC1 TIOA3	AFEC1
			TC1 TIOA4	AFEC1
			TC1 TIOA5	AFEC1
			ACC	AFEC1
	Motor control	ADC-PWM synchronization (see **Notes 12, 14**) Trigger source selection in AFEC (see **Note 9**)	PWM1 Event Line 0 and 1	AFEC1

15. ARM Cortex-M7 (ARM)

Refer to ARM reference documents *Cortex-M7 Processor User Guide* (ARM DUI 0644) and *Cortex-M7 Technical Reference Manual* (ARM DDI 0489), available on www.arm.com.

15.1 ARM Cortex-M7 Configuration

The following table provides the configuration for the ARM Cortex-M7 processor in SAM E70/S70/V70/V71 devices.

Table 15-1. ARM Cortex-M7 Configuration

Features	Configuration
Debug	
Comparator set	Full comparator set: 4 DWT and 8 FPB comparators
ETM support	Instruction ETM interface
Internal Trace support (ITM)	ITM and DWT trace functionality implemented
CTI and WIC	Not embedded
TCM	
ITCM max size	128 KB
DTCM max size	256 KB
Cache	
Cache size	16 KB for instruction cache, 16 KB for data cache
Number of sets	256 for instruction cache, 128 for data cache
Number of ways	2 for instruction cache, 4 for data cache
Number of words per cache line	8 words (32 bytes)
ECC on Cache	Embedded
NVIC	
IRQ number	74
IRQ priority levels	8
MPU	
Number of regions	16
FPU	
FPU precision	Single and double precision
AHB Port	
AHBP addressing size	512 MB

31.20.8 PMC Clock Generator Main Oscillator Register

Name: CKGR_MOR
Offset: 0x0020
Reset: 0x00000008
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
						XT32KFME	CFDEN	MOSCSEL
Access								
Reset						0	0	0

Bit	23	22	21	20	19	18	17	16
	KEY[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	MOSCXTST[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		MOSCRCF[2:0]			MOSCRCEN	WAITMODE	MOSCXTBY	MOSCXTEN
Access								
Reset		0	0	0	1	0	0	0

Bit 26 – XT32KFME 32.768 kHz Crystal Oscillator Frequency Monitoring Enable

Value	Description
0	The 32.768 kHz crystal oscillator frequency monitoring is disabled.
1	The 32.768 kHz crystal oscillator frequency monitoring is enabled.

Bit 25 – CFDEN Clock Failure Detector Enable

Value	Description
0	The clock failure detector is disabled.
1	The clock failure detector is enabled.

Bit 24 – MOSCSEL Main Clock Oscillator Selection

Value	Description
0	The Main RC oscillator is selected.
1	The Main crystal oscillator is selected.

Bits 23:16 – KEY[7:0] Write Access Password

Value	Name	Description
0x37	PASSWD	Writing any other value in this field aborts the write operation.

Value	Description
0	MAINF value is not valid or the measured oscillator is disabled or a measure has just been started by means of RCMEAS.
1	The measured oscillator has been enabled previously and MAINF value is available. Note: To ensure that a correct value is read on the MAINF field, the MAINFRDY flag must be read at '1' then another read access must be performed on the register to get a stable value on the MAINF field.

Bits 15:0 – MAINF[15:0] Main Clock Frequency
Gives the number of cycles of the clock selected by the bit CCSS within 16 SLCK periods. To calculate the frequency of the measured clock:

$f_{SELCLK} = (MAINF \times f_{SLCK})/16$

where frequency is in MHz.

Related Links

58. Electrical Characteristics for SAM V70/V71
59. Electrical Characteristics for SAM E70/S70

32.5.13 Programmable Schmitt Trigger

It is possible to configure each input for the Schmitt trigger. By default the Schmitt trigger is active. Disabling the Schmitt trigger is requested when using the QTouch® Library.

32.5.14 Parallel Capture Mode

32.5.14.1 Overview

The PIO Controller integrates an interface able to read data from a CMOS digital image sensor, a high-speed parallel ADC, a DSP synchronous port in Synchronous mode, etc. For better understanding and to ease reading, the following description uses an example with a CMOS digital image sensor.

32.5.14.2 Functional Description

The CMOS digital image sensor provides a sensor clock, an 8-bit data synchronous with the sensor clock and two data enables which are also synchronous with the sensor clock.

Figure 32-8. PIO Controller Connection with CMOS Digital Image Sensor

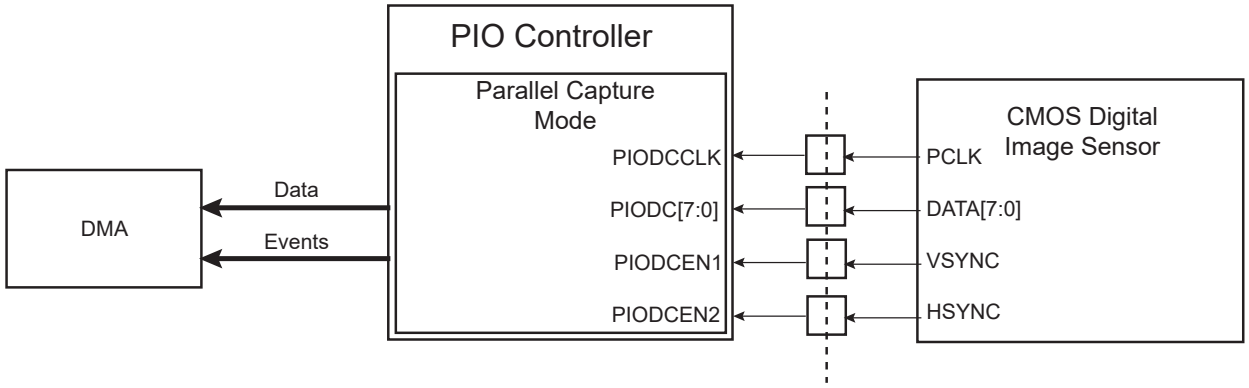
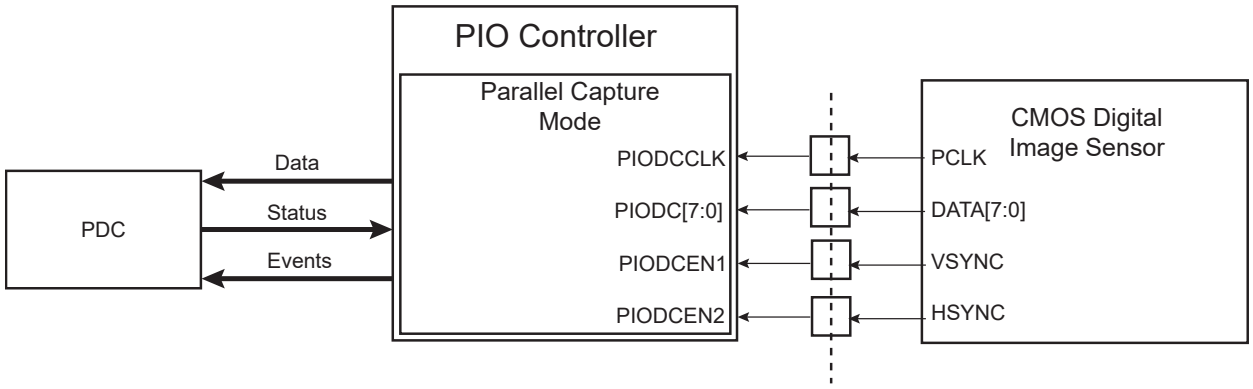


Figure 32-9.



As soon as the Parallel Capture mode is enabled by writing a one to the PCEN bit in PIO_PCMR, the I/O lines connected to the sensor clock (PIODCCLK), the sensor data (PIODC[7:0]) and the sensor data enable signals (PIODCEN1 and PIODCEN2) are configured automatically as inputs. To know which I/O lines are associated with the sensor clock, the sensor data and the sensor data enable signals, refer to the I/O multiplexing table(s) in the section “Package and Pinout”.

Once enabled, the Parallel Capture mode samples the data at rising edge of the sensor clock and resynchronizes it with the peripheral clock domain.

32.6.1.43 PIO Rising Edge/High-Level Select Register

Name: PIO_REHLSR
Offset: 0x00D4
Property: Write-only

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Rising Edge/High-Level Interrupt Selection

Value	Description
0	No effect.
1	The interrupt source is set to a rising edge detection or high-level detection event, depending on PIO_ELSR.

Offset	Name	Bit Pos.								
		23:16					STALLRQ	RSTDT	NYETDIS	EPDISHDMA
		31:24								
0x01C4	USBHS_DEVEPTIMR1 (ISOENPT)	7:0	SHORTPACKETE	CRCERRE	OVERFE	HBISOFLUSHE	HBISOINERRE	UNDERFE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE		ERRORTRANSE	DATAXE	MDATAE
		23:16						RSTDT		EPDISHDMA
		31:24								
0x01C8	USBHS_DEVEPTIMR2	7:0	SHORTPACKETE	STALLEDE	OVERFE	NAKINE	NAKOUTE	RXSTPE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE				
		23:16					STALLRQ	RSTDT	NYETDIS	EPDISHDMA
		31:24								
0x01C8	USBHS_DEVEPTIMR2 (ISOENPT)	7:0	SHORTPACKETE	CRCERRE	OVERFE	HBISOFLUSHE	HBISOINERRE	UNDERFE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE		ERRORTRANSE	DATAXE	MDATAE
		23:16						RSTDT		EPDISHDMA
		31:24								
0x01CC	USBHS_DEVEPTIMR3	7:0	SHORTPACKETE	STALLEDE	OVERFE	NAKINE	NAKOUTE	RXSTPE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE				
		23:16					STALLRQ	RSTDT	NYETDIS	EPDISHDMA
		31:24								
0x01CC	USBHS_DEVEPTIMR3 (ISOENPT)	7:0	SHORTPACKETE	CRCERRE	OVERFE	HBISOFLUSHE	HBISOINERRE	UNDERFE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE		ERRORTRANSE	DATAXE	MDATAE
		23:16						RSTDT		EPDISHDMA
		31:24								
0x01D0	USBHS_DEVEPTIMR4	7:0	SHORTPACKETE	STALLEDE	OVERFE	NAKINE	NAKOUTE	RXSTPE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE				
		23:16					STALLRQ	RSTDT	NYETDIS	EPDISHDMA
		31:24								
0x01D0	USBHS_DEVEPTIMR4 (ISOENPT)	7:0	SHORTPACKETE	CRCERRE	OVERFE	HBISOFLUSHE	HBISOINERRE	UNDERFE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE		ERRORTRANSE	DATAXE	MDATAE
		23:16						RSTDT		EPDISHDMA
		31:24								
0x01D4	USBHS_DEVEPTIMR5	7:0	SHORTPACKETE	STALLEDE	OVERFE	NAKINE	NAKOUTE	RXSTPE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE				
		23:16					STALLRQ	RSTDT	NYETDIS	EPDISHDMA
		31:24								

Offset	Name	Bit Pos.								
0x0544	USBHS_HSTPIPISR5 (INTPIPES)	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0544	USBHS_HSTPIPISR5 (ISOPIPES)	7:0	SHORTPACKETI	CRCERRI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0548	USBHS_HSTPIPISR6	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	TXSTPI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0548	USBHS_HSTPIPISR6 (INTPIPES)	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0548	USBHS_HSTPIPISR6 (ISOPIPES)	7:0	SHORTPACKETI	CRCERRI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x054C	USBHS_HSTPIPISR7	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	TXSTPI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x054C	USBHS_HSTPIPISR7 (INTPIPES)	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x054C	USBHS_HSTPIPISR7 (ISOPIPES)	7:0	SHORTPACKETI	CRCERRI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0550	USBHS_HSTPIPISR8	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	TXSTPI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						

39.6.31 Host General Control Register

Name: USBHS_HSTCTRL
Offset: 0x0400
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
			SPDCONF[1:0]			RESUME	RESET	SOFE
Access								
Reset			0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 13:12 – SPDCONF[1:0] Mode Configuration
This field contains the host speed capability:.

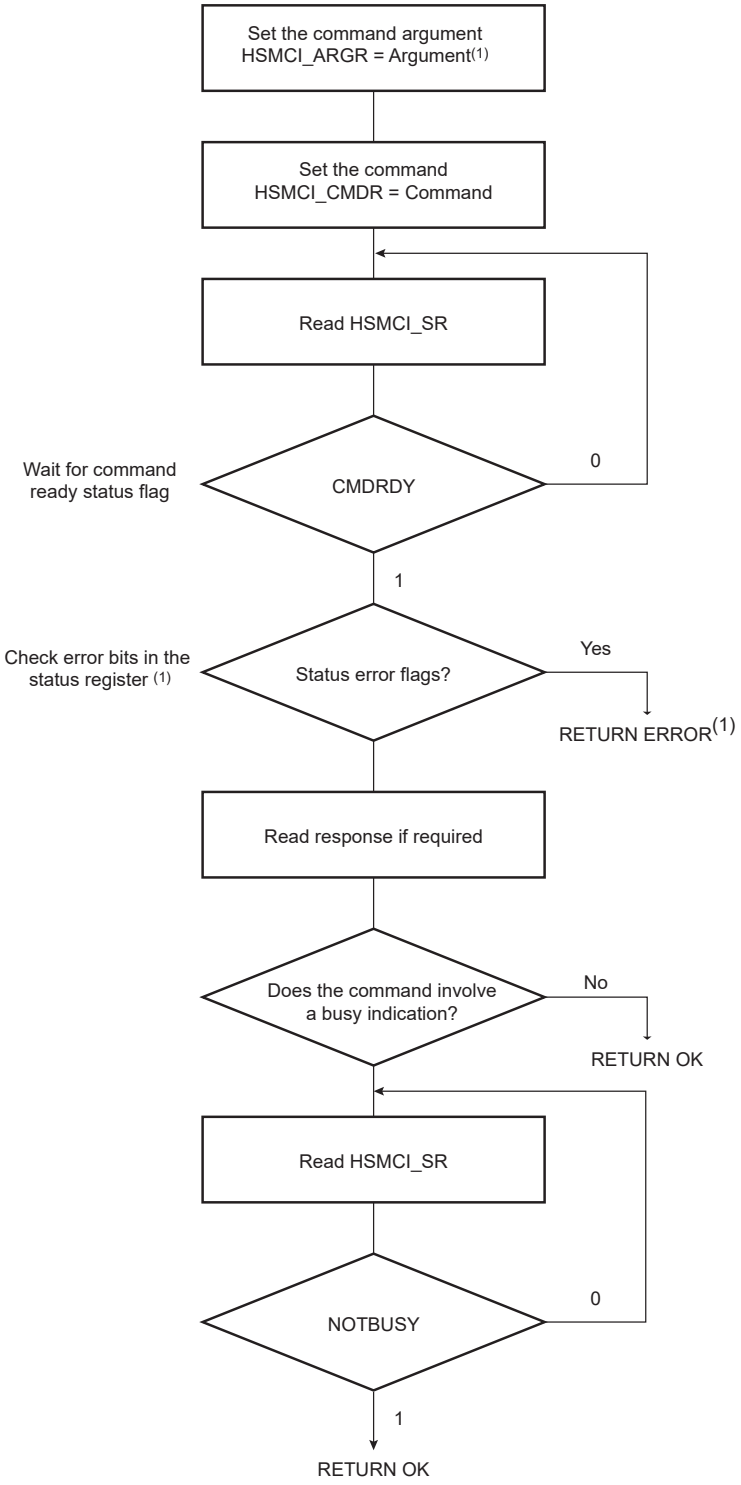
Value	Name	Description
0	NORMAL	The host starts in Full-speed mode and performs a high-speed reset to switch to High-speed mode if the downstream peripheral is high-speed capable.
1	LOW_POWER	For a better consumption, if high speed is not needed.
2	HIGH_SPEED	Forced high speed.
3	FORCED_FS	The host remains in Full-speed mode whatever the peripheral speed capability.

Bit 10 – RESUME Send USB Resume
This bit is cleared when the USB Resume has been sent or when a USB reset is requested.

This bit should be written to one only when the start of frame generation is enabled (SOFE = 1).

Value	Description
0	No effect.
1	Generates a USB Resume on the USB bus.

Figure 40-7. Command/Response Functional Flow Diagram



Note: If the command is SEND_OP_COND, the CRC error flag is always present (refer to R3 response in the High Speed MultiMedia Card specification) .

46.7.14 USART Interrupt Mask Register (SPI_MODE)

Name: US_IMR (SPI_MODE)
Offset: 0x0010
Reset: 0x0
Property: Read-only

This configuration is relevant only if USART_MODE = 0xE or 0xF in the USART Mode Register.

The following configuration values are valid for all listed bit names of this register:

0: The corresponding interrupt is not enabled.

1: The corresponding interrupt is enabled.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset					0			

Bit	15	14	13	12	11	10	9	8
Access								
Reset						0	0	

Bit	7	6	5	4	3	2	1	0
Access								
Reset			0				0	0

Bit 19 – NSSE NSS Line (Driving CTS Pin) Rising or Falling Edge Event Interrupt Mask

Bit 10 – UNRE SPI Underrun Error Interrupt Mask

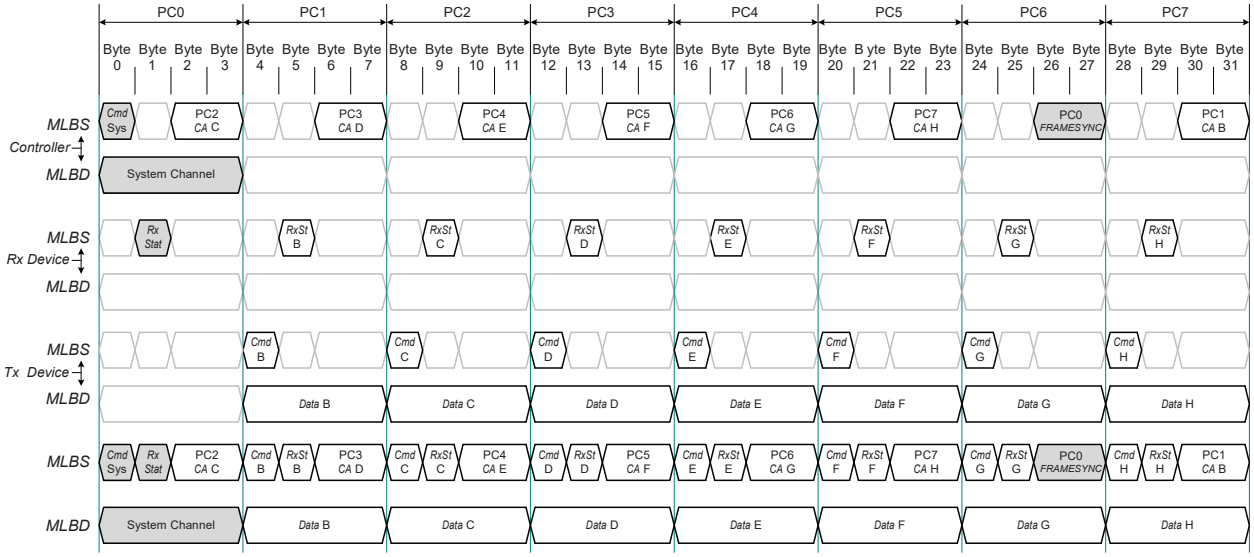
Bit 9 – TXEMPTY TXEMPTY Interrupt Mask

Bit 5 – OVRE Overrun Error Interrupt Mask

Bit 1 – TXRDY TXRDY Interrupt Mask

Bit 0 – RXRDY RXRDY Interrupt Mask

Figure 48-5. 3-pin MediaLB 256Fs Interface Example



48.6.1.7 Initialization

At power up, the MediaLB Controller might output a MLBReset command in the System Channel (all System commands are optional). Upon reception of the MLBReset command, all MediaLB Devices will cancel any current transmissions or receptions and clear their buffers.

Two scenarios are supported to configure MediaLB Devices and ChannelAddresses:

- Static pre-configured before startup. The system implementor decides which ChannelAddresses are to be used for every communication path on MediaLB. This static MediaLB configuration can be communicated by the EHC to the Controller through pre-defined power-up logical channels or through a secondary port.
- Dynamically at run-time. Dynamic configuration allows the board designer to support multiple build options where the EHC can query to find out if a particular Device is present or not on a particular board. The EHC instructs the Controller to scan for a particular DeviceAddress in the System Channel. The Controller uses the MLBScan command to look for a Device. The Controller then notifies the EHC whether the Device is present or not. If the Device is present, then the EHC can instruct the Controller to set the ChannelAddresses for the Device found. The EHC sends messages to the Controller to set each Indices/Logical channel, and waits the appropriate amount of time between each message as specified in the Devices documentation. When that particular Device is configured, the EHC can instruct the Controller to scan for the next Device.

Since the MediaLB Controller is the interface between the MediaLB Devices and the MOST Network, the Controller provides the MLBC signal and will also continue to operate even when the MOST Network is unlocked. When no activity exists on MediaLB, the Controller can shut off the MLBC placing MediaLB in a low-power state. The ChannelAddress assignments are not affected in low-power state; therefore, the same communication paths exists once MLBC is restarted.

MediaLB Devices are synchronously slaved to the MediaLB Controller through the MLBC signal. Since the Controller is synchronized to the MOST Network, the MLBC signal provides Network synchronization to all MediaLB Devices. Once the Controller starts up MLBC, all MediaLB Devices must synchronize to the MediaLB frame before communication can commence. When not frame-locked, Devices must search for the FRAMESYNC pattern, which defines a byte and physical channel boundary. Additionally, the start of the MediaLB frame (PC0) occurs one quadlet after FRAMESYNC is present on the bus. Even when a

49.5.4.1 Acceptance Filtering

The MCAN offers the possibility to configure two sets of acceptance filters, one for standard identifiers and one for extended identifiers. These filters can be assigned to an Rx Buffer or to Rx FIFO 0,1. For acceptance filtering each list of filters is executed from element #0 until the first matching element. Acceptance filtering stops at the first matching element. The following filter elements are not evaluated for this message.

The main features are:

- Each filter element can be configured as
  - range filter (from - to)
  - filter for one or two dedicated IDs
  - classic bit mask filter
- Each filter element is configurable for acceptance or rejection filtering
- Each filter element can be enabled / disabled individually
- Filters are checked sequentially, execution stops with the first matching filter element

Related configuration registers are:

- Global Filter Configuration (MCAN_GFC)
- Standard ID Filter Configuration (MCAN_SIDFC)
- Extended ID Filter Configuration (MCAN_XIDFC)
- Extended ID and Mask (MCAN_XIDAM)

Depending on the configuration of the filter element (SFEC/EFEC) a match triggers one of the following actions:

- Store received frame in FIFO 0 or FIFO 1
- Store received frame in Rx Buffer
- Store received frame in Rx Buffer and generate pulse at filter event pin
- Reject received frame
- Set High Priority Message interrupt flag (MCAN_IR.HPM)
- Set High Priority Message interrupt flag (MCAN_IR.HPM) and store received frame in FIFO 0 or FIFO 1

Acceptance filtering is started after the complete identifier has been received. After acceptance filtering has completed, and if a matching Rx Buffer or Rx FIFO has been found, the Message Handler starts writing the received message data in portions of 32 bit to the matching Rx Buffer or Rx FIFO. If the CAN protocol controller has detected an error condition (e.g. CRC error), this message is discarded with the following impact on the effected Rx Buffer or Rx FIFO:

- Rx Buffer
  New Data flag of matching Rx Buffer is not set, but Rx Buffer (partly) overwritten with received data. For error type, see MCAN_PSR.LEC and MCAN_PSR.DLEC.
- Rx FIFO
  Put index of matching Rx FIFO is not updated, but related Rx FIFO element (partly) overwritten with received data. For error type, see MCAN_PSR.LEC and MCAN_PSR.DLEC. In case the matching Rx FIFO is operated in Overwrite mode, the boundary conditions described in Rx FIFO Overwrite Mode have to be considered.

Bits 15:2 – F1SA[13:0] Receive FIFO 1 Start Address
Start address of Receive FIFO 1 in Message RAM (32-bit word address, see Message RAM Configuration).

Write F1SA with the bits [15:2] of the 32-bit address.

Depending on the quadrature signals, the direction is decoded and allows to count up or down in TC channels 0 and 1. The direction status is reported on TC_QISR.

50.6.16.5 Speed Measurement

When TC_BMR.SPEEDEN is set, the speed measure is enabled on channel 0.

A time base must be defined on channel 2 by writing the TC_RC2 period register. Channel 2 must be configured in Waveform mode (WAVE bit set) in TC_CMR2. The WAVSEL field must be defined with 0x10 to clear the counter by comparison and matching with TC_RC value. Field ACPC must be defined at 0x11 to toggle TIOAx output.

This time base is automatically fed back to TIOAx of channel 0 when QDEN and SPEEDEN are set.

Channel 0 must be configured in Capture mode (WAVE = 0 in TC_CMR0). TC_CMR0.ABETRG must be configured at 1 to select TIOAx as a trigger for this channel.

EDGTRG must be set to 0x01, to clear the counter on a rising edge of the TIOAx signal and field LDRA must be set accordingly to 0x01, to load TC_RA0 at the same time as the counter is cleared (LDRB must be set to 0x01). As a consequence, at the end of each time base period the differentiation required for the speed calculation is performed.

The process must be started by configuring bits CLKEN and SWTRG in the TC_CCR.

The speed can be read on field RA in TC_RA0.

Channel 1 can still be used to count the number of revolutions of the motor.

50.6.16.6 Detecting a Missing Index Pulse

To detect a missing index pulse due contamination, dust, etc., the TC_SR0.CPCS flag can be used. It is also possible to assert the interrupt line if the TC_SR0.CPCS flag is enabled as a source of the interrupt by writing a ‘1’ to TC_IER0.CPCS.

The TC_RC0.RC field must be written with the nominal number of counts per revolution provided by the rotary encoder, plus a margin to eliminate potential noise (e.g., if nominal count per revolution is 1024, then TC_RC0.RC=1026).

If the index pulse is missing, the timer value is not cleared and the nominal value is exceeded, then the comparator on the RC triggers an event, TC_SR0.CPCS=1, and the interrupt line is asserted if TC_IER0.CPCS=1.

The missing index pulse detection is only valid if the bit TC_QISR.DIRCHG=0.

50.6.16.7 Detecting Contamination/Dust at Rotary Encoder Low Speed

The contamination/dust that can be filtered when the rotary encoder speed is high may not be filtered at low speed, thus creating unsollicited direction change, etc.

At low speed, even a minor contamination may appear as a long pulse, and thus not filtered and processed as a standard quadrature encoder pulse.

This contamination can be detected by using the similar method as the missing index detection.

A contamination exists on a phase line if TC_SR.CPCS = 1 and TC_QISR.DIRCHG = 1 when there is no sollicited change of direction.

50.6.16.8 Missing Pulse Detection and Autocorrection

The QDEC is equipped with a circuitry which detects and corrects some errors that may result from contamination on optical disks or other materials producing the quadrature phase signals.

51.7.14 PWM Interrupt Enable Register 2

Name: PWM_IER2
Offset: 0x34
Reset: –
Property: Write-only

This register can only be written if bits WPSWS1 and WPHWS1 are cleared in the PWM Write Protection Status Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CMPU7	CMPU6	CMPU5	CMPU4	CMPU3	CMPU2	CMPU1	CMPU0
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bit	15	14	13	12	11	10	9	8
	CMPM7	CMPM6	CMPM5	CMPM4	CMPM3	CMPM2	CMPM1	CMPM0
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bit	7	6	5	4	3	2	1	0
					UNRE			WRDY
Access					W			W
Reset					–			–

Bits 16, 17, 18, 19, 20, 21, 22, 23 – CMPUx Comparison x Update Interrupt Enable

Bits 8, 9, 10, 11, 12, 13, 14, 15 – CMPMx Comparison x Match Interrupt Enable

Bit 3 – UNRE Synchronous Channels Update Underrun Error Interrupt Enable

Bit 0 – WRDY Write Ready for Synchronous Channels Update Interrupt Enable

51.7.21 PWM Output Selection Clear Register

Name: PWM_OSC
Offset: 0x50
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					OSCL3	OSCL2	OSCL1	OSCL0
Access					W	W	W	W
Reset					0	0	0	–

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					OSCH3	OSCH2	OSCH1	OSCH0
Access					W	W	W	W
Reset					0	0	0	–

Bits 16, 17, 18, 19 – OSCLx Output Selection Clear for PWML output of the channel x

Value	Description
0	No effect.
1	Dead-time generator output DTOLx selected as PWML output of channel x.

Bits 0, 1, 2, 3 – OSCHx Output Selection Clear for PWMH output of the channel x

Value	Description
0	No effect.
1	Dead-time generator output DTOHx selected as PWMH output of channel x.

56.6.6 TRNG Output Data Register

Name: TRNG_ODATA
Offset: 0x50
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	ODATA[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ODATA[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ODATA[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ODATA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ODATA[31:0] Output Data
The 32-bit Output Data register contains the 32-bit random data.

57.5.9 AES Output Data Register x

Name: AES_ODATARx
Offset: 0x50 + x*0x04 [x=0..3]
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	ODATA[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ODATA[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ODATA[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ODATA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ODATA[31:0] Output Data
The four 32-bit Output Data registers contain the 128-bit data block that has been encrypted/decrypted.

AES_ODATAR0 corresponds to the first word, AES_ODATAR3 to the last one.