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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70q21b-cn

All lock regions must be unlocked before the Full Erase command by using the CLB command. Otherwise, the erase command is aborted and no page is erased.

Table 18-8. Full Erase Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	EA
2	Write handshaking	DATA	0

18.3.5.4 Flash Lock Commands

Lock bits can be set using WPL or EWPL commands. They can also be set by using the Set Lock command (SLB). With this command, several lock bits can be activated. A Bit Mask is provided as argument to the command. When bit 0 of the bit mask is set, then the first lock bit is activated.

In the same way, the Clear Lock command (CLB) is used to clear lock bits.

Table 18-9. Set and Clear Lock Bit Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	SLB or CLB
2	Write handshaking	DATA	Bit Mask

Lock bits can be read using Get Lock Bit command (GLB). The n^{th} lock bit is active when the bit n of the bit mask is set.

Table 18-10. Get Lock Bit Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	GLB
2	Read handshaking	DATA	Lock Bit Mask Status 0 = Lock bit is cleared 1 = Lock bit is set

18.3.5.5 Flash General-purpose NVM Commands

General-purpose NVM bits (GP NVM bits) can be set using the Set GPNVM command (SGPB). This command also activates GP NVM bits. A bit mask is provided as argument to the command. When bit 0 of the bit mask is set, then the first GP NVM bit is activated.

In the same way, the Clear GPNVM command (CGPB) is used to clear general-purpose NVM bits. The general-purpose NVM bit is deactivated when the corresponding bit in the pattern value is set to 1.

Table 18-11. Set/Clear GP NVM Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	SGPB or CGPB
2	Write handshaking	DATA	GP NVM bit pattern value

General-purpose NVM bits can be read using the Get GPNVM Bit command (GGPB). The n^{th} GP NVM bit is active when bit n of the bit mask is set.

19.4.11 Write Protection Mode Register

Name: MATRIX_WPMR
Offset: 0x01E4
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	WPKEY[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	WPKEY[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	WPKEY[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
								WPEN
Access								
Reset								0

Bits 31:8 – WPKEY[23:0] Write Protection Key

Value	Name	Description
0x4D4154	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

Bit 0 – WPEN Write Protection Enable
Refer to the "Register Write Protection" section for the list of registers that can be write-protected.

Value	Description
0	Disables the write protection if WPKEY corresponds to 0x4D4154 (“MAT” in ASCII).
1	Enables the write protection if WPKEY corresponds to 0x4D4154 (“MAT” in ASCII).

3. When programming is completed, the bit EEFC_FSR.FRDY rises. If an interrupt has been enabled by setting the bit EEFC_FMR.FRDY, the corresponding interrupt line of the interrupt controller is activated.

Two errors can be detected in EEFC_FSR after this sequence:

- Command Error: A bad keyword has been written in EEFC_FCR.
- Flash Error: At the end of the programming, the WriteVerify test of the Flash memory has failed.

The sequence to erase the user signature area is the following:

1. Execute the 'Erase User Signature' command by writing EEFC_FCR.FCMD with the EUS command. Field EEFC_FCR.FARG is meaningless.
2. When programming is completed, the bit EEFC_FSR.FRDY rises. If an interrupt has been enabled by setting the bit EEFC_FMR.FRDY, the corresponding interrupt line of the interrupt controller is activated.

Two errors can be detected in EEFC_FSR after this sequence:

- Command Error: A bad keyword has been written in EEFC_FCR.
- Flash Error: At the end of the programming, the EraseVerify test of the Flash memory has failed.

22.4.3.10 ECC Errors and Corrections

The Flash embeds an ECC module able to correct one unique error and able to detect two errors. The errors are detected while a read access is performed into memory array and stored in EEFC_FSR (see "EEFC Flash Status Register"). The error report is kept until EEFC_FSR is read.

There is one flag for a unique error on lower half part of the Flash word (64 LSB) and one flag for the upper half part (MSB). The multiple errors are reported in the same way.

Due to the anticipation technique to improve bandwidth throughput on instruction fetch, a reported error can be located in the next sequential Flash word compared to the location of the instruction being executed, which is located in the previously fetched Flash word.

If a software routine processes the error detection independently from the main software routine, the entire Flash located software must be rewritten because there is no storage of the error location.

If only a software routine is running to program and check pages by reading EEFC_FSR, the situation differs from the previous case. Performing a check for ECC unique errors just after page programming completion involves a read of the newly programmed page. This read sequence is viewed as data accesses and is not optimized by the Flash controller. Thus, in case of unique error, only the current page must be reprogrammed.

22.4.4 Register Write Protection

To prevent any single software error from corrupting EEFC behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the "EEFC Write Protection Mode Register" (EEFC_WPMR).

The following register can be write-protected:

- "EEFC Flash Mode Register"

26. Reset Controller (RSTC)

26.1 Description

The Reset Controller (RSTC), driven by Power-On Reset (POR) cells, software, external reset pin and peripheral events, handles all the resets of the system without any external components. It reports which reset occurred last.

The RSTC also drives simultaneously the external reset and the peripheral and processor resets.

26.2 Embedded Characteristics

- Driven by embedded POR, software, external reset pin and peripheral events
- Management of all system resets, including:
  - External devices through the NRST pin
  - Processor
  - Peripheral set
- Reset source status:
  - Status of the last reset
  - Either VDDCORE and VDDIO POR, Software Reset, User Reset, Watchdog Reset
- External reset signal control and shaping

26.3 Block Diagram

Figure 26-1. Reset Controller Block Diagram

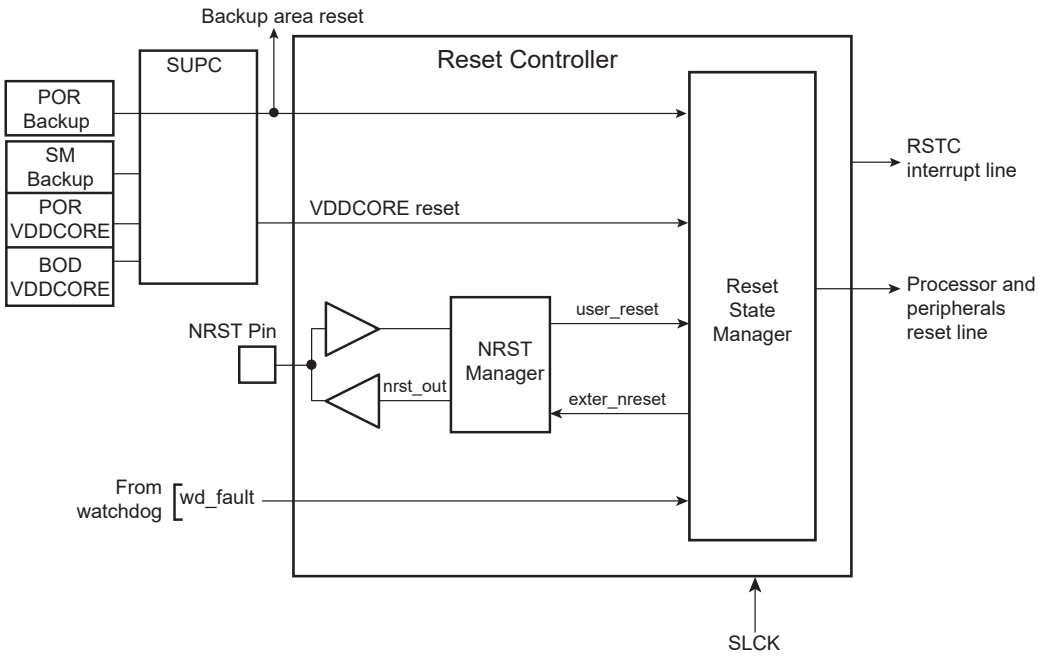
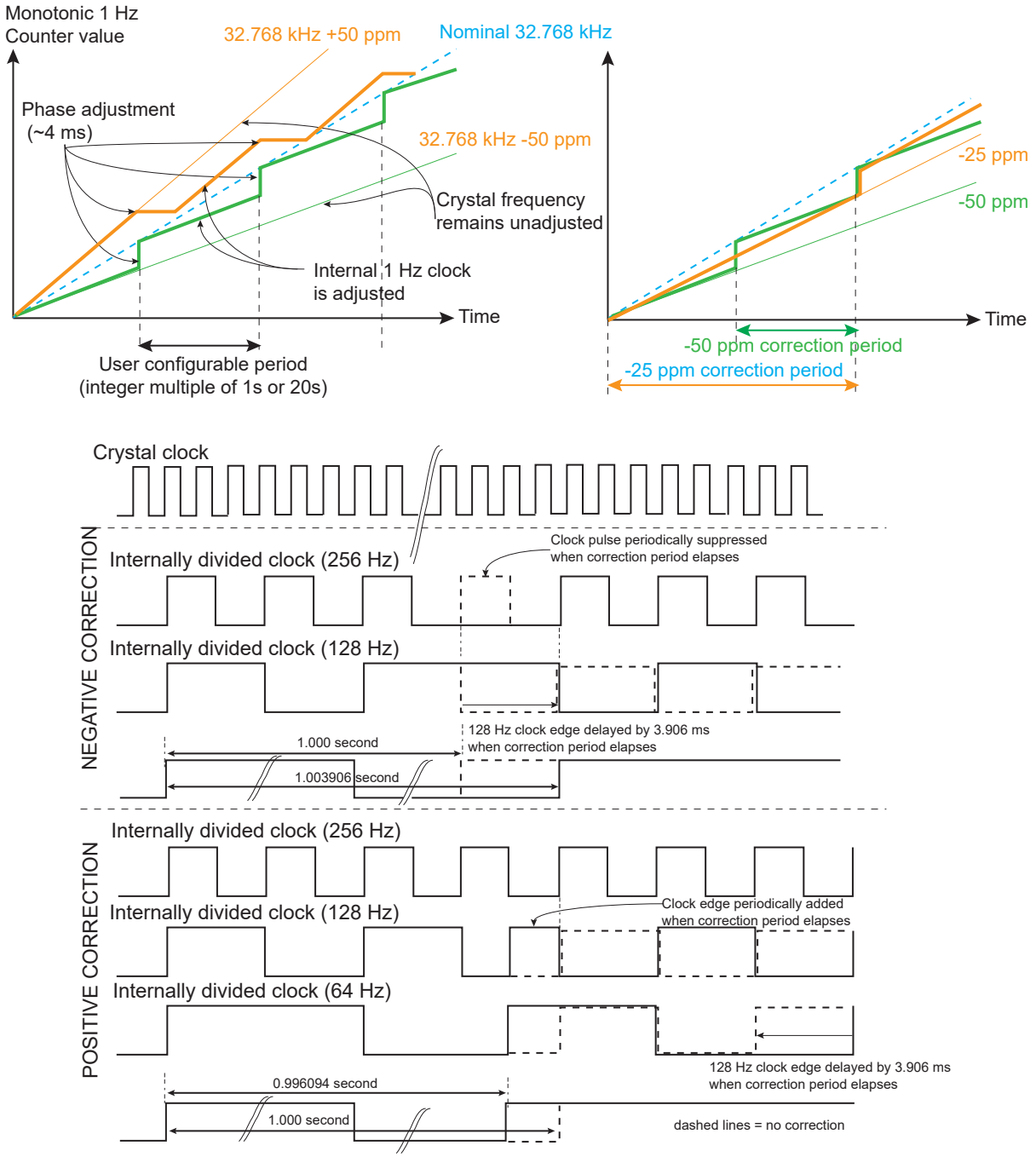


Figure 27-5. Calibration Circuitry Waveforms



The inaccuracy of a crystal oscillator at typical room temperature (±20 ppm at 20–25 °C) can be compensated if a reference clock/signal is used to measure such inaccuracy. This kind of calibration operation can be set up during the final product manufacturing by means of measurement equipment embedding such a reference clock. The correction of value must be programmed into the (RTC_MR), and this value is kept as long as the circuitry is powered (backup area). Removing the backup power supply cancels this calibration. This room temperature calibration can be further processed by means of the networking capability of the target application.

To ease the comparison of the inherent crystal accuracy with the reference clock/signal during manufacturing, an internal prescaled 32.768 kHz clock derivative signal can be assigned to drive RTC

31.20.27 PMC Oscillator Calibration Register

Name: PMC_OCR
Offset: 0x0110
Reset: 0x00404040
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	SEL12	CAL12[6:0]						
Access								
Reset	0	1	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SEL8	CAL8[6:0]						
Access								
Reset	0	1	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SEL4	CAL4[6:0]						
Access								
Reset	0	1	0	0	0	0	0	0

Bit 23 – SEL12 Selection of Main RC Oscillator Calibration Bits for 12 MHz

Value	Description
0	Factory-determined value stored in Flash memory.
1	Value written by user in CAL12 field of this register.

Bits 22:16 – CAL12[6:0] Main RC Oscillator Calibration Bits for 12 MHz
Calibration bits applied to the RC Oscillator when SEL12 is set.

Bit 15 – SEL8 Selection of Main RC Oscillator Calibration Bits for 8 MHz

Value	Description
0	Factory-determined value stored in Flash memory.
1	Value written by user in CAL8 field of this register.

Bits 14:8 – CAL8[6:0] Main RC Oscillator Calibration Bits for 8 MHz
Calibration bits applied to the RC Oscillator when SEL8 is set.

Bit 7 – SEL4 Selection of Main RC Oscillator Calibration Bits for 4 MHz

31.20.28 PMC SleepWalking Enable Register 0

Name: PMC_SLPWK_ER0
Offset: 0x0114
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	PID31	PID30	PID29	PID28	PID27	PID26	PID25	PID24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	PID23	PID22	PID21	PID20	PID19	PID18	PID17	PID16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PID7							
Access								
Reset								

Bits 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – PIDx
Peripheral x SleepWalking Enable
Not all PIDs can be configured with asynchronous partial wake-up.

Only the following PID can be configured with asynchronous partial wake-up: UARTx and TWIHSx.

The clock of the peripheral must be enabled before using its asynchronous partial wake-up (SleepWalking) function (its associated PIDx field in PMC Peripheral Clock Status Register 0 or PMC Peripheral Clock Status Register 1 is set to ‘1’).

Value	Description
0	No effect.
1	The asynchronous partial wakeup (SleepWalking) function of the corresponding peripheral is enabled. **Note:** “PIDx” refers to identifiers as defined in the section “Peripheral Identifiers”

Offset	Name	Bit Pos.								
0x0400	GMAC_ISRPQ1	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x0404	GMAC_ISRPQ2	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x0408	GMAC_ISRPQ3	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x040C	GMAC_ISRPQ4	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x0410	GMAC_ISRPQ5	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x0414 ... 0x043F	Reserved									
0x0440	GMAC_TBQBAPQ1	7:0	TXBQBA[5:0]							
		15:8	TXBQBA[13:6]							
		23:16	TXBQBA[21:14]							
		31:24	TXBQBA[29:22]							
0x0444	GMAC_TBQBAPQ2	7:0	TXBQBA[5:0]							
		15:8	TXBQBA[13:6]							
		23:16	TXBQBA[21:14]							
		31:24	TXBQBA[29:22]							
0x0448	GMAC_TBQBAPQ3	7:0	TXBQBA[5:0]							
		15:8	TXBQBA[13:6]							
		23:16	TXBQBA[21:14]							
		31:24	TXBQBA[29:22]							
0x044C	GMAC_TBQBAPQ4	7:0	TXBQBA[5:0]							
		15:8	TXBQBA[13:6]							
		23:16	TXBQBA[21:14]							
		31:24	TXBQBA[29:22]							
0x0450	GMAC_TBQBAPQ5	7:0	TXBQBA[5:0]							
		15:8	TXBQBA[13:6]							
		23:16	TXBQBA[21:14]							
		31:24	TXBQBA[29:22]							
0x0454 ... 0x047F	Reserved									

Bit 24 – RXCOEN Receive Checksum Offload Enable
Writing a '1' to this bit enables the receive checksum engine, and frames with bad IP, TCP or UDP checksums are discarded.

Bit 23 – DCPF Disable Copy of Pause Frames
Writing a '1' to this bit prevents valid pause frames from being copied to memory. Pause frames are not copied regardless of the state of the Copy All Frames (CAF) bit, whether a hash match is found or whether a type ID match is identified.

If a destination address match is found, the pause frame will be copied to memory. Note that valid pause frames received will still increment pause statistics and pause the transmission of frames, as required.

Bits 22:21 – DBW[1:0] Data Bus Width
Should always be written to '0'.

Value	Name	Description
0	DBW32	32-bit data bus width
1	DBW64	64-bit data bus width

Bits 20:18 – CLK[2:0] MDC Clock Division
These bits must be set according to MCK speed, and determine the number MCK will be divided by to generate Management Data Clock (MDC). For conformance with the 802.3 specification, MDC must not exceed 2.5MHz.

Note: MDC is only active during MDIO read and write operations.

Value	Name	Description
0	MCK_8	MCK divided by 8 (MCK up to 20MHz)
1	MCK_16	MCK divided by 16 (MCK up to 40MHz)
2	MCK_32	MCK divided by 32 (MCK up to 80MHz)
3	MCK_48	MCK divided by 48 (MCK up to 120MHz)
4	MCK_64	MCK divided by 64 (MCK up to 160MHz)
5	MCK_96	MCK divided by 96 (MCK up to 240MHz)

Bit 17 – RFCS Remove FCS
Writing this bit to '1' will cause received frames to be written to memory without their frame check sequence (last 4 bytes). The indicated frame length will be reduced by four bytes in this mode.

Bit 16 – LFERD Length Field Error Frame Discard
Writing a '1' to this bit discards frames with a measured length shorter than the extracted length field (as indicated by bytes 13 and 14 in a non-VLAN tagged frame). This only applies to frames with a length field less than 0x0600.

Bits 15:14 – RXBUFO[1:0] Receive Buffer Offset
These bits determine the number of bytes by which the received data is offset from the start of the receive buffer.

Bit 13 – PEN Pause Enable
When written to '1', transmission will pause if a non-zero 802.3 classic pause frame is received and PFC has not been negotiated.

Offset	Name	Bit Pos.								
0x016C	USBHS_DEVEPTICR3 (ISOENPT)	7:0	SHORTPACKETC	CRCERRIC	OVERFIC	HBISOFLUSHIC	HBISOINERRIC	UNDERFIC	RXOUTIC	TXINIC
		15:8								
		23:16								
		31:24								
0x0170	USBHS_DEVEPTICR4	7:0	SHORTPACKETC	STALLEDIC	OVERFIC	NAKINIC	NAKOUTIC	RXSTPIC	RXOUTIC	TXINIC
		15:8								
		23:16								
		31:24								
0x0170	USBHS_DEVEPTICR4 (ISOENPT)	7:0	SHORTPACKETC	CRCERRIC	OVERFIC	HBISOFLUSHIC	HBISOINERRIC	UNDERFIC	RXOUTIC	TXINIC
		15:8								
		23:16								
		31:24								
0x0174	USBHS_DEVEPTICR5	7:0	SHORTPACKETC	STALLEDIC	OVERFIC	NAKINIC	NAKOUTIC	RXSTPIC	RXOUTIC	TXINIC
		15:8								
		23:16								
		31:24								
0x0174	USBHS_DEVEPTICR5 (ISOENPT)	7:0	SHORTPACKETC	CRCERRIC	OVERFIC	HBISOFLUSHIC	HBISOINERRIC	UNDERFIC	RXOUTIC	TXINIC
		15:8								
		23:16								
		31:24								
0x0178	USBHS_DEVEPTICR6	7:0	SHORTPACKETC	STALLEDIC	OVERFIC	NAKINIC	NAKOUTIC	RXSTPIC	RXOUTIC	TXINIC
		15:8								
		23:16								
		31:24								
0x0178	USBHS_DEVEPTICR6 (ISOENPT)	7:0	SHORTPACKETC	CRCERRIC	OVERFIC	HBISOFLUSHIC	HBISOINERRIC	UNDERFIC	RXOUTIC	TXINIC
		15:8								
		23:16								
		31:24								
0x017C	USBHS_DEVEPTICR7	7:0	SHORTPACKETC	STALLEDIC	OVERFIC	NAKINIC	NAKOUTIC	RXSTPIC	RXOUTIC	TXINIC
		15:8								
		23:16								
		31:24								
0x017C	USBHS_DEVEPTICR7 (ISOENPT)	7:0	SHORTPACKETC	CRCERRIC	OVERFIC	HBISOFLUSHIC	HBISOINERRIC	UNDERFIC	RXOUTIC	TXINIC
		15:8								
		23:16								
		31:24								

Offset	Name	Bit Pos.								
0x0364	USBHS_DEVDMAADDRESS7	7:0	BUFF_ADD[7:0]							
		15:8	BUFF_ADD[15:8]							
		23:16	BUFF_ADD[23:16]							
		31:24	BUFF_ADD[31:24]							
0x0368	USBHS_DEVDMACONTROL7	7:0	BURST_LCK	DESC_LD_IT	END_BUFFIT	END_TR_IT	END_B_EN	END_TR_EN	LDNXT_DSC	CHANN_ENB
		15:8								
		23:16	BUFF_LENGTH[7:0]							
		31:24	BUFF_LENGTH[15:8]							
0x036C	USBHS_DEVDMASTATUS7	7:0		DESC_LDST	END_BF_ST	END_TR_ST			CHANN_ACT	CHANN_ENB
		15:8								
		23:16	BUFF_COUNT[7:0]							
		31:24	BUFF_COUNT[15:8]							
0x0370 ... 0x03FF	Reserved									
0x0400	USBHS_HSTCTRL	7:0								
		15:8			SPDCONF[1:0]			RESUME	RESET	SOFE
		23:16								
		31:24								
0x0404	USBHS_HSTISR	7:0		HWUPI	HSOFI	RXRSMI	RSMEDI	RSTI	DDISCI	DCONNI
		15:8	PEP_7	PEP_6	PEP_5	PEP_4	PEP_3	PEP_2	PEP_1	PEP_0
		23:16							PEP_9	PEP_8
		31:24	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	DMA_0	
0x0408	USBHS_HSTICR	7:0		HWUPIC	HSOFIC	RXRSMIC	RSMEDIC	RSTIC	DDISCIC	DCONNIC
		15:8								
		23:16								
		31:24								
0x040C	USBHS_HSTIFR	7:0		HWUPIS	HSOFIS	RXRSMIS	RSMEDIS	RSTIS	DDISCIS	DCONNIS
		15:8								
		23:16								
		31:24	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	DMA_0	
0x0410	USBHS_HSTIMR	7:0		HWUPIE	HSOFIE	RXRSMIE	RSMEDIE	RSTIE	DDISCIE	DCONNIE
		15:8	PEP_7	PEP_6	PEP_5	PEP_4	PEP_3	PEP_2	PEP_1	PEP_0
		23:16							PEP_9	PEP_8
		31:24	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	DMA_0	
0x0414	USBHS_HSTIDR	7:0		HWUPIEC	HSOFIEC	RXRSMIEC	RSMEDIEC	RSTIEC	DDISCIEC	DCONNIEC
		15:8	PEP_7	PEP_6	PEP_5	PEP_4	PEP_3	PEP_2	PEP_1	PEP_0
		23:16							PEP_9	PEP_8
		31:24	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	DMA_0	
0x0418	USBHS_HSTIER	7:0		HWUPIES	HSOFIES	RXRSMIES	RSMEDIES	RSTIES	DDISCIES	DCONNIES
		15:8	PEP_7	PEP_6	PEP_5	PEP_4	PEP_3	PEP_2	PEP_1	PEP_0
		23:16							PEP_9	PEP_8
		31:24	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	DMA_0	
0x041C	USBHS_HSTPIP	7:0	PEN7	PEN6	PEN5	PEN4	PEN3	PEN2	PEN1	PEN0
		15:8								PEN8
		23:16	PRST7	PRST6	PRST5	PRST4	PRST3	PRST2	PRST1	PRST0

40.14 Register Summary

Offset	Name	Bit Pos.								
0x00	HSMCI_CR	7:0	SWRST				PWSDIS	PWSEN	MCIDIS	MCIEN
		15:8								
		23:16								
		31:24								
0x00	HSMCI_FIFOx [x=0..255]	7:0	DATA[7:0]							
		15:8	DATA[15:8]							
		23:16	DATA[23:16]							
		31:24	DATA[31:24]							
0x04	HSMCI_MR	7:0	CLKDIV[7:0]							
		15:8		PADV	FBYTE	WRPROOF	RDPROOF	PWSDIV[2:0]		
		23:16								CLKODD
		31:24								
0x08	HSMCI_DTOR	7:0		DTOMUL[2:0]			DTOCYC[3:0]			
		15:8								
		23:16								
		31:24								
0x0C	HSMCI_SDCR	7:0	SDCBUS[1:0]						SDCSEL[1:0]	
		15:8								
		23:16								
		31:24								
0x10	HSMCI_ARGR	7:0	ARG[7:0]							
		15:8	ARG[15:8]							
		23:16	ARG[23:16]							
		31:24	ARG[31:24]							
0x14	HSMCI_CMDR	7:0	RSPTYP[1:0]		CMDNB[5:0]					
		15:8				MAXLAT	OPDCMD	SPCMD[2:0]		
		23:16			TRTYP[2:0]			TRDIR	TRCMD[1:0]	
		31:24					BOOT_ACK	ATACS	IOSPCMD[1:0]	
0x18	HSMCI_BLKR	7:0	BCNT[7:0]							
		15:8	BCNT[15:8]							
		23:16	BLKLEN[7:0]							
		31:24	BLKLEN[15:8]							
0x1C	HSMCI_CSTOR	7:0		CSTOMUL[2:0]			CSTOCYC[3:0]			
		15:8								
		23:16								
		31:24								
0x20	HSMCI_RSPR	7:0	RSP[7:0]							
		15:8	RSP[15:8]							
		23:16	RSP[23:16]							
		31:24	RSP[31:24]							
0x24 ... 0x2F	Reserved									

42.7.6 QSPI Interrupt Enable Register

Name: QSPI_IER
Offset: 0x14
Reset: –
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
						INSTRE	CSS	CSR
Access						W	W	W
Reset						–	–	–

Bit	7	6	5	4	3	2	1	0
					OVRES	TXEMPTY	TDRE	RDRF
Access					W	W	W	W
Reset					–	–	–	–

Bit 10 – INSTRE Instruction End Interrupt Enable

Bit 9 – CSS Chip Select Status Interrupt Enable

Bit 8 – CSR Chip Select Rise Interrupt Enable

Bit 3 – OVRES Overrun Error Interrupt Enable

Bit 2 – TXEMPTY Transmission Registers Empty Enable

Bit 1 – TDRE Transmit Data Register Empty Interrupt Enable

Bit 0 – RDRF Receive Data Register Full Interrupt Enable

If no parity error is detected, the I/O line remains at 1 during the guard time and the transmitter can continue with the transmission of the next character, as shown in Figure 46-30.

If a parity error is detected by the receiver, it drives the I/O line to 0 during the guard time, as shown in Figure 46-31. This error bit, NACK, for Non Acknowledge. In this case, the character lasts one additional bit time, as the guard time does not change and is added to the error bit time, which lasts one bit time.

When the USART is the receiver and it detects an error, it does not load the erroneous character in US_RHR. It sets US_SR.PARE so that the software can handle the error.

Figure 46-30. T = 0 Protocol without Parity Error

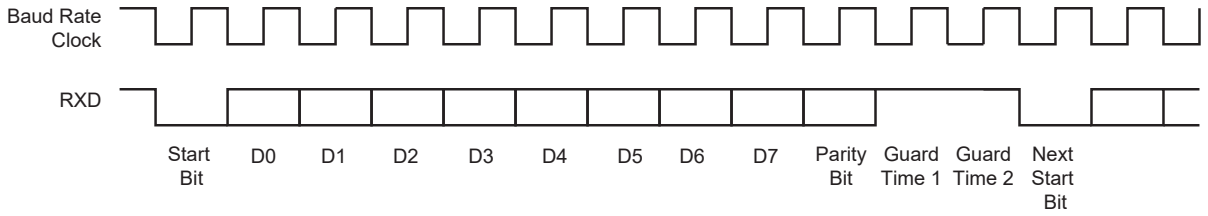
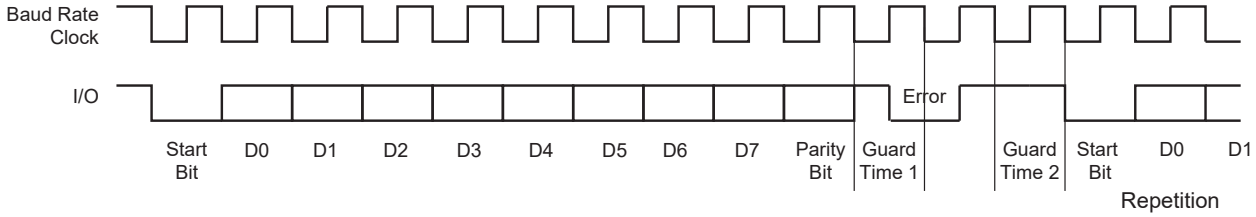


Figure 46-31. T = 0 Protocol with Parity Error



46.6.4.2.1 Receive Error Counter

The USART receiver also records the total number of errors. This can be read in the Number of Errors (US_NER) register. The NB_ERRORS field can record up to 255 errors. Reading US_NER automatically clears the NB_ERRORS field.

46.6.4.2.2 Receive NACK Inhibit

The USART can be configured to inhibit an error. This is done by writing a ‘1’ to US_MR.INACK. In this case, no error signal is driven on the I/O line even if a parity bit is detected.

Moreover, if INACK = 1, the erroneous received character is stored in the Receive Holding register as if no error occurred, and the RXRDY bit rises.

46.6.4.2.3 Transmit Character Repetition

When the USART is transmitting a character and gets a NACK, it can automatically repeat the character before moving on to the next one. Repetition is enabled by writing US_MR.MAX_ITERATION to a value greater than 0. Each character can be transmitted up to eight times; the first transmission plus seven repetitions.

If MAX_ITERATION does not equal zero, the USART repeats the character as many times as the value loaded in MAX_ITERATION.

When the USART repetition number reaches MAX_ITERATION and the last repeated character is not acknowledged, the US_CSR.ITER is set. If the repetition of the character is acknowledged by the receiver, the repetitions are stopped and the iteration counter is cleared.

US_CSR.ITER can be cleared by writing a ‘1’ to US_CR.RSTIT.

46.6.4.2.4 Disable Successive Receive NACK

The receiver can limit the number of successive NACKs sent back to the remote transmitter. This is programmed by setting US_MR.DSNACK. The maximum number of NACKs transmitted is configured in

Field	Description
FCE	Flow Control Enable [2]: 1 = Enabled 0 = Disabled
MFE	Multi-Frame per Sub-buffer Enable[3]: 1 = Enabled 0 = Disabled
rsvd	Reserved. Software writes a zero to all reserved bits when the entry is initialized. The reserved bits are Read-only after initialization.

Notes: 1. When set for synchronous channels, the MT bit forces Rx channels to write zeros into the channel data buffer, and Tx channels to output zeros on the physical interface. When set for asynchronous and control channels, the MT bit causes DMA to halt at a packet boundary. Not valid for isochronous channels.

2. The FCE bit is used by MediaLB isochronous Rx channels only.

3. The MFE bit is used by MediaLB synchronous channels only.

Channel Setup

Data direction in the MLB is in reference to the DBR. Therefore, the data direction of CAT entries corresponding to the same channel is reversed for the HBI CAT and the MediaLB CAT.

For a Tx channel (from the HC to the MediaLB interface):

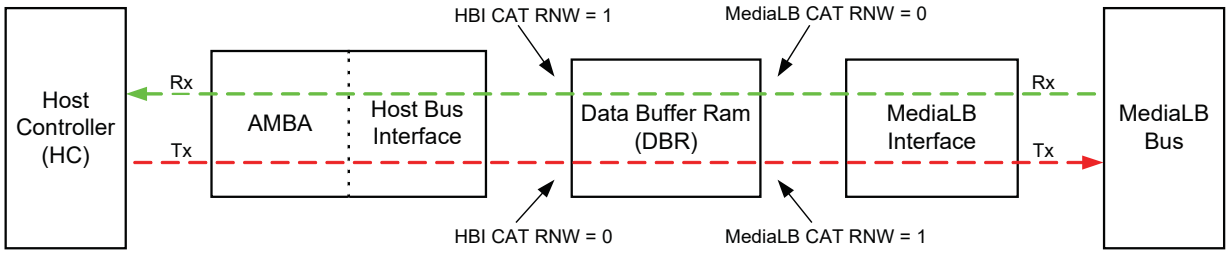
- HBI CAT entry: RNW = 0 (write)
- MediaLB CAT entry: RNW = 1 (read)

Conversely, for a Rx channel (data from MediaLB to HC):

- HBI CAT entry: RNW = 1 (read)
- MediaLB CAT entry: RNW = 0 (write)

The figure below illustrates the directional relationship in the MLB.

Figure 48-16. MLB DBR Directional Relationship



Channel Descriptor Table

The Channel Descriptor Table (CDT) is comprised of 64 CTR entries (addresses 0x00–0x3F), as shown in Table 48-10.

Each 128-bit CDT entry (also referred to as a Channel Descriptor) is referenced by a Connection Label and contains information about a data buffer in the DBR (e.g., buffer size, address pointers).

The format of each CDT entry (also referred to as a Channel Descriptor) depends on the channel type (e.g. synchronous, isochronous, asynchronous, or control).

48.7.15 MIF Data 0 Register

Name: MLB_MDAT0
Offset: 0x0C0
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	DATA[31:24]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DATA[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DATA[31:0] CRT or DBR Data
CTR data - bits[31:0] of 128-bit entry or

DBR data - bits[7:0] of 8-bit entry

48.7.23 MIF Control Register

Name: MLB_MCTL
Offset: 0x0E0
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

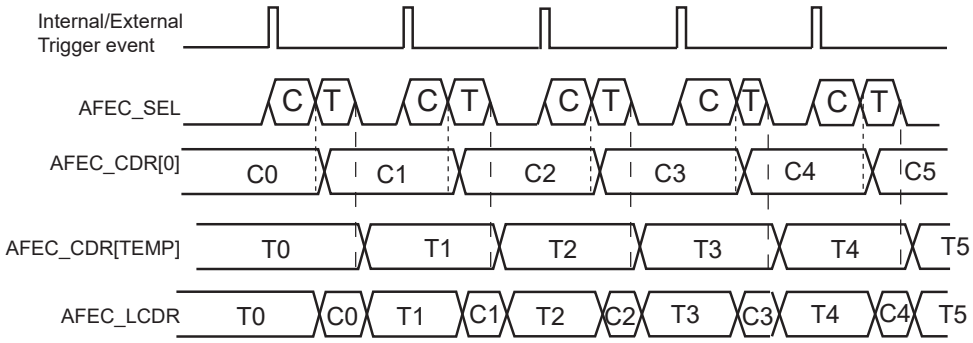
Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								XCMP
Access								
Reset								0

Bit 0 – XCMP Transfer Complete (Write 0 to Clear)

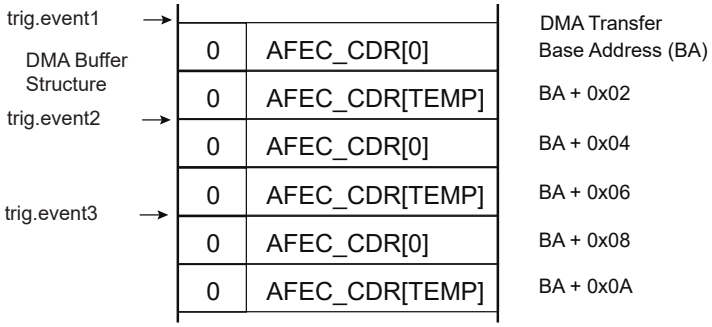
Figure 52-8. Non-Optimized Temperature Conversion

AFEC_CHSR[TEMP] = 1, AFEC_MR.TRGEN = 1 and AFEC_TEMPMR.RTCT = 0



C: Classic AFE Conversion Sequence - T: Temperature Sensor Channel

Assuming AFEC_CHSR[0] = 1 and AFEC_CHSR[TEMP] = 1
where TEMP is the index of the temperature sensor channel



The temperature factor has a slow variation rate and may be different from other conversion channels. As a result, the AFEC allows a different way of triggering temperature measurement when AFEC_TEMPMR.RTCT is set but AFEC_CHSR.CH11 is cleared.

In this configuration, the measurement is triggered every second by means of an internal trigger generated by the RTC. This trigger is always enabled and independent of the triggers used for other channels. It is selected in AFEC_MR.TRGSEL. In this mode of operation, the temperature sensor is only powered for a period of time covering startup time and conversion time.

Every second, a conversion is scheduled for channel 11 but the result of the conversion is only uploaded to an internal register read by means of AFEC_CDR, and not to AFEC_LCDR. Therefore, the temperature channel is not part of the Peripheral DMA Controller buffer; only the enabled channel are kept in the buffer. The end of conversion of the temperature channel is reported by means of the EOC11 flag in AFEC_ISR.

55.6.7 ICM Interrupt Status Register

Name: ICM_ISR
Offset: 0x1C
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
								URAD
Access								R
Reset								0

Bit	23	22	21	20	19	18	17	16
	RSU[3:0]				REC[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RWC[3:0]				RBE[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RDM[3:0]				RHC[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 24 – URAD Undefined Register Access Detection Status
The URAD bit is only reset by the SWRST bit in ICM_CTRL.

The URAT field in ICM_UASR indicates the unspecified access type.

Value	Description
0	No undefined register access has been detected since the last SWRST.
1	At least one undefined register access has been detected since the last SWRST.

Bits 23:20 – RSU[3:0] Region Status Updated Detected
When RSU[i] is set, it indicates that a region status updated condition has been detected.

Bits 19:16 – REC[3:0] Region End Bit Condition Detected
When REC[i] is set, it indicates that an end bit condition has been detected.

Bits 15:12 – RWC[3:0] Region Wrap Condition Detected
When RWC[i] is set, it indicates that a wrap condition has been detected.

Bits 11:8 – RBE[3:0] Region Bus Error
When RBE[i] is set, it indicates that a bus error has been detected while hashing memory region i.