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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsame70q21b-cnt

11. Memories

11.1 Embedded Memories

11.1.1 Internal SRAM

SAM E70/S70/V70/V71 devices embed 384 Kbytes or 256 Kbytes of high-speed SRAM.

The SRAM is accessible over the system Cortex-M bus at address 0x2040 0000.

SAM E70/S70/V70/V71 devices embed a Multi-Port SRAM with four ports to optimize the bandwidth and latency. The priorities, defined in the Bus Matrix for each SRAM port slave are propagated, for each request, up to the SRAM slaves.

The Bus Matrix supports four priority levels: Normal, Bandwidth-sensitive, Latency-sensitive and Latency-critical in order to increase the overall processor performance while securing the high-priority latency-critical requests from the peripherals.

The SRAM controller manages interleaved addressing of SRAM blocks to minimize access latencies. It uses Bus Matrix priorities to give the priority to the most urgent request. The less urgent request is performed no later than the next cycle.

Two SRAM slave ports are dedicated to the Cortex-M7 while two ports are shared by the AHB masters.

11.1.2 Tightly Coupled Memory (TCM) Interface

SAM E70/S70/V70/V71 devices embed Tightly Coupled Memory (TCM) running at processor speed.

- ITCM is a single 64-bit interface, based at 0x0000 0000 (code region).
- DTCM is composed of dual 32-bit interfaces interleaved, based at 0x2000 0000 (data region).

ITCM and DTCM are enabled/disabled in the ITCMR and DTCMR registers in ARM SCB.

DTCM is enabled by default at reset. ITCM is disabled by default at reset.

There are four TCM configurations controlled by software. When enabled, ITCM is located at 0x0000 0000, overlapping ROM or Flash depending on the general-purpose NVM bit 1 (GPNVM). The configuration is done with GPNVM bits [8:7].

Table 11-1. TCM Configurations in Kbytes

ITCM	DTCM	SRAM for 384K RAM-based	SRAM for 256K RAM-based	GPNVM Bits [8:7]
0	0	384	256	0
32	32	320	192	1
64	64	256	128	2
128	128	128	0	3

Accesses made to TCM regions when the relevant TCM is disabled and accesses made to the Code and SRAM region above the TCM size limit are performed on the AHB matrix, i.e., on internal Flash or on ROM depending on remap GPNVM bit.

Accesses made to the SRAM above the size limit will not generate aborts.

The Memory Protection Unit (MPU) can to be used to protect these areas.

22.5.2 EEFC Flash Command Register

Name: EEFC_FCR
Offset: 0x04
Property: Write-only

GETD, GLB, GGPB, STUI, SPUI, GCALB, WUS, EUS, STUS, SPUS, EA	Commands requiring no argument, including Erase all command	FARG is meaningless, must be written with 0
ES	Erase sector command	FARG must be written with any page number within the sector to be erased
EPA	Erase pages command	FARG[1:0] defines the number of pages to be erased The start page must be written in FARG[15:2]. FARG[1:0] = 0: Four pages to be erased. FARG[15:2] = Page_Number / 4 FARG[1:0] = 1: Eight pages to be erased. FARG[15:3] = Page_Number / 8, FARG[2]=0 FARG[1:0] = 2: Sixteen pages to be erased. FARG[15:4] = Page_Number / 16, FARG[3:2]=0 FARG[1:0] = 3: Thirty-two pages to be erased. FARG[15:5] = Page_Number / 32, FARG[4:2]=0 Refer to “EEFC_FCR.FARG Field for EPA Command”.
WP, WPL, EWP, EWPL	Programming commands	FARG must be written with the page number to be programmed
SLB, CLB	Lock bit commands	FARG defines the page number to be locked or unlocked
SGPB, CGPB	GPNVM commands	FARG defines the GPNVM number to be programmed

31.20.21 PMC Write Protection Mode Register

Name: PMC_WPMR
Offset: 0x00E4
Reset: 0x0
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	WPKEY[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	WPKEY[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	WPKEY[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
								WPEN
Access								
Reset								0

Bits 31:8 – WPKEY[23:0] Write Protection Key

Value	Name	Description
0x504D43	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

Bit 0 – WPEN Write Protection Enable
See "Register Write Protection" for the list of registers that can be write-protected.

Value	Description
0	Disables the write protection if WPKEY corresponds to 0x504D43 (“PMC” in ASCII).
1	Enables the write protection if WPKEY corresponds to 0x504D43 (“PMC” in ASCII).

Offset	Name	Bit Pos.								
... 0x2F										
0x30	PIO_SODR	7:0	P7	P6	P5	P4	P3	P2	P1	P0
		15:8	P15	P14	P13	P12	P11	P10	P9	P8
		23:16	P23	P22	P21	P20	P19	P18	P17	P16
		31:24	P31	P30	P29	P28	P27	P26	P25	P24
0x34	PIO_CODR	7:0	P7	P6	P5	P4	P3	P2	P1	P0
		15:8	P15	P14	P13	P12	P11	P10	P9	P8
		23:16	P23	P22	P21	P20	P19	P18	P17	P16
		31:24	P31	P30	P29	P28	P27	P26	P25	P24
0x38	PIO_ODSR	7:0	P7	P6	P5	P4	P3	P2	P1	P0
		15:8	P15	P14	P13	P12	P11	P10	P9	P8
		23:16	P23	P22	P21	P20	P19	P18	P17	P16
		31:24	P31	P30	P29	P28	P27	P26	P25	P24
0x3C	PIO_PDSR	7:0	P7	P6	P5	P4	P3	P2	P1	P0
		15:8	P15	P14	P13	P12	P11	P10	P9	P8
		23:16	P23	P22	P21	P20	P19	P18	P17	P16
		31:24	P31	P30	P29	P28	P27	P26	P25	P24
0x40	PIO_IER	7:0	P7	P6	P5	P4	P3	P2	P1	P0
		15:8	P15	P14	P13	P12	P11	P10	P9	P8
		23:16	P23	P22	P21	P20	P19	P18	P17	P16
		31:24	P31	P30	P29	P28	P27	P26	P25	P24
0x44	PIO_IDR	7:0	P7	P6	P5	P4	P3	P2	P1	P0
		15:8	P15	P14	P13	P12	P11	P10	P9	P8
		23:16	P23	P22	P21	P20	P19	P18	P17	P16
		31:24	P31	P30	P29	P28	P27	P26	P25	P24
0x48	PIO_IMR	7:0	P7	P6	P5	P4	P3	P2	P1	P0
		15:8	P15	P14	P13	P12	P11	P10	P9	P8
		23:16	P23	P22	P21	P20	P19	P18	P17	P16
		31:24	P31	P30	P29	P28	P27	P26	P25	P24
0x4C	PIO_ISR	7:0	P7	P6	P5	P4	P3	P2	P1	P0
		15:8	P15	P14	P13	P12	P11	P10	P9	P8
		23:16	P23	P22	P21	P20	P19	P18	P17	P16
		31:24	P31	P30	P29	P28	P27	P26	P25	P24
0x50	PIO_MDER	7:0	P7	P6	P5	P4	P3	P2	P1	P0
		15:8	P15	P14	P13	P12	P11	P10	P9	P8
		23:16	P23	P22	P21	P20	P19	P18	P17	P16
		31:24	P31	P30	P29	P28	P27	P26	P25	P24
0x54	PIO_MDDR	7:0	P7	P6	P5	P4	P3	P2	P1	P0
		15:8	P15	P14	P13	P12	P11	P10	P9	P8
		23:16	P23	P22	P21	P20	P19	P18	P17	P16
		31:24	P31	P30	P29	P28	P27	P26	P25	P24
0x58	PIO_MDSR	7:0	P7	P6	P5	P4	P3	P2	P1	P0
		15:8	P15	P14	P13	P12	P11	P10	P9	P8
		23:16	P23	P22	P21	P20	P19	P18	P17	P16
		31:24	P31	P30	P29	P28	P27	P26	P25	P24

34.7.12 SDRAMC OCMS KEY1 Register

Name: SDRAMC_OCMS_KEY1
Offset: 0x30
Property: Write-only

Bit	31	30	29	28	27	26	25	24
	KEY1[31:24]							
Access	W	W	W	W	W	W	W	W
Reset								

Bit	23	22	21	20	19	18	17	16
	KEY1[23:16]							
Access	W	W	W	W	W	W	W	W
Reset								

Bit	15	14	13	12	11	10	9	8
	KEY1[15:8]							
Access	W	W	W	W	W	W	W	W
Reset								

Bit	7	6	5	4	3	2	1	0
	KEY1[7:0]							
Access	W	W	W	W	W	W	W	W
Reset								

Bits 31:0 – KEY1[31:0] Off-chip Memory Scrambling (OCMS) Key Part 1
When off-chip memory scrambling is enabled, the data scrambling depends on KEY1 and KEY2 values.

Offset	Name	Bit Pos.								
0x054C	GMAC_ST2RPQ3	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x0550	GMAC_ST2RPQ4	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x0554	GMAC_ST2RPQ5	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x0558	GMAC_ST2RPQ6	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x055C	GMAC_ST2RPQ7	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x0560 ... 0x05FF	Reserved									
0x0600	GMAC_IERPQ1	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x0604	GMAC_IERPQ2	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x0608	GMAC_IERPQ3	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x060C	GMAC_IERPQ4	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x0610	GMAC_IERPQ5	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x0614 ... 0x061F	Reserved									

38.8.15 GMAC Receive Pause Quantum Register

Name: GMAC_RPQ
Offset: 0x038
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RPQ[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RPQ[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – RPQ[15:0] Received Pause Quantum
Stores the current value of the Receive Pause Quantum Register which is decremented every 512 bit times.

38.8.63 GMAC Pause Frames Received Register

Name: GMAC_PFR
Offset: 0x164
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PFRX[15:0] Pause Frames Received Register
This register counts the number of pause frames received without error.

Offset	Name	Bit Pos.								
		31:24								
0x0198	USBHS_DEVEPTIFR2 (ISOENPT)	7:0	SHORTPACKETS	CRCERRIS	OVERFIS	HBISOFLUSHIS	HBISOINERRIS	UNDERFIS	RXOUTIS	TXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x019C	USBHS_DEVEPTIFR3	7:0	SHORTPACKETS	STALLEDIS	OVERFIS	NAKINIS	NAKOUTIS	RXSTPIS	RXOUTIS	TXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x019C	USBHS_DEVEPTIFR3 (ISOENPT)	7:0	SHORTPACKETS	CRCERRIS	OVERFIS	HBISOFLUSHIS	HBISOINERRIS	UNDERFIS	RXOUTIS	TXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x01A0	USBHS_DEVEPTIFR4	7:0	SHORTPACKETS	STALLEDIS	OVERFIS	NAKINIS	NAKOUTIS	RXSTPIS	RXOUTIS	TXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x01A0	USBHS_DEVEPTIFR4 (ISOENPT)	7:0	SHORTPACKETS	CRCERRIS	OVERFIS	HBISOFLUSHIS	HBISOINERRIS	UNDERFIS	RXOUTIS	TXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x01A4	USBHS_DEVEPTIFR5	7:0	SHORTPACKETS	STALLEDIS	OVERFIS	NAKINIS	NAKOUTIS	RXSTPIS	RXOUTIS	TXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x01A4	USBHS_DEVEPTIFR5 (ISOENPT)	7:0	SHORTPACKETS	CRCERRIS	OVERFIS	HBISOFLUSHIS	HBISOINERRIS	UNDERFIS	RXOUTIS	TXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x01A8	USBHS_DEVEPTIFR6	7:0	SHORTPACKETS	STALLEDIS	OVERFIS	NAKINIS	NAKOUTIS	RXSTPIS	RXOUTIS	TXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x01A8	USBHS_DEVEPTIFR6 (ISOENPT)	7:0	SHORTPACKETS	CRCERRIS	OVERFIS	HBISOFLUSHIS	HBISOINERRIS	UNDERFIS	RXOUTIS	TXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								

Bit 1 – RXOUTIC Received OUT Data Interrupt Clear

Bit 0 – TXINIC Transmitted IN Data Interrupt Clear

39.6.64 Host Pipe x Error Register

Name: USBHS_HSTPIPERRx
Offset: 0x0680 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

Writing a zero in a bit/field in this register clears the bit/field. Writing a one has no effect.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
Access								
Reset		0	0	0	0	0	0	0

Bits 6:5 – COUNTER[1:0] Error Counter
This field is incremented each time an error occurs (CRC16, TIMEOUT, PID, DATAPID or DATATGL).

This field is cleared when receiving a USB packet free of error.

When this field reaches 3 (i.e., 3 consecutive errors), this pipe is automatically frozen (USBHS_HSTPIPIMRx.PFREEZE is set).

Bit 4 – CRC16 CRC16 Error

Value	Description
0	No CRC16 error occurred since last clear of this bit.
1	This bit is automatically set when a CRC16 error has been detected.

Bit 3 – TIMEOUT Time-Out Error

Value	Description
0	No Time-Out error occurred since last clear of this bit.
1	This bit is automatically set when a Time-Out error has been detected.

Bit 2 – PID PID Error

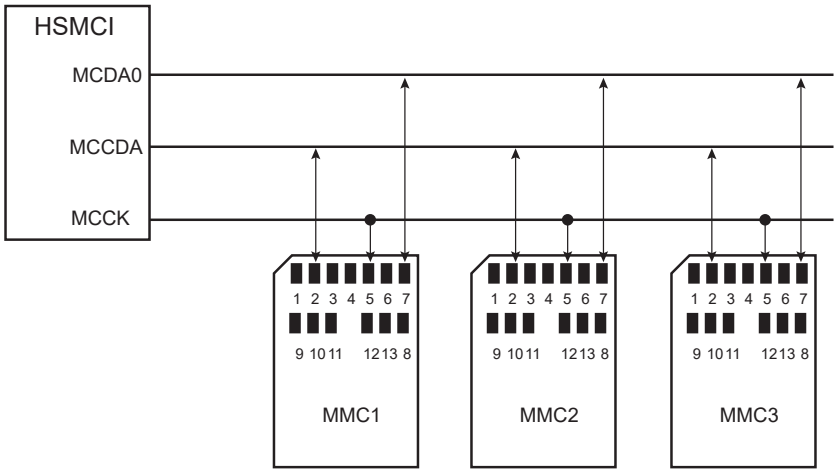
Table 40-2. Bus Topology

Pin Number	Name	Type[1]	Description	HSMCI Pin Name[2] (Slot z)
1	DAT[3]	I/O/PP	Data	MCDz3
2	CMD	I/O/PP/OD	Command/response	MCCDz
3	VSS1	S	Supply voltage ground	VSS
4	VDD	S	Supply voltage	VDD
5	CLK	I/O	Clock	MCCK
6	VSS2	S	Supply voltage ground	VSS
7	DAT[0]	I/O/PP	Data 0	MCDz0
8	DAT[1]	I/O/PP	Data 1	MCDz1
9	DAT[2]	I/O/PP	Data 2	MCDz2

Notes: 1. I: Input, O: Output, PP: Push/Pull, OD: Open Drain, S: Supply

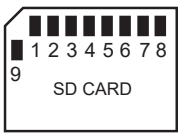
2. When several HSMCI (x HSMCI) are embedded in a product, MCCK refers to HSMCIx_CK, MCCDA to HSMCIx_CDA, MCDAy to HSMCIx_DAy.

Figure 40-4. MMC Bus Connections (One Slot)



Note: When several HSMCI (x HSMCI) are embedded in a product, MCCK refers to HSMCIx_CK, MCCDA to HSMCIx_CDA MCDAy to HSMCIx_DAy.

Figure 40-5. SD Memory Card Bus Topology



The SD Memory Card bus includes the signals listed in Table 1-6.

Bit 20 – RTOE Response Time-out Error Interrupt Enable

Bit 19 – RENDE Response End Bit Error Interrupt Enable

Bit 18 – RCRCE Response CRC Error Interrupt Enable

Bit 17 – RDIRE Response Direction Error Interrupt Enable

Bit 16 – RINDE Response Index Error Interrupt Enable

Bit 13 – CSRCV Completion Signal Received Interrupt Enable

Bit 12 – SDIOWAIT SDIO Read Wait Operation Status Interrupt Enable

Bit 8 – SDIOIRQA SDIO Interrupt for Slot A Interrupt Enable

Bit 5 – NOTBUSY Data Not Busy Interrupt Enable

Bit 4 – DTIP Data Transfer in Progress Interrupt Enable

Bit 3 – BLKE Data Block Ended Interrupt Enable

Bit 2 – TXRDY Transmit Ready Interrupt Enable

Bit 1 – RXRDY Receiver Ready Interrupt Enable

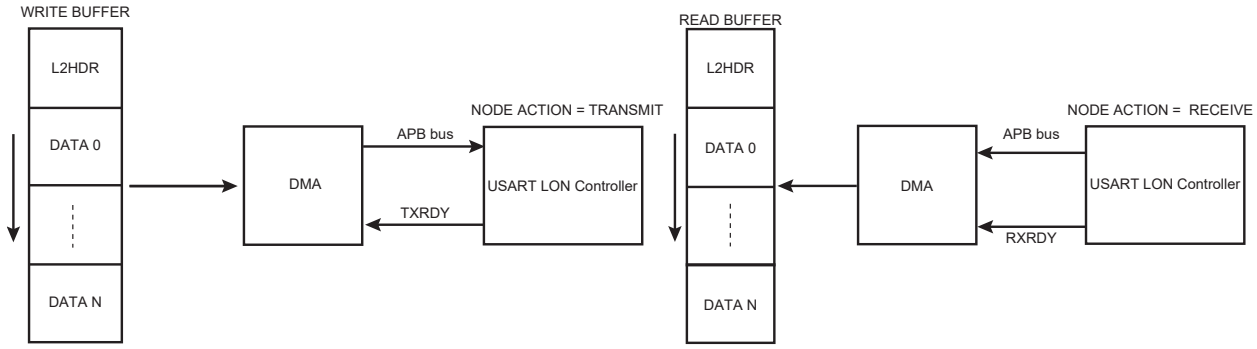
Bit 0 – CMDRDY Command Ready Interrupt Enable

Value	Description
0	The corresponding interrupt is disabled. This bit is cleared when the corresponding bit in I2SC_IDR is written to ’1’.
1	The corresponding interrupt is enabled. This bit is set when the corresponding bit in I2SC_IER is written to ’1’.

Bit 1 – RXRDY Receiver Ready Interrupt Disable

Value	Description
0	The corresponding interrupt is disabled. This bit is cleared when the corresponding bit in I2SC_IDR is written to ’1’.
1	The corresponding interrupt is enabled. This bit is set when the corresponding bit in I2SC_IER is written to ’1’.

Figure 46-64. DMAM = 0



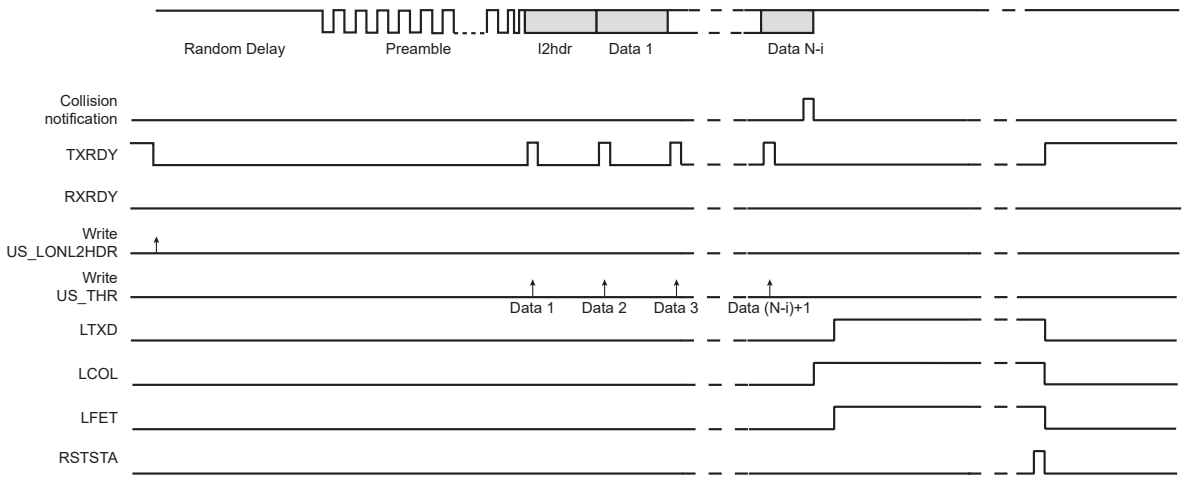
46.6.10.12.2 DMA and Collision Detection

As explained in "comm_type", depending on LON configuration the transmission may be terminated early upon collision notification which means that the DMA transfer may be stopped before its end.

In case of early end of transmission due to collision detection the USART in LON mode acts as follows:

- Send the end of frame trigger.
- Hold down TXRDY avoiding thus any additional DMA transfer.
- Set LTXD, LCOL and LFET flags in US_CSR.
- Wait that the application reconfigure the DMA.
- Wait until LCOL and LFET flags are cleared through US_CR. RSTSTA (it releases the TXRDY signal).

Figure 46-65. DMA, Collision and Early Frame Termination



46.6.11 Test Modes

The USART can be programmed to operate in three different test modes. The internal loopback capability allows on-board diagnostics. In Loopback mode, the USART interface pins are disconnected or not and reconfigured for loopback internally or externally.

46.6.11.1 Normal Mode

Normal mode connects the RXD pin on the receiver input and the transmitter output on the TXD pin.

Bits 15:2 – F1SA[13:0] Receive FIFO 1 Start Address
Start address of Receive FIFO 1 in Message RAM (32-bit word address, see Message RAM Configuration).

Write F1SA with the bits [15:2] of the 32-bit address.

50.7.10 TC Interrupt Status Register

Name: TC_SRx
Offset: 0x20 + x*0x40 [x=0..2]
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
						MTIOB	MTIOA	CLKSTA
Access						R	R	R
Reset						0	0	0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 18 – MTIOB TIOBx Mirror

Value	Description
0	TIOBx is low. If TC_CMRx.WAVE = 0, TIOBx pin is low. If TC_CMRx.WAVE = 1, TIOBx is driven low.
1	TIOBx is high. If TC_CMRx.WAVE = 0, TIOBx pin is high. If TC_CMRx.WAVE = 1, TIOBx is driven high.

Bit 17 – MTIOA TIOAx Mirror

Value	Description
0	TIOAx is low. If TC_CMRx.WAVE = 0, TIOAx pin is low. If TC_CMRx.WAVE = 1, TIOAx is driven low.
1	TIOAx is high. If TC_CMRx.WAVE = 0, TIOAx pin is high. If TC_CMRx.WAVE = 1, TIOAx is driven high.

Bit 16 – CLKSTA Clock Enabling Status

Value	Description
0	Clock is disabled.
1	Clock is enabled.

51.7.29 PWM Event Line x Mode Register

Name: PWM_ELMRx
Offset: 0x7C + x*0x04 [x=0..1]
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	CSEL7	CSEL6	CSEL5	CSEL4	CSEL3	CSEL2	CSEL1	CSEL0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7 – CSELy Comparison y Selection

Value	Description
0	A pulse is not generated on the event line x when the comparison y matches.
1	A pulse is generated on the event line x when the comparison y match.

Figure 58-27. USART SPI Slave Mode (Mode 1 or 2)

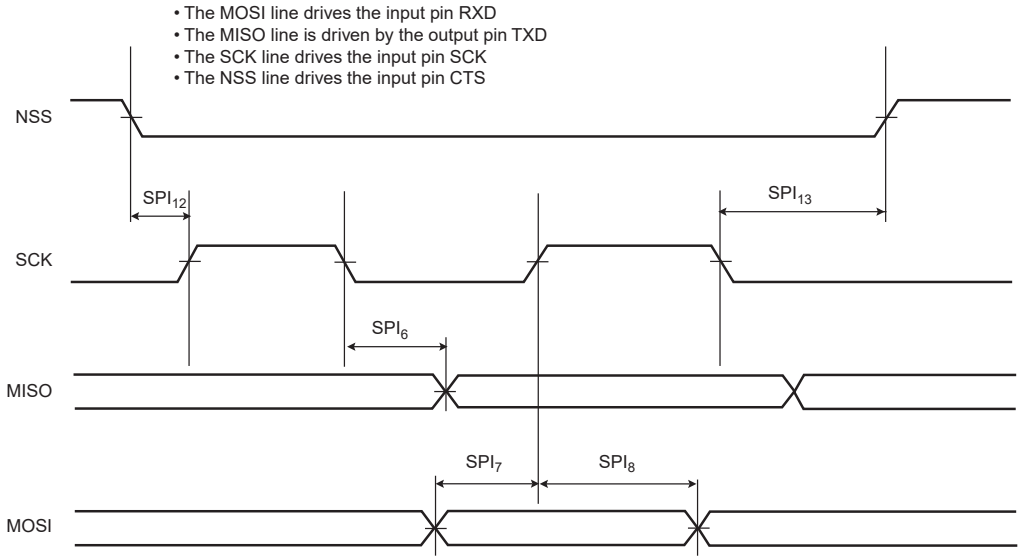
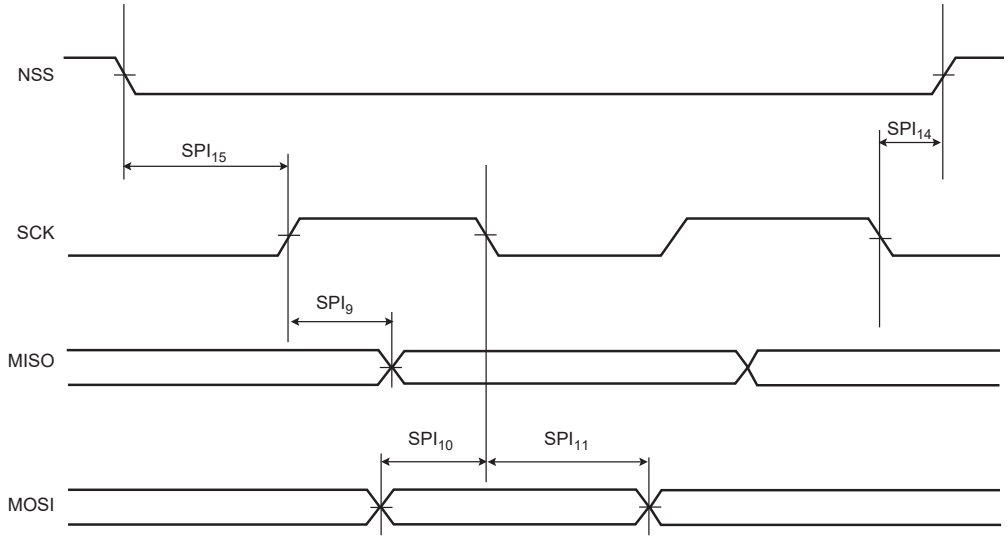


Figure 58-28. USART SPI Slave Mode (Mode 0 or 3)



58.13.1.11.1 USART SPI TImings

Timings are given in the following domains:

- 1.8V domain: VDDIO from 1.7V to 1.95V, maximum external capacitor = 20 pF
- 3.3V domain: VDDIO from 2.85V to 3.6V, maximum external capacitor = 40 pF

Table 58-66. USART SPI Timings

Symbol	Parameter	Conditions	Min	Max	Unit
Master Mode					
SPI_0	SCK Period	1.8V domain 3.3V domain	MCK/6	–	ns
SPI_1	Input Data Setup Time	1.8V domain 3.3V domain	2.8 2.5	–	ns

Date	Changes
	Section 39.6.3.9 ”Priority Queueing in the DMA”: added Table 39-5 “Queue Size” and updated queue sizes. Section 39.6.15 ”Time Stamp Unit”: changed pin reference from “TIOB11/PD22” to “TIOA11/PD21”. Section 39.6.18 ”Energy-efficient Ethernet Support”: removed all references to Gigabit Ethernet. Updated Section 39.6.19 ”802.1Qav Support - Credit-based Shaping”: added definitions of portTransmitRate and IdleSlope; updated content on queue priority management. Section 39.6.20 ”LPI Operation in the GMAC”: Updated steps for transmit and receive paths. Section 39.8.1 ”GMAC Network Control Register” changed description of NRTSM bit. Section 39.8.107 ”GMAC Received LPI Time” and Section 39.8.109 ”GMAC Transmit LPI Time”: corrected ‘PCLK’ to ‘MCK” in field description. Section 39.8.115 ”GMAC Credit-Based Shaping IdleSlope Register for Queue A” and Section 39.8.116 ”GMAC Credit-Based Shaping IdleSlope Register for Queue B”: updated example for calculation of IdleSlope.
	Section 41. ”Serial Peripheral Interface (SPI)” Section 41.7.4 ”SPI Slave Mode”: added paragraph on SFERR flag. Updated Section 41.7.5 ”Register Write Protection”. Section 41.8.1 ”SPI Control Register”: below register table, added “This register can only be written if the WPCREN bit is cleared in the SPI Write Protection Mode Register.” Section 41.8.6 ”SPI Interrupt Enable Register”, Section 41.8.7 ”SPI Interrupt Disable Register”: below each register table, added “This register can only be written if the WPITEN bit is cleared in the SPI Write Protection Mode Register.” Section 41.8.5 ”SPI Status Register”: added bit SFERR at index 12 and bit description. Section 41.8.10 ”SPI Write Protection Mode Register”: added bit WPITEN at index 1 and bit description. Added bit WPCREN at index 2 and bit description.
12-Oct-16	Section 42. ”Quad Serial Peripheral Interface (QSPI)” Section 42.1 ”Description”: added Note on device support. Section 42.6.5 ”QSPI Serial Memory Mode”: updated text on data transfer constraint. Figure 42-9 “Instruction Transmission Flow Diagram”: corrected typos: --- “Wait for flag QSPI_SR.INSTRE ... “ (was “QSPI_CR“) --- “Wait for flag QSPI_SR.CSR ... “ (was “QSPI_CR“) - Added new instruction: “Read QSPI_SR (dummy read) to clear QSPI_SR.INSTRE and QSPI_SR.CSR“. Updated Figure 42-8 “Instruction Frame”, Figure 42-10 “Continuous Read Mode”, Figure 42-16 “Instruction Transmission Waveform 6”, Figure 42-17 “Instruction Transmission Waveform 7” and Figure 42-19 “Instruction Transmission Waveform 9”.