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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	I²C, IrDA, LINbus, SPI, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	44
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 5x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70j19a-ant

11.1.3 Internal ROM

The SAM E70/S70/V70/V71 embeds an Internal ROM for the SAM Boot Assistant (SAM-BA®), In Application Programming functions (IAP) and Fast Flash Programming Interface (FFPI).

At any time, the ROM is mapped at address 0x0080 0000.

The ROM may also be mapped at 0x00000000 depending on GPNVM bit setting and ITCM use.

11.1.4 Backup SRAM

The SAM E70/S70/V70/V71 embeds 1 Kbytes of backup SRAM located at 0x4007 4000.

The backup SRAM is accessible in 32-bit words only. Byte or half-word accesses are not supported.

The backup SRAM is supplied by VDDCORE in Normal mode.

In Backup mode, the backup SRAM supply is automatically switched to VDDIO through the backup SRAM power switch when VDDCORE falls. For more details, see the “Backup SRAM Power Switch” section.

11.1.5 Flash Memories

SAM E70/S70/V70/V71 devices embed 512 Kbytes, 1024 Kbytes or 2084 Kbytes of internal Flash mapped at address 0x40 0000.

The devices feature a Quad SPI (QSPI) interface, mapped at address 0x80000000, that extends the Flash size by adding an external SPI or QSPI Flash.

When accessed by the Cortex-M7 processor for programming operations, the QSPI and internal Flash address spaces must be defined in the Cortex-M7 memory protection unit (MPU) with the attribute 'Device' or 'Strongly Ordered'. For fetch or read operations, the attribute ‘Normal memory’ must be set to benefit from the internal cache. Refer to the ARM Cortex-M7 Technical Reference Manual (ARM DDI 0489) available on www.arm.com.

Some precautions must be taken when the accesses are performed by the central DMA. Refer to 22. Enhanced Embedded Flash Controller (EEFC) and 42. Quad Serial Peripheral Interface (QSPI).

11.1.5.1 Embedded Flash Overview

The memory is organized in sectors. Each sector has a size of 128 Kbytes. The first sector is divided into 3 smaller sectors.

The three smaller sectors are organized in 2 sectors of 8 Kbytes and 1 sector of 112 Kbytes. Refer to the figure below.

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Description
45	UART3	X	X	Universal Asynchronous Receiver/ Transmitter
46	UART4	X	X	Universal Asynchronous Receiver/ Transmitter
47	TC2_CHANNEL0	X	X	16-bit Timer Counter 2, Channel 0
48	TC2_CHANNEL1	X	X	16-bit Timer Counter 2, Channel 1
49	TC2_CHANNEL2	X	X	16-bit Timer Counter 2, Channel 2
50	TC3_CHANNEL0	X	X	16-bit Timer Counter 3, Channel 0
51	TC3_CHANNEL1	X	X	16-bit Timer Counter 3, Channel 1
52	TC3_CHANNEL2	X	X	16-bit Timer Counter 3, Channel 2
53	–	–	–	Reserved
54	–	–	–	Reserved
55	–	–	–	Reserved
53	MLB	X	X	MediaLB IRQ 0
54	MLB	X	–	MediaLB IRQ 1
55	–	X	–	Reserved
56	AES	X	X	Advanced Encryption Standard
57	TRNG	X	X	True Random Number Generator
58	XDMAC	X	X	DMA Controller
59	ISI	X	X	Image Sensor Interface
60	PWM1	X	X	Pulse Width Modulation Controller
61	ARM	FPU	–	ARM Floating Point Unit interrupt associated with OFC, UFC, IOC, DZC and IDC bits
62	SDRAMC	X	–	SDRAM Controller
63	RSWDT	X	–	Reinforced Safety Watchdog Timer
64	ARM	CCW	–	ARM Cache ECC Warning
65	ARM	CCF	–	ARM Cache ECC Fault
66	GMAC	Q1	–	GMAC Queue 1 Interrupt signal toggled on a DMA write to the first word of each DMA data buffer associated with queue 1

1. Round-robin Arbitration (default)
2. Fixed Priority Arbitration

Each algorithm may be complemented by selecting a default master configuration for each slave.

When re-arbitration is required, specific conditions apply. Refer to the "Arbitration Rules" section.

19.3.3.1 Arbitration Rules

Each arbiter has the ability to arbitrate between requests from two or more masters. To avoid burst breaking and to provide maximum throughput for slave interfaces, arbitration should take place during the following cycles:

- Idle cycles: When a slave is not connected to any master or is connected to a master which is not currently accessing it
- Single cycles: When a slave is performing a single access
- End of Burst cycles: When the current cycle is the last cycle of a burst transfer. For a defined length burst, predicted end of burst matches the size of the transfer but is managed differently for undefined length burst. Refer to the "Undefined Length Burst Arbitration" section.
- Slot cycle limit: When the slot cycle counter has reached the limit value indicating that the current master access is too long and must be broken. Refer to the "Slot Cycle Limit Arbitration" section.

19.3.3.1.1 Undefined Length Burst Arbitration

In order to prevent slave handling during undefined length bursts, the user can trigger the re-arbitration before the end of the incremental bursts. The re-arbitration period can be selected from the following Undefined Length Burst Type (ULBT) possibilities:

1. Unlimited: no predetermined end of burst is generated. This value enables 1-Kbyte burst lengths.
2. 1-beat bursts: predetermined end of burst is generated at each single transfer during the INCR transfer.
3. 4-beat bursts: predetermined end of burst is generated at the end of each 4-beat boundary during INCR transfer.
4. 8-beat bursts: predetermined end of burst is generated at the end of each 8-beat boundary during INCR transfer.
5. 16-beat bursts: predetermined end of burst is generated at the end of each 16-beat boundary during INCR transfer.
6. 32-beat bursts: predetermined end of burst is generated at the end of each 32-beat boundary during INCR transfer.
7. 64-beat bursts: predetermined end of burst is generated at the end of each 64-beat boundary during INCR transfer.
8. 128-beat bursts: predetermined end of burst is generated at the end of each 128-beat boundary during INCR transfer.

The use of undefined length16-beat bursts, or less, is discouraged since this decreases the overall bus bandwidth due to arbitration and slave latencies at each first access of a burst.

If the master does not permanently and continuously request the same slave or has an intrinsically limited average throughput, the ULBT should be left at its default unlimited value, knowing that the AHB specification natively limits all word bursts to 256 beats and double-word bursts to 128 beats because of its 1-Kbyte address boundaries.

Unless duly needed, the ULBT should be left at its default value of 0 for power saving.

This selection is made through the ULBT field of the Master Configuration Registers (MATRIX_MCFG).

31.20.23 PMC Peripheral Clock Enable Register 1

Name: PMC_PCER1
Offset: 0x0100
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
		PID62		PID60	PID59	PID58	PID57	PID56
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
			PID53	PID52	PID51	PID50	PID49	PID48
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	PID47	PID46	PID45	PID44	PID43	PID42	PID41	PID40
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	PID39		PID37		PID35	PID34	PID33	PID32
Access								
Reset								

Bits 0:3,5,7:28,30 – PID Peripheral Clock x Disable

Value	Description
0	No effect.
1	Disables the corresponding peripheral clock.

has been used. It re-initializes to the receive buffer queue base address if any descriptor has its wrap bit set.

As receive AHB buffers are used, the receive AHB buffer manager sets bit zero of the first word of the descriptor to logic one indicating the AHB buffer has been used.

Software should search through the “used” bits in the AHB buffer descriptors to find out how many frames have been received, checking the start of frame and end of frame bits.

When the DMA is configured in the packet buffer Partial Store And Forward mode, received frames are written out to the AHB buffers as soon as enough frame data exists in the packet buffer. For both cases, this may mean several full AHB buffers are used before some error conditions can be detected. If a receive error is detected the receive buffer currently being written will be recovered. Previous buffers will not be recovered. As an example, when receiving frames with cyclic redundancy check (CRC) errors or excessive length, it is possible that a frame fragment might be stored in a sequence of AHB receive buffers. Software can detect this by looking for start of frame bit set in a buffer following a buffer with no end of frame bit set.

To function properly, a 10/100 Ethernet system should have no excessive length frames or frames greater than 128 Bytes with CRC errors. Collision fragments will be less than 128 Bytes long, therefore it will be a rare occurrence to find a frame fragment in a receive AHB buffer, when using the default value of 128 Bytes for the receive buffers size.

When in packet buffer full store and forward mode, only good received frames are written out of the DMA, so no fragments will exist in the AHB buffers due to MAC receiver errors. There is still the possibility of fragments due to DMA errors, for example used bit read on the second buffer of a multi-buffer frame.

If bit zero of the receive buffer descriptor is already set when the receive buffer manager reads the location of the receive AHB buffer, the buffer has been already used and cannot be used again until software has processed the frame and cleared bit zero. In this case, the “buffer not available” bit in the receive status register is set and an interrupt triggered. The receive resource error statistics register is also incremented.

When the DMA is configured in the packet buffer full store and forward mode, the user can optionally select whether received frames should be automatically discarded when no AHB buffer resource is available. This feature is selected via the DMA Discard Receive Packets bit in the DMA Configuration register (GMAC_DCFGR.DDRP). By default, the received frames are not automatically discarded. If this feature is off, then received packets will remain to be stored in the SRAM-based packet buffer until AHB buffer resource next becomes available. This may lead to an eventual packet buffer overflow if packets continue to be received when bit zero (used bit) of the receive buffer descriptor remains set.
Note: After a used bit has been read, the receive buffer manager will re-read the location of the receive buffer descriptor every time a new packet is received. When the DMA is not configured in the packet buffer full store and forward mode and a used bit is read, the frame currently being received will be automatically discarded.

When the DMA is configured in the packet buffer full store and forward mode, a receive overrun condition occurs when the receive SRAM-based packet buffer is full, or because HRESP was not OK. In all other modes, a receive overrun condition occurs when either the AHB bus was not granted quickly enough, or because HRESP was not OK, or because a new frame has been detected by the receive block, but the status update or write back for the previous frame has not yet finished. For a receive overrun condition, the receive overrun interrupt is asserted and the buffer currently being written is recovered. The next frame that is received whose address is recognized reuses the buffer.

Value	Description
0	Normal operation
1	All received frames' CRC is replaced with a time stamp.

Bit 12 – TXZQPF Transmit Zero Quantum Pause Frame
Writing a '1' to this bit causes a pause frame with zero quantum to be transmitted.

Writing a '0' to this bit has no effect.

Bit 11 – TXPF Transmit Pause Frame
Writing one to this bit causes a pause frame to be transmitted.

Writing a '0' to this bit has no effect.

Bit 10 – THALT Transmit Halt
Writing a '1' to this bit halts transmission as soon as any ongoing frame transmission ends.

Writing a '0' to this bit has no effect.

Bit 9 – TSTART Start Transmission
Writing a '1' to this bit starts transmission.

Writing a '0' to this bit has no effect.

Bit 8 – BP Back Pressure
In 10M or 100M half duplex mode, writing a '1' to this bit forces collisions on all received frames. Ignored in gigabit half duplex mode.

Value	Description
0	Frame collisions are not forced.
1	Frame collisions are forced in 10M and 100M half duplex mode.

Bit 7 – WESTAT Write Enable for Statistics Registers
Writing a '1' to this bit makes the statistics registers writable for functional test purposes.

Value	Description
0	Statistics Registers are write-protected.
1	Statistics Registers are write-enabled.

Bit 6 – INCSTAT Increment Statistics Registers
Writing a '1' to this bit increments all Statistics Registers by one for test purposes.

Writing a '0' to this bit has no effect.

This bit will always read '0'.

Bit 5 – CLRSTAT Clear Statistics Registers
Writing a '1' to this bit clears the Statistics Registers.

Writing a '0' to this bit has no effect.

This bit will always read '0'.

Bit 4 – MPE Management Port Enable
Writing a '1' to this bit enables the Management Port.

38.8.12 GMAC Interrupt Disable Register

Name: GMAC_IDR
Offset: 0x02C
Reset: –
Property: Write-only

This register is write-only and will always return zero.

The following values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
Access			W	W	R	W	W	W
Reset			–	–	–	–	–	–

Bit	23	22	21	20	19	18	17	16
	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
Access	W	W	W	W	W	W		
Reset	–	–	–	–	–	–		

Bit	15	14	13	12	11	10	9	8
	EXINT	PFTR	PTZ	PFNZ	HRESP	ROVR		
Access	W	W	W	W	W	W		
Reset	–	–	–	–	–	–		

Bit	7	6	5	4	3	2	1	0
	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bit 29 – TSUTIMCMP TSU Timer Comparison

Bit 28 – WOL Wake On LAN

Bit 27 – RXLPISBC Receive LPI indication Status Bit Change
Receive LPI indication status bit change.

Cleared on read.

Bit 26 – SRI TSU Seconds Register Increment

Bit 25 – PDRSFT PDelay Response Frame Transmitted

Bit 24 – PDRQFT PDelay Request Frame Transmitted

Bit 23 – PDRSFR PDelay Response Frame Received

38.8.22 GMAC Specific Address n Bottom Register

Name: GMAC_SABx
Offset: 0x88 + x*0x08 [x=0..3]
Reset: 0x00000000
Property: Read/Write

The addresses stored in the Specific Address Registers are deactivated at reset or when their corresponding Specific Address Register Bottom is written. They are activated when Specific Address Register Top is written.

Bit	31	30	29	28	27	26	25	24
	ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ADDR[31:0] Specific Address n
Least significant 32 bits of the destination address, that is, bits 31:0. Bit zero indicates whether the address is multicast or unicast and corresponds to the least significant bit of the first byte received.

38.8.82 GMAC UDP Checksum Errors Register

Name: GMAC_UCE
Offset: 0x1B0
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	UCKER[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – UCKER[7:0] UDP Checksum Errors
This register counts the number of frames discarded due to an incorrect UDP checksum, but are between 64 and 1518 Bytes (1536 Bytes if GMAC_NCFGR.MAXFS=1) and do not have a CRC error, an alignment error, nor a symbol error.

Bits 23:19 – COMPB[4:0] Index of Screening Type 2 Compare Word 0/Word 1 register x
COMPB is a pointer to the compare registers GMAC_ST2CW0x and GMAC_ST2CW1x. When COMPBE=1, the compare is true if the data at the frame offset ANDed with the value MASKVAL is equal to the value of COMPVAL ANDed with the value of MASKVAL.

Bit 18 – COMPAE Compare A Enable

Value	Description
0	Compare A is disabled.
1	Comparison via the register designated by index COMPA is enabled.

Bits 17:13 – COMPA[4:0] Index of Screening Type 2 Compare Word 0/Word 1 register x
COMPA is a pointer to the compare registers GMAC_ST2CW0x and GMAC_ST2CW1x. When COMPAE=1, the compare is true if the data at the frame offset ANDed with the value MASKVAL is equal to the value of COMPVAL ANDed with the value of MASKVAL.

Bit 12 – ETHE EtherType Enable

Value	Description
0	EtherType match is disabled
1	EtherType match with bits [15:0] of the register designated by the value in I2ETH is enabled

Bits 11:9 – I2ETH[2:0] Index of Screening Type 2 EtherType register x
When EtherType is enabled (ETHE=1), the EtherType field (last EtherType in the header if the frame is VLAN-tagged) is compared with bits [15:0] in the register designated by the value of this bit field.

Bit 8 – VLANE VLAN Enable

Value	Description
0	VLAN match disabled
1	VLAN match is enabled

Bits 6:4 – VLANP[2:0] VLAN Priority
When VLAN match is enabled (VLANE=1), the VLAN Priority field of the received frame is matched against the value of this bit field.

Bits 2:0 – QNB[2:0] Queue Number
If a match is successful, then the queue value programmed in QNB is allocated to the frame.

Bit 9 – DATAXES DataX Interrupt Enable

Bit 8 – MDATAES MData Interrupt Enable

Bit 7 – SHORTPACKETES Short Packet Interrupt Enable

Bit 6 – CRCERRES CRC Error Interrupt Enable

Bit 5 – OVERFES Overflow Interrupt Enable

Bit 4 – HBISOFLUSHES High Bandwidth Isochronous IN Flush Interrupt Enable

Bit 3 – HBISOINERRES High Bandwidth Isochronous IN Error Interrupt Enable

Bit 2 – UNDERFES Underflow Interrupt Enable

Bit 1 – RXOUTES Received OUT Data Interrupt Enable

Bit 0 – TXINES Transmitted IN Data Interrupt Enable

39.6.27 Device DMA Channel x Next Descriptor Address Register

Name: USBHS_DEVDMANXTDSCx
Offset: 0x0300 + x*0x10 [x=0..6]
Reset: 0
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	NXT_DSC_ADD[31:24]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NXT_DSC_ADD[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NXT_DSC_ADD[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NXT_DSC_ADD[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NXT_DSC_ADD[31:0] Next Descriptor Address
This field points to the next channel descriptor to be processed. This channel descriptor must be aligned, so bits 0 to 3 of the address must be equal to zero.

Bit 5 – OVERFIEC Overflow Interrupt Disable

Bit 4 – NAKEDEC NAKed Interrupt Disable

Bit 3 – PERREC Pipe Error Interrupt Disable

Bit 2 – UNDERFIEC Underflow Interrupt Disable

Bit 1 – TXOUTEC Transmitted OUT Data Interrupt Disable

Bit 0 – RXINEC Received IN Data Interrupt Disable

44.9.8 SSC Transmit Holding Register

Name: SSC_THR
Offset: 0x24
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
	TDAT[31:24]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TDAT[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TDAT[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TDAT[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bits 31:0 – TDAT[31:0] Transmit Data
Right aligned regardless of the number of data bits defined by DATLEN in SSC_TFMR.

Value	Name	Description
2	DOMINANT	Dominant (‘0’) level at pin CANTX.
3	RECESSIVE	Recessive (‘1’) at pin CANTX.

Bit 4 – LBCK Loop Back Mode (read/write)
0 (DISABLED): Reset value. Loop Back mode is disabled.

1 (ENABLED): Loop Back mode is enabled (see Test Modes).

51.7.30 PWM Spread Spectrum Register

Name: PWM_SSPR
Offset: 0xA0
Reset: 0x00000000
Property: Read/Write

This register can only be written if bits WPSWS3 and WPHWS3 are cleared in the PWM Write Protection Status Register.

Only the first 16 bits (channel counter size) are significant.

Bit	31	30	29	28	27	26	25	24
								SPRDM
Access								R/W
Reset								0

Bit	23	22	21	20	19	18	17	16
	SPRD[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SPRD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SPRD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 24 – SPRDM Spread Spectrum Counter Mode

Value	Description
0	Triangular mode. The spread spectrum counter starts to count from -SPRD when the channel 0 is enabled and counts upwards at each PWM period. When it reaches +SPRD, it restarts to count from -SPRD again.
1	Random mode. The spread spectrum counter is loaded with a new random value at each PWM period. This random value is uniformly distributed and is between -SPRD and +SPRD.

Bits 23:0 – SPRD[23:0] Spread Spectrum Limit Value
The spread spectrum limit value defines the range for the spread spectrum counter. It is introduced in order to achieve constant varying PWM period for the output waveform.

Bits 11:8 – RBE[3:0] Region Bus Error Interrupt Disable

Value	Description
0	No effect.
1	When RBE[i] is set to one, the Region i Bus Error interrupt is disabled.

Bits 7:4 – RDM[3:0] Region Digest Mismatch Interrupt Disable

Value	Description
0	No effect.
1	When RDM[i] is set to one, the Region i Digest Mismatch interrupt is disabled.

Bits 3:0 – RHC[3:0] Region Hash Completed Interrupt Disable

Value	Description
0	No effect.
1	When RHC[i] is set to one, the Region i Hash Completed interrupt is disabled.

56.6.6 TRNG Output Data Register

Name: TRNG_ODATA
Offset: 0x50
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	ODATA[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ODATA[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ODATA[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ODATA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ODATA[31:0] Output Data
The 32-bit Output Data register contains the 32-bit random data.

converted to a gain error by the AFE. The noise generated by V_{VREFP} is converted by the AFE to count noise.

Table 59-30. VREFP Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VREFP}	Voltage Range	Full operational	1.7	–	VDDIN	V
	RMS Noise (see **Note 2**)	Bandwidth up to 1.74MHz VREFP=1.7V	–	–	120	µV
R_{VREFP}	Input DC Impedance	AFE reference resistance bridge (see **Note 1**)	–	4.7	–	kOhm
Vin	Input Linear Range (see **Note 3**)	Operational Range	2	-	98	%VVREFP
I_{VREFP}	Current	V_{VREFP} = 3.3V	–	0.8	–	mA

Note:

1. When the AFE is in Sleep mode, the VREFP impedance has a minimum of 10 MOhm.
2. Requested noise on VREFP.
3. Electrical parameters specified inside the operational range. Exceeding this range can introduce additional INL error up to +/- 5 LSB and temperature dependency up to +/-10 LSB.

59.8.3 AFE Timings

Table 59-31. AFE Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{AFE\ Clock}$	Clock Frequency	–	4	20	40	MHz
$t_{AFE\ Clock}$	Clock Period	–	25	50	250	ns
f_S	Sampling Frequency (see **Note 1**)	–	–	–	1.74	MHz
t_{START}	AFE Startup Time	Sleep mode to Normal mode	–	–	4	µs
		Fast Wake-up mode to Normal mode	-	-	2	µs

Note:

1. $f_s = 1 / t_{AFE\_conv}$ in Free Run mode; otherwise defined by the trigger timing.

59.8.4 AFE Transfer Function

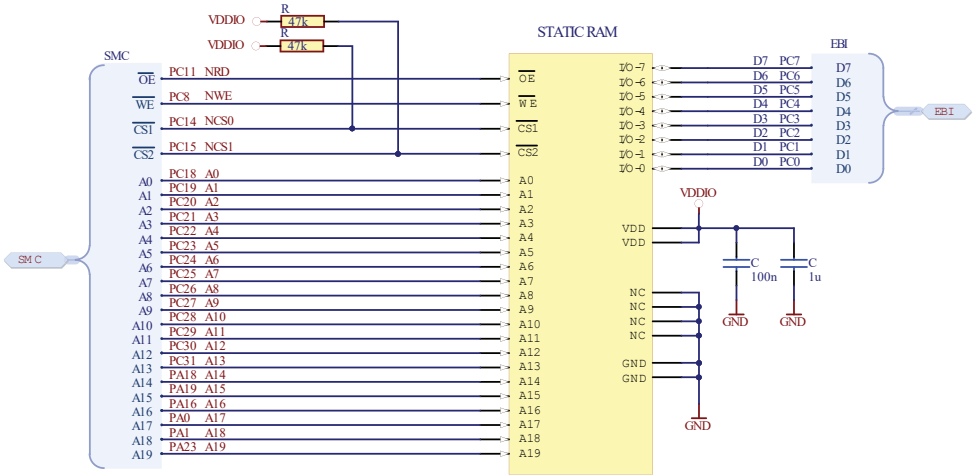
The first operation of the AFE is a sampling function relative to V_{DAC}. V_{DAC} is generated by an internal DAC0 or DAC1. All operations after the Sample-and-Hold are differential relative to an internal common mode voltage $V_{CM} = V_{VREFP}/2$.

In Differential mode, the Sample-and-Hold common mode voltage is equal to $V_{DAC} = V_{VREFP}/2$ (set by software DAC0 and DAC1 to code 512).

In Single-ended mode, V_{DAC} is the common mode voltage. V_{DAC} is the output of DAC0 or DAC1 voltage. All operations after the Sample-and-Hold are differential, including those in Single-ended mode.

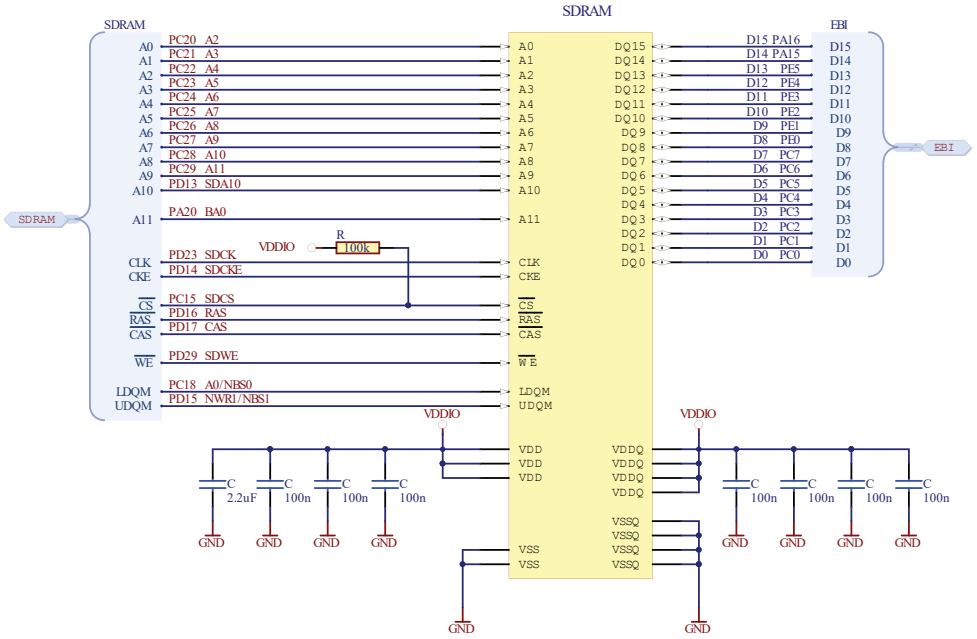
For the formula example, the internal DAC0 or DAC1 is set for the code 512.

Figure 60-3. Schematic Example with a 8 Mb/8-bit Static RAM



Note: For more details on the pin configuration of the EBI, refer to Table 33-3.

Figure 60-4. Schematic Example with a 16 Mb/16-bit SDRAM



Note:

1. It is required to adjust the drive (LOW/HIGH) and it may be required to add external resistors for impedance adjustment.
2. For more details on the pin configuration of the EBI, refer to Table 33-3.