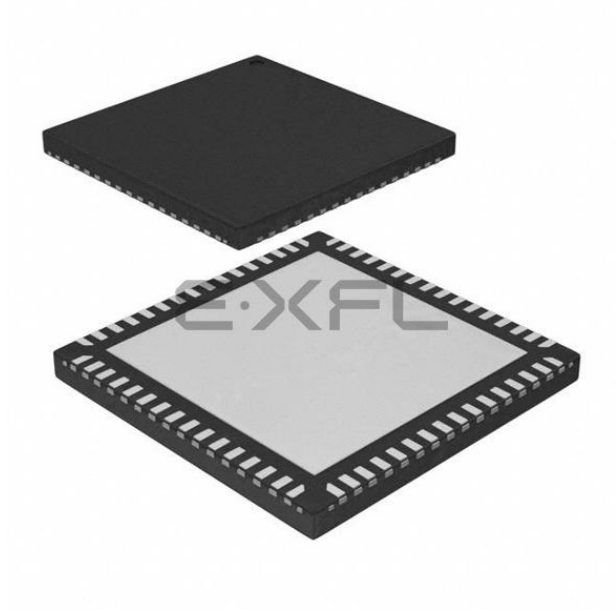

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	I²C, IrDA, LINbus, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	44
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 5x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70j19a-mn

32.6.1.52 PIO Parallel Capture Interrupt Disable Register

Name: PIO_PCIDR
Offset: 0x0158
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect

1: Disables the corresponding interrupt

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access					RXBUFF	ENDRX	OVRE	DRDY
Reset								

Bit 3 – RXBUFF Reception Buffer Full Interrupt Disable

Bit 2 – ENDRX End of Reception Transfer Interrupt Disable

Bit 1 – OVRE Parallel Capture Mode Overrun Error Interrupt Disable

Bit 0 – DRDY Parallel Capture Mode Data Ready Interrupt Disable

36.9.20 XDMAC Channel x Interrupt Mask Register [x = 0..23]

Name: XDMAC_CIM
Offset: 0x58 + n*0x40 [n=0..23]
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

Bit 6 – ROIM Request Overflow Error Interrupt Mask Bit

Value	Description
0	Request overflow interrupt is masked.
1	Request overflow interrupt is activated.

Bit 5 – WBEIM Write Bus Error Interrupt Mask Bit

Value	Description
0	Bus error interrupt is masked.
1	Bus error interrupt is activated.

Bit 4 – RBEIM Read Bus Error Interrupt Mask Bit

Value	Description
0	Bus error interrupt is masked.
1	Bus error interrupt is activated.

Bit 3 – FIM End of Flush Interrupt Mask Bit

Value	Description
0	End of flush interrupt is masked.
1	End of flush interrupt is activated.

36.9.26 XDMAC Channel x Microblock Control Register [x = 0..23]

Name: XDMAC_CUBC
Offset: 0x70 + n*0x40 [n=0..23]
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	UBLEN[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	UBLEN[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	UBLEN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – UBLEN[23:0] Channel x Microblock Length
This field indicates the number of data in the microblock. The microblock contains UBLEN data.

The GMAC supports both hardware controlled pause of the transmitter, upon reception of a pause frame, and hardware generated pause frame transmission.

38.6.16.1 802.3 Pause Frame Reception

Bit 13 of the Network Configuration register is the pause enable control for reception. If this bit is set, transmission will pause if a non zero pause quantum frame is received.

If a valid pause frame is received then the Pause Time register is updated with the new frame's pause time, regardless of whether a previous pause frame is active or not. An interrupt (either bit 12 or bit 13 of the Interrupt Status register) is triggered when a pause frame is received, but only if the interrupt has been enabled (bit 12 and bit 13 of the Interrupt Mask register). Pause frames received with non zero quantum are indicated through the interrupt bit 12 of the Interrupt Status register. Pause frames received with zero quantum are indicated on bit 13 of the Interrupt Status register.

Once the Pause Time register is loaded and the frame currently being transmitted has been sent, no new frames are transmitted until the pause time reaches zero. The loading of a new pause time, and hence the pausing of transmission, only occurs when the GMAC is configured for full duplex operation. If the GMAC is configured for half duplex there will be no transmission pause, but the pause frame received interrupt will still be triggered. A valid pause frame is defined as having a destination address that matches either the address stored in Specific Address register 1 or if it matches the reserved address of 0x0180C2000001. It must also have the MAC control frame type ID of 0x8808 and have the pause opcode of 0x0001.

Pause frames that have frame check sequence (FCS) or other errors will be treated as invalid and will be discarded. 802.3 Pause frames that are received after Priority-based Flow Control (PFC) has been negotiated will also be discarded. Valid pause frames received will increment the pause frames received statistic register.

The pause time register decrements every 512 bit times once transmission has stopped. For test purposes, the retry test bit can be set (bit 12 in the Network Configuration register) which causes the Pause Time register to decrement every GTXCK cycle once transmission has stopped.

The interrupt (bit 13 in the Interrupt Status register) is asserted whenever the Pause Time register decrements to zero (assuming it has been enabled by bit 13 in the Interrupt Mask register). This interrupt is also set when a zero quantum pause frame is received.

38.6.16.2 802.3 Pause Frame Transmission

Automatic transmission of pause frames is supported through the transmit pause frame bits of the Network Control register. If either bit 11 or bit 12 of the Network Control register is written with logic 1, an 802.3 pause frame will be transmitted, providing full duplex is selected in the Network Configuration register and the transmit block is enabled in the Network Control register.

Pause frame transmission will happen immediately if transmit is inactive or if transmit is active between the current frame and the next frame due to be transmitted.

Transmitted pause frames comprise the following:

- A destination address of 01-80-C2-00-00-01
- A source address taken from Specific Address register 1
- A type ID of 88-08 (MAC control frame)
- A pause opcode of 00-01
- A pause quantum register
- Fill of 00 to take the frame to minimum frame length
- Valid FCS

38.8.26 GMAC IPG Stretch Register

Name: GMAC_IPGS
Offset: 0x0BC
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	FL[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	FL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – FL[15:0] Frame Length
Bits FL[7:0] are multiplied with the previously transmitted frame length (including preamble), and divided by FL[15:8]+1 (adding 1 to prevent division by zero). $\mathrm{RESULT} = \frac{\mathrm{FL[7:0]}}{\mathrm{F[15+8]+1}}$

If RESULT > 96 and the IP Stretch Enable bit in the Network Configuration Register (GMAC_NCFGR.IPGSEN) is written to '1', RESULT is used for the transmit inter-packet-gap.

38.8.112 GMAC Interrupt Mask Register Priority Queue x

Name: GMAC_IMRPQx
Offset: 0x0640 + x*0x04 [x=0..4]
Reset: 0x00000000
Property: Read/Write

A read of this register returns the value of the receive complete interrupt mask.

A write to this register directly affects the state of the corresponding bit in the Interrupt Status Register, causing an interrupt to be generated if a '1' is written.

The following values are valid for all listed bit names of this register:

0: Corresponding interrupt is enabled.

1: Corresponding interrupt is disabled.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access					HRESP	ROVR		
Reset					0	0		

Bit	7	6	5	4	3	2	1	0
Access	TCOMP	AHB	RLEX			RXUBR	RCOMP	
Reset	0	0	0			0	0	

Bit 11 – HRESP HRESP Not OK

Bit 10 – ROVR Receive Overrun

Bit 7 – TCOMP Transmit Complete

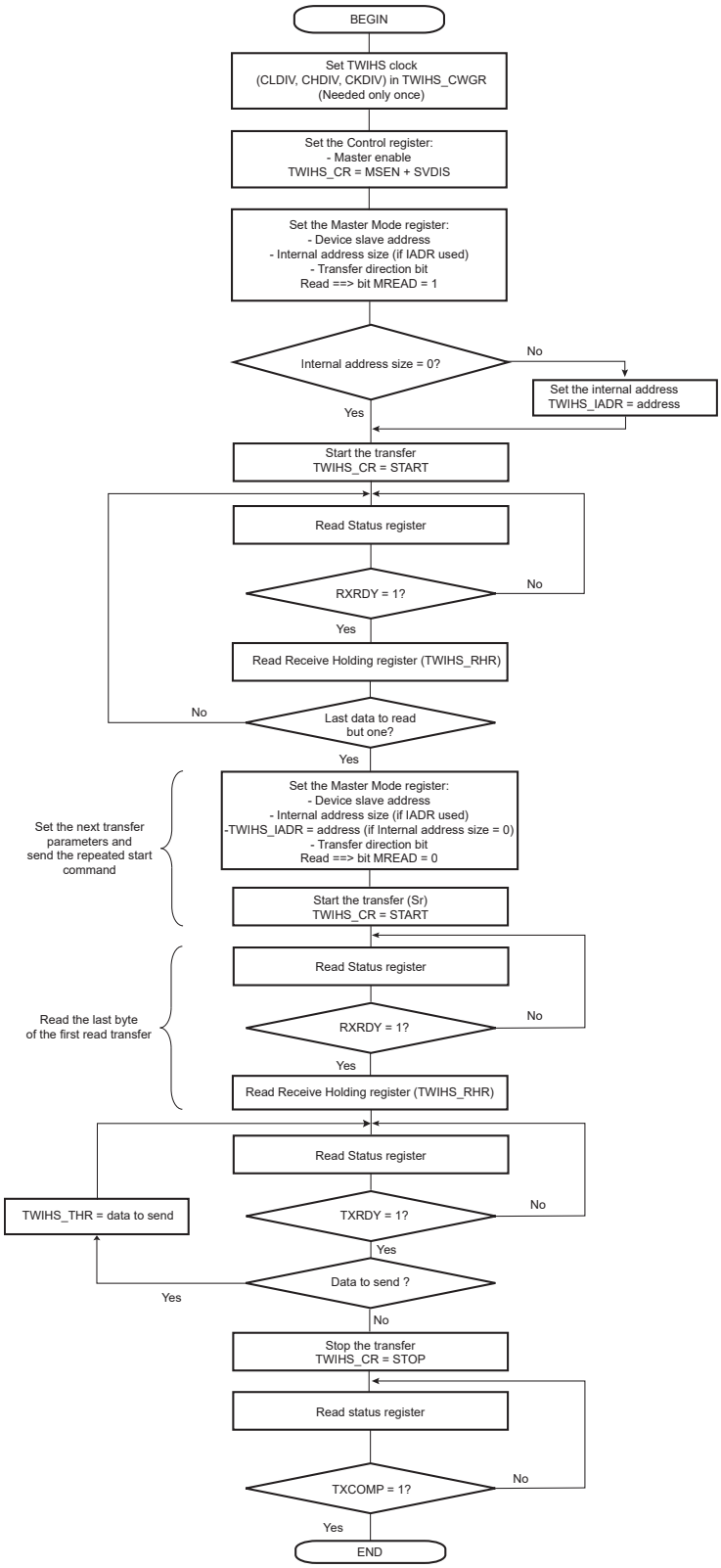
Bit 6 – AHB AHB Error

Bit 5 – RLEX Retry Limit Exceeded or Late Collision

Bit 2 – RXUBR RX Used Bit Read

Bit 1 – RCOMP Receive Complete

Figure 43-26. TWIHS Read Operation with Multiple Data Bytes + Write Operation with Multiple Data Bytes (Sr)



Bit 7 – UNRE Underrun Error Interrupt Disable

Bit 6 – OVRE Overrun Error Interrupt Disable

Bit 5 – GACC General Call Access Interrupt Disable

Bit 4 – SVACC Slave Access Interrupt Disable

Bit 2 – TXRDY Transmit Holding Register Ready Interrupt Disable

Bit 1 – RXRDY Receive Holding Register Ready Interrupt Disable

Bit 0 – TXCOMP Transmission Completed Interrupt Disable

Figure 44-3. Audio Application Block Diagram

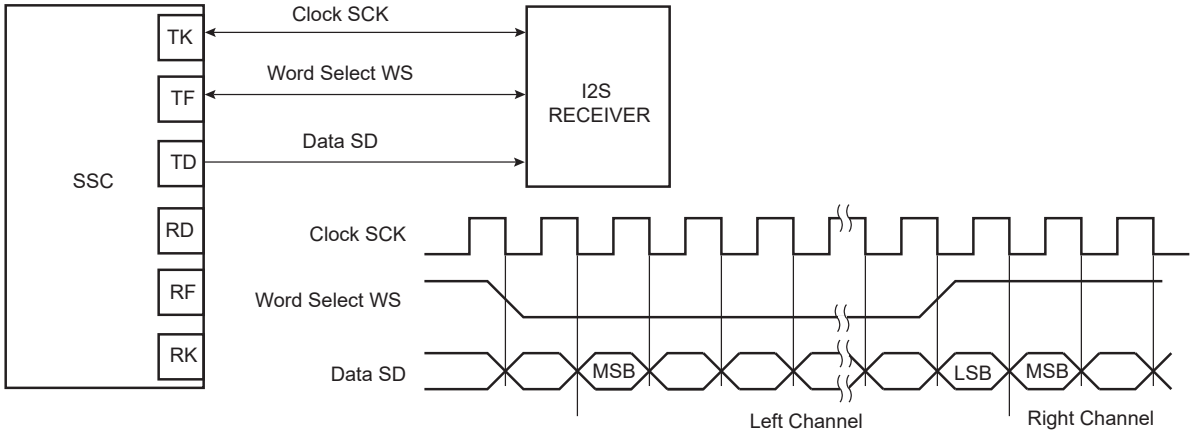
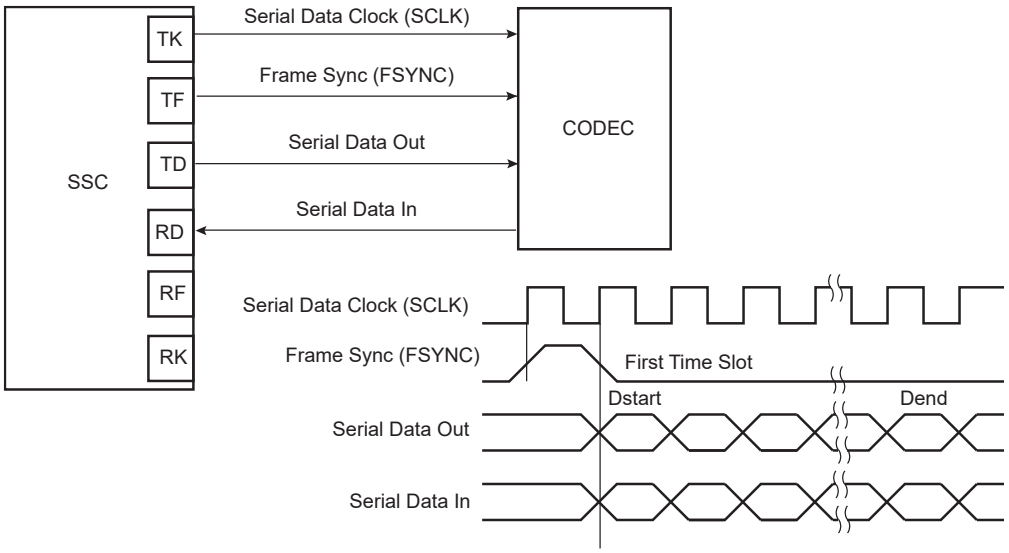


Figure 44-4. Codec Application Block Diagram



Value	Name	Description
3	TF_HIGH	Detection of a high level on TF signal
4	TF_FALLING	Detection of a falling edge on TF signal
5	TF_RISING	Detection of a rising edge on TF signal
6	TF_LEVEL	Detection of any level change on TF signal
7	TF_EDGE	Detection of any edge on TF signal

Bits 7:6 – CKG[1:0] Transmit Clock Gating Selection

Value	Name	Description
0	CONTINUOUS	None
1	EN_TF_LOW	Transmit Clock enabled only if TF Low
2	EN_TF_HIGH	Transmit Clock enabled only if TF High

Bit 5 – CKI Transmit Clock Inversion
CKI affects only the Transmit Clock and not the Output Clock signal.

Value	Description
0	The data outputs (Data and Frame Sync signals) are shifted out on Transmit Clock falling edge. The Frame Sync signal input is sampled on Transmit Clock rising edge.
1	The data outputs (Data and Frame Sync signals) are shifted out on Transmit Clock rising edge. The Frame Sync signal input is sampled on Transmit Clock falling edge.

Bits 4:2 – CKO[2:0] Transmit Clock Output Mode Selection

Value	Name	Description
0	NONE	None, TK pin is an input
1	CONTINUOUS	Continuous Transmit Clock, TK pin is an output
2	TRANSFER	Transmit Clock only during data transfers, TK pin is an output

Bits 1:0 – CKS[1:0] Transmit Clock Selection

Value	Name	Description
0	MCK	Divided Clock
1	RK	RK Clock signal
2	TK	TK pin

44.9.8 SSC Transmit Holding Register

Name: SSC_THR
Offset: 0x24
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
	TDAT[31:24]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TDAT[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TDAT[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TDAT[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bits 31:0 – TDAT[31:0] Transmit Data
Right aligned regardless of the number of data bits defined by DATLEN in SSC_TFMR.

44.9.13 SSC Status Register

Name: SSC_SR
Offset: 0x40
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RXEN	TXEN
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
					RXSYN	TXSYN	CP1	CP0
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
			OVRUN	RXRDY			TXEMPTY	TXRDY
Access			R	R			R	R
Reset			0	0			0	0

Bit 17 – RXEN Receive Enable

Value	Description
0	Receive is disabled.
1	Receive is enabled.

Bit 16 – TXEN Transmit Enable

Value	Description
0	Transmit is disabled.
1	Transmit is enabled.

Bit 11 – RXSYN Receive Sync

Value	Description
0	An Rx Sync has not occurred since the last read of the Status Register.
1	An Rx Sync has occurred since the last read of the Status Register.

Bit 10 – TXSYN Transmit Sync

Value	Description
0	A Tx Sync has not occurred since the last read of the Status Register.
1	A Tx Sync has occurred since the last read of the Status Register.

45.8.5 I2SC Status Set Register

Name: I2SC_SSR
Offset: 0x10
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			TXURCH[1:0]					
Access			W	W				
Reset			–	–				

Bit	15	14	13	12	11	10	9	8
							RXORCH[1:0]	
Access							W	W
Reset							–	–

Bit	7	6	5	4	3	2	1	0
		TXUR				RXOR		
Access		W				W		
Reset		–				–		

Bits 21:20 – TXURCH[1:0] Transmit Underrun Per Channel Status Set
Writing a ’0’ has no effect.

Writing a ’1’ to any bit in this field sets the corresponding bit in I2SC_SR and the corresponding interrupt request.

Bits 9:8 – RXORCH[1:0] Receive Overrun Per Channel Status Set
Writing a ’0’ has no effect.

Writing a ’1’ to any bit in this field sets the corresponding bit in I2SC_SR and the corresponding interrupt request.

Bit 6 – TXUR Transmit Underrun Status Set
Writing a ’0’ to this bit has no effect.

Writing a ’1’ to this bit sets the status bit.

Bit 2 – RXOR Receive Overrun Status Set
Writing a ’0’ to this bit has no effect.

Writing a ’1’ to this bit sets the status bit.

46.7.42 USART LON Priority Register

Name: US_LONPRIO
Offset: 0x007C
Reset: 0x0
Property: Read/Write

This register is relevant only if USART_MODE = 0x9 in the USART Mode Register.

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
		NPS[6:0]						
Access								
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		PSNB[6:0]						
Access								
Reset		0	0	0	0	0	0	0

Bits 14:8 – NPS[6:0] LON Node Priority Slot

Value	Description
0-127	Node priority slot.

Bits 6:0 – PSNB[6:0] LON Priority Slot Number

Value	Description
0-127	Number of priority slots in the LON network configuration.

Value	Description
0	The interrupt on IDX input is disabled.
1	The interrupt on IDX input is enabled.

51.7.43 PWM Channel Period Register

Name: PWM_CPRDx
Offset: 0x020C + x*0x20 [x=0..3]
Reset: 0x00000000
Property: Read/Write

This register can only be written if bits WPSWS3 and WPHWS3 are cleared in the PWM Write Protection Status Register.

Only the first 16 bits (channel counter size) are significant.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CPRD[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CPRD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CPRD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – CPRD[23:0] Channel Period
If the waveform is left-aligned, then the output waveform period depends on the channel counter source clock and can be calculated:

– By using the PWM peripheral clock divided by a given prescaler value “X” (where X = 2^{PREA} is 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, or 1024). The resulting period formula is:

$$\frac{(X \times \mathrm{CPRD})}{f_{\text{peripheral clock}}}$$

– By using the PWM peripheral clock divided by a given prescaler value “X” (see above) and by either the DIVA or the DIVB divider. The formula becomes, respectively:

$$\frac{(X \times \mathrm{CPRD} \times \mathrm{DIVA})}{f_{\text{peripheral clock}}} \text{ or } \frac{(X \times \mathrm{CPRD} \times \mathrm{DIVB})}{f_{\text{peripheral clock}}}$$

If the waveform is center-aligned, then the output waveform period depends on the channel counter source clock and can be calculated:

Value	Name	Description
		TRGMODE = 2, 3: TRGINx active level is 0
1	RISING_ONE	TRGMODE = 1: TRGINx event detection on rising edge. TRGMODE = 2, 3: TRGINx active level is 1

Bits 25:24 – TRGMODE[1:0] External Trigger Mode

Value	Name	Description
0	OFF	External trigger is not enabled.
1	MODE1	External PWM Reset Mode
2	MODE2	External PWM Start Mode
3	MODE3	Cycle-by-cycle Duty Mode

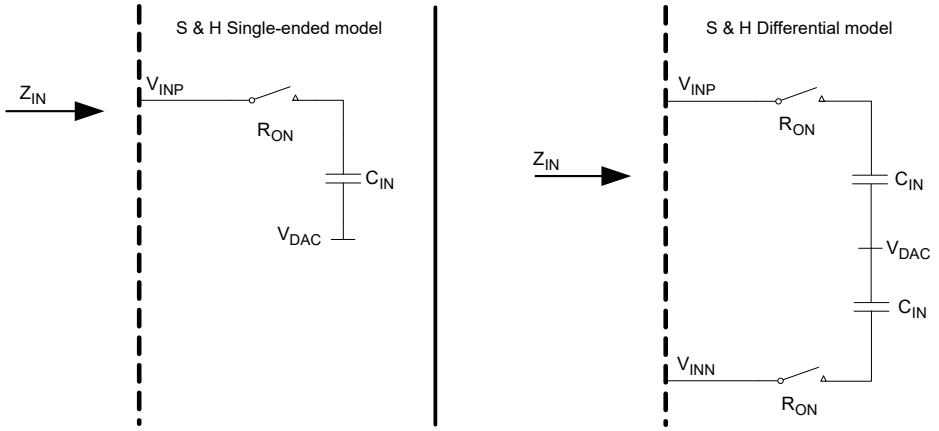
Bits 23:0 – MAXCNT[23:0] Maximum Counter value
Maximum channel x counter value measured at the TRGINx event since the last read of the register.

At the TRGINx event, if the channel x counter value is greater than the stored MAXCNT value, then MAXCNT is updated by the channel x counter value.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
		Gain=2	-0.3	0.3	1.4	
		Gain=4	-0.3	0.7	3.3	
Single-Ended Mode						
E_O	Single-ended Offset Error (see **Note 1**)	Gain=1	-20	–	35	LSB
E_G	Single-ended Gain Error	Gain=1	0.3	0.7	1.8	%
		Gain=2	0.3	1.3	3.6	
		Gain=4	0.3	1.7	4.7	

58.8.6 AFE Channel Input Impedance

Figure 58-15. Input Channel Model



where:

- Z_{IN} is input impedance in Single-ended or Differential mode
- C_{IN} = 2 to 8 pF ±20% depending on the gain value and mode (SE or DIFF); temperature dependency is negligible
- R_{ON} is typical 2 kΩ and 8 kΩ max (worst case process and high temperature)

The following formula is used to calculate input impedance:

$$Z_{\mathrm{IN}} = \frac{1}{f_S \times C_{\mathrm{IN}}}$$

where:

- f_S is the sampling frequency of the AFE channel
- Typ values are used to compute AFE input impedance Z_{IN}

Table 58-37. Input Capacitance (C_{IN}) Values

Gain Selection	Single-ended	Differential	Unit
1	2	2	pF
2	4	4	
4	8	8	

Date	Changes
	Updated Section 30.5.2 ”Main RC Oscillator Frequency Adjustment”
	Section 31. ”Power Management Controller (PMC)” Figure 31-1 “General Clock Distribution Block Diagram”: updated PMC_PCR block. Section 31.4 ”Master Clock Controller”: added note concerning fields MDIV and CSS. “Core and Bus Independent Clocks for Peripherals” now Section 31.8 (was Section 32.12). Table 31-1 “Clock Assignments” : added note on PCKx requirements. Section 31.9 ”Peripheral and Generic Clock Controller”: changed title (was “Peripheral Clock Controller”) and updated content regarding generic clock. Section 31.12 ”Programmable Clock Output Controller”: in second paragraph, modified range of selectable Output Signal dividing values from “a power of 2 between 1 and 64” to “1 to 256”. Section 31.17 ”Recommended Programming Sequence”: in Step 8, modified range of PCKx prescaler selectable values from “1, 2, 4, 8, 16, 32, 64” to “1 to 256”. Table 31-4 “Register Mapping” : defined 0x0040_4040 as PMC_OCR reset value; deleted footnote “The reset value depends on factory settings.” Section 31.20.1 ”PMC System Clock Enable Register”, Section 31.20.2 ”PMC System Clock Disable Register” and Section 31.20.3 ”PMC System Clock Status Register”: bit 15 modified to PCK7 (was ‘reserved’). Section 31.20.10 ”PMC Clock Generator PLLA Register”: changed DIVA description for value ‘0’.
cont’d on next page	
12-Oct-16	Section 33. ”External Bus Interface (EBI)” Table 33-1 “EBI I/O Lines Description” : added Note (1) on SDCK.
	Section 34. ”SDRAM Controller (SDRAMC)” Section 34.7.3 ”SDRAMC Configuration Register”: in TWO_CS description, added “This feature is not supported when SDR-SDRAM device embeds two internal banks.” Updated description tables for NC and NR fields.
	Section 36. ”DMA Controller (XDMAC)” Table 36-1 “Peripheral Hardware Requests” : replaced line with ‘DACC - Transmit - 30’ by two lines ‘DACC0 - Transmit - 30’ and ‘DACC1 - Transmit - 31’ Added information regarding XDMAC_CC.INITD in Section 36.8 ”XDMAC Software Requirements” and Section 36.9.28 ”XDMAC Channel x [x = 0..23] Configuration Register”. Section 36.9.3 ”XDMAC Global Weighted Arbiter Configuration Register”: replaced “XDMAC scheduler” with “DMAC scheduler” throughout.
	Section 39. ”Ethernet MAC (GMAC)” Section 39.2 ”Embedded Characteristics”: deleted queue sizes (now found in Table 39-5 “Queue Size”).