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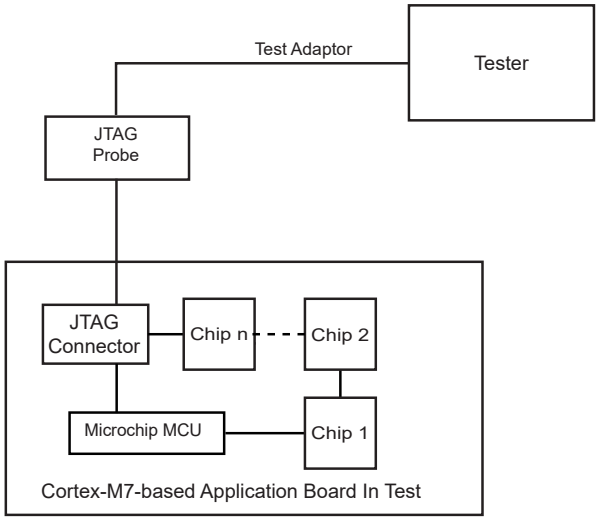
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	I²C, IrDA, LINbus, SPI, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	44
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 5x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70j20a-an

Figure 16-3. Application Test Environment Example



16.7 Functional Description

16.7.1 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash Programming mode. The TST pin integrates a permanent pulldown resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enable Fast Flash Programming mode, refer to 18. Fast Flash Programming Interface (FFPI).

16.7.2 Debug Architecture

Figure 16-4 shows the debug architecture used. The Cortex-M7 embeds six functional units for debug:

- Serial Wire Debug Port (SW-DP) debug access
- FPB (Flash Patch Breakpoint)
- DWT (Data Watchpoint and Trace)
- ITM (Instrumentation Trace Macrocell)
- 6-pin Embedded Trace Macrocell (ETM) for instruction trace stream, including CoreSight Trace Port Interface Unit (TPIU)
- IEEE1149.1 JTAG Boundary scan on all digital pins

The debug architecture information that follows is mainly dedicated to developers of SW-DP Emulators/ Probes and debugging tool vendors for Cortex-M7-based microcontrollers. For further details on SW-DP, see the Cortex - M7 Technical Reference Manual.

19.4.8 Peripheral Clock Configuration Register

Name: CCFG_PCCR
Offset: 0x0118
Reset: 0x00022224
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		I2SC1CC	I2SC0CC	TC0CC				
Access								
Reset		0	0	0				

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 22 – I2SC1CC I2SC1 Clock Configuration

Value	Description
0	Peripheral clock of I2SC1 is used.
1	GCLK is used.

Bit 21 – I2SC0CC I2SC0 Clock Configuration

Value	Description
0	Peripheral clock of I2SC0 is used.
1	GCLK is used.

Bit 20 – TC0CC TC0 Clock Configuration

Value	Description
0	PCK6 is used (default).
1	PCK7 is used.

31.6 SysTick External Clock

When the processor selects the SysTick external clock, the calibration value is fixed to 37500. This allows the generation of a time base of 1 ms with the SysTick clock at the maximum frequency on MCK divided by 8.

Refer to the section “ARM Cortex-M7 Processor” for details on selecting the SysTick external clock.

Related Links

15. ARM Cortex-M7 (ARM)

31.7 USB Full-speed Clock Controller

The user can select the PLLA or the UPLL output as the USB FS clock (USB_48M) by writing a ‘1’ to the USBS bit in the USB Clock Register (PMC_USB). The user then must program the corresponding PLL to generate an appropriate frequency depending on the USBDIV bit in PMC_USB.

When PMC_SR.LOCKA and PMC_SR.LOCKU are set to ‘1’, the PLLA and UPLL are stable. Then, USB_48M can be enabled by setting the USBCLK bit in the System Clock Enable register (PMC_SCER). To save power on this peripheral when not used, the user can set the USBCLK bit in the System Clock Disable register (PMC_SCDR). The USBCLK bit in the System Clock Status register (PMC_SCSR) gives the status of this clock. The USB port requires both the USB clock signal and the peripheral clock. The USB peripheral clock is controlled by means of the Master Clock Controller.

31.8 Core and Bus Independent Clocks for Peripherals

The following table lists the peripherals that require a PCKx clock to operate while the core, bus and peripheral clock frequencies are modified, thus providing communications at a bit rate which is independent for the core/bus/peripheral clock. This mode of operation is possible by using the internally generated independent clock sources.

Internal clocks can be independently selected between SLCK, MAINCK, any available PLL clock, and MCK by configuring PMC_PCKx.CSS. The independent clock sources can be also divided by configuring PMC_PCKx.PRES.

Each internal clock signal (PCKx) can be enabled and disabled by writing a ‘1’ to the corresponding PMC_SCER.PCKx and PMC_SCDR.PCKx, respectively. The status of the internal clocks are given in PMC_SCSR.PCKx.

The status flag PMC_SR.PCKRDYx indicates that the programmable internal clock has been programmed in the Programmable clock registers.

The independent clock source must also be selected in each peripheral in the Clock Assignments table to operate communications, timings, etc without influencing the frequency of the core/bus/peripherals (except frequency limitations listed in each peripheral).

Table 31-1. Clock Assignments

Clock Name	Peripheral
PCK3	ETM
PCK4	UARTx/USARTx

32.6.1.4 PIO Output Enable Register

Name: PIO_OER
Offset: 0x0010
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Output Enable

Value	Description
0	No effect.
1	Enables the output on the I/O line.

Figure 35-24. TDF Optimization Disabled (TDF Mode = 0): TDF wait states between 2 read accesses on different chip selects

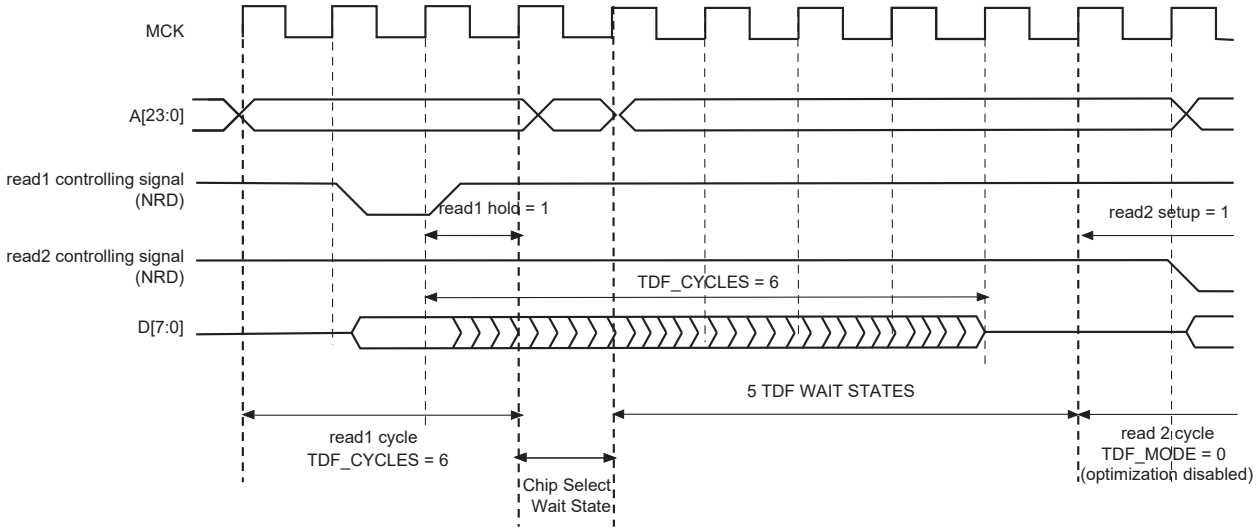
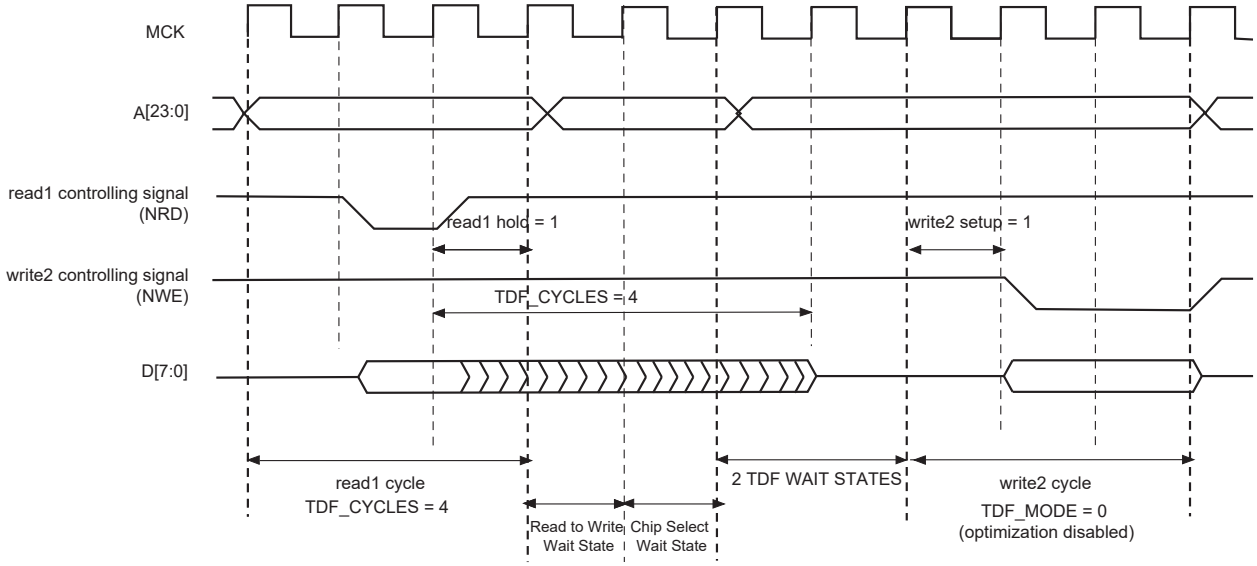


Figure 35-25. TDF Mode = 0: TDF wait states between a read and a write access on different chip selects



36.9.11 XDMAC Global Channel Read Suspend Register

Name: XDMAC_GRS
Offset: 0x28
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	RS23	RS22	RS21	RS20	RS19	RS18	RS17	RS16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RS15	RS14	RS13	RS12	RS11	RS10	RS9	RS8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RS7	RS6	RS5	RS4	RS3	RS2	RS1	RS0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 – RSx XDMAC Channel x Read Suspend

Value	Description
0	The read channel is not suspended.
1	The source requests for channel n are no longer serviced by the system scheduler.

Offset	Name	Bit Pos.								
0x0670	USBHS_HSTPIPINRQ8	7:0	INRQ[7:0]							
		15:8								INMODE
		23:16								
		31:24								
0x0674	USBHS_HSTPIPINRQ9	7:0	INRQ[7:0]							
		15:8								INMODE
		23:16								
		31:24								
0x0678 ... 0x067F	Reserved									
0x0680	USBHS_HSTPIPERR0	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0684	USBHS_HSTPIPERR1	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0688	USBHS_HSTPIPERR2	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x068C	USBHS_HSTPIPERR3	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0690	USBHS_HSTPIPERR4	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0694	USBHS_HSTPIPERR5	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0698	USBHS_HSTPIPERR6	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x069C	USBHS_HSTPIPERR7	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x06A0	USBHS_HSTPIPERR8	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								

Value	Description
	USBHS_DEVEPTIMRx) but not the endpoint configuration (USBHS_DEVEPTCFGx.ALLOC, USBHS_DEVEPTCFGx.EPBK, USBHS_DEVEPTCFGx.EPSIZE, USBHS_DEVEPTCFGx.EPDIR, USBHS_DEVEPTCFGx.EPTYPE).
1	Endpoint x is enabled.

39.6.57 Host Pipe x Disable Register (Control, Bulk Pipes)

Name: USBHS_HSTPIPIDRx
Offset: 0x0620 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

This register view is relevant only if PTYPE = 0x0 or 0x2 in "Host Pipe x Configuration Register".

For additional information, see "Host Pipe x Mask Register (Control, Bulk Pipes)".

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Clears the corresponding bit in USBHS_HSTPIPIMRx.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							PFREEZEC	PDISHDMAC
Access								
Reset							0	0

Bit	15	14	13	12	11	10	9	8
		FIFOCONC		NBUSYBKEC				
Access								
Reset		0		0				

Bit	7	6	5	4	3	2	1	0
	SHORTPACKETIEC	RXSTALLDEC	OVERFIEC	NAKEDEC	PERREC	TXSTPEC	TXOUTEC	RXINEC
Access								
Reset	0	0	0	0	0	0	0	0

Bit 17 – PFREEZEC Pipe Freeze Disable

Bit 16 – PDISHDMAC Pipe Interrupts Disable HDMA Request Disable

Bit 14 – FIFOCONC FIFO Control Disable

Bit 12 – NBUSYBKEC Number of Busy Banks Disable

Bit 7 – SHORTPACKETIEC Short Packet Interrupt Disable

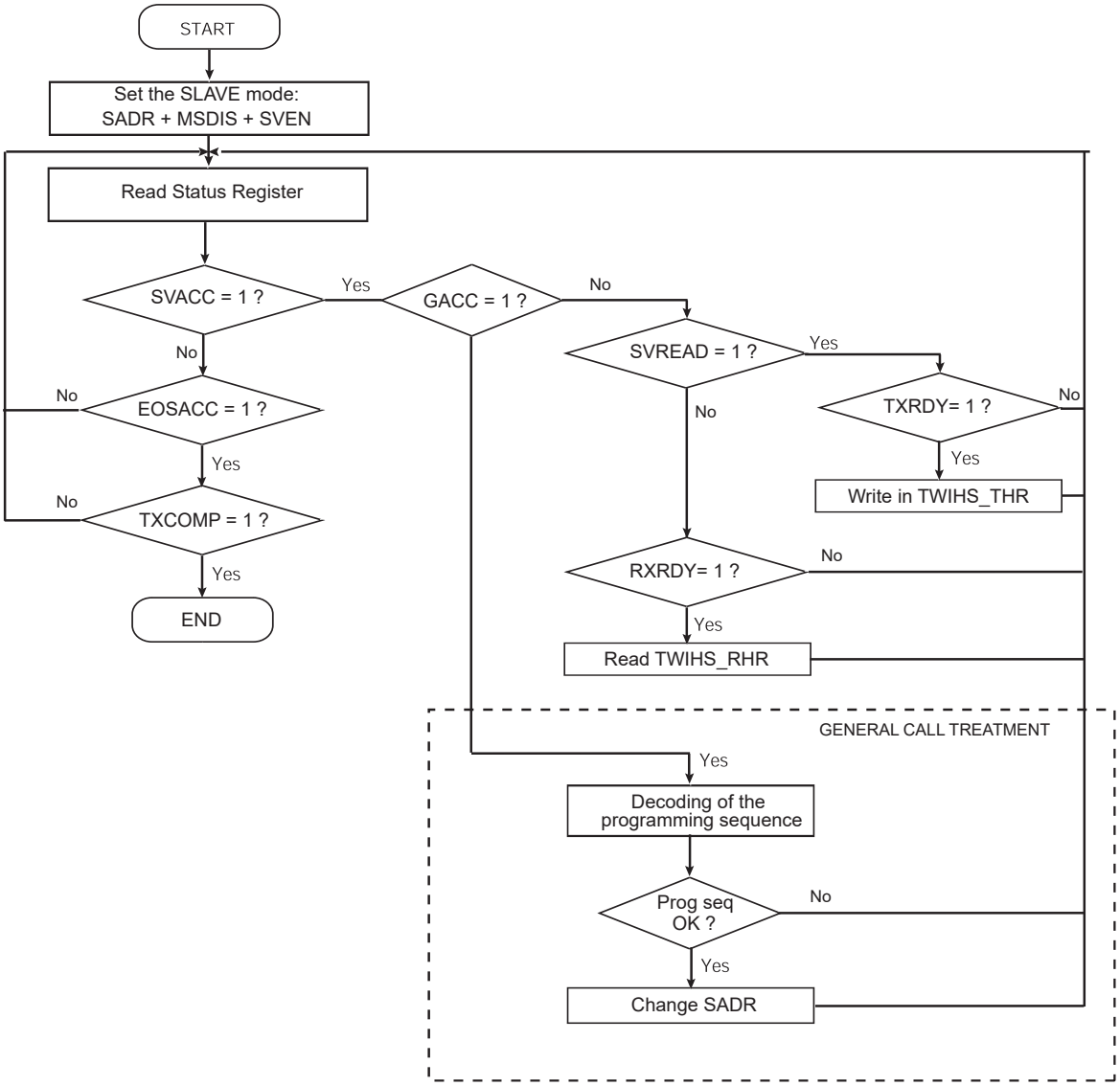
Bit 6 – RXSTALLDEC Received STALLed Interrupt Disable

Value	Description
0	No effect.
1	Disables the QSPI.

Bit 0 – QSPIEN QSPI Enable

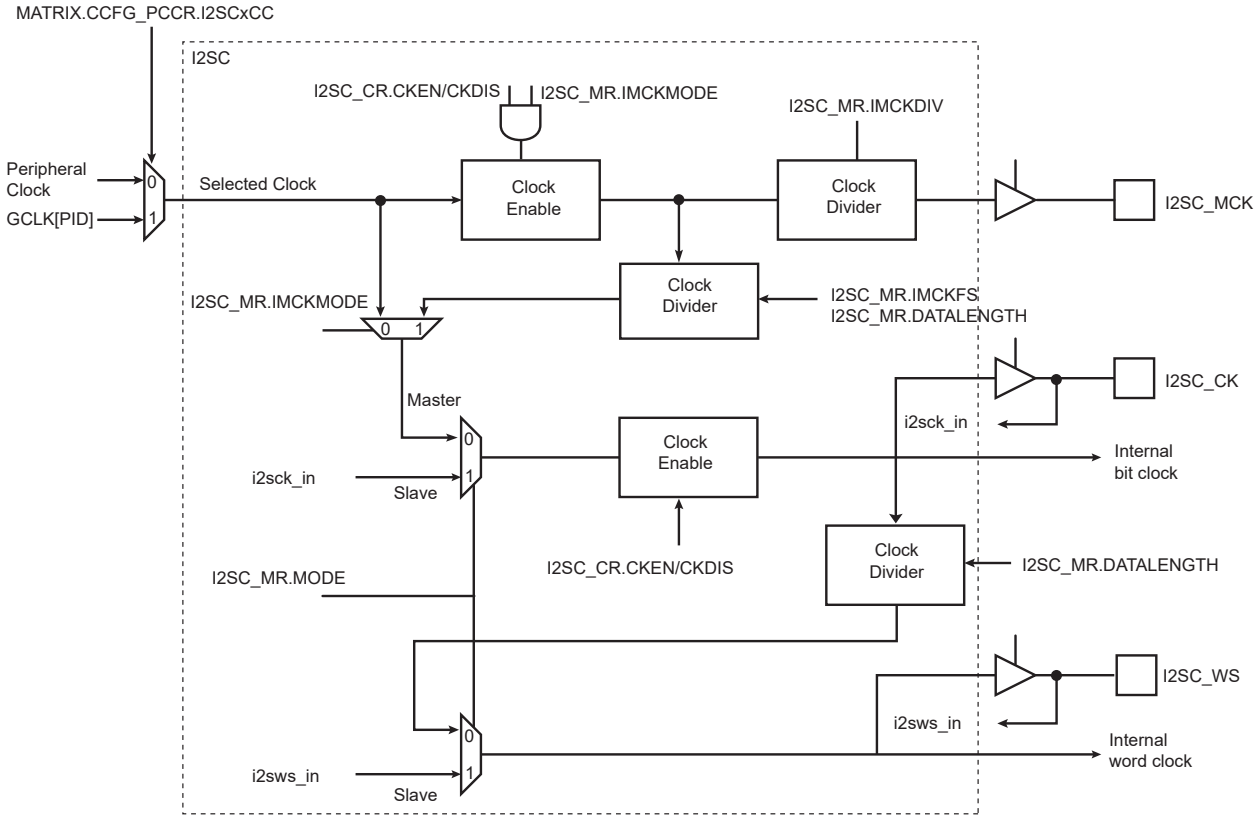
Value	Description
0	No effect.
1	Enables the QSPI to transfer and receive data.

Figure 43-43. Read Write Flowchart in Slave Mode



The I2SC_WS pin is used as word select as described in section "I2S Reception and Transmission Sequence".

Figure 45-3. I2SC Clock Generation



45.6.6 Mono

When the Transmit Mono bit (TXMONO) in I2SC_MR is set, data written to the left channel is duplicated to the right output channel.

When the Receive Mono bit (RXMONO) in I2SC_MR is set, data received from the left channel is duplicated to the right channel.

45.6.7 Holding Registers

The I2SC user interface includes a Receive Holding Register (I2SC_RHR) and a Transmit Holding Register (I2SC_THR). These registers are used to access audio samples for both audio channels.

When a new data word is available in I2SC_RHR, the Receive Ready bit (RXRDY) in I2SC_SR is set. Reading I2SC_RHR clears this bit.

A receive overrun condition occurs if a new data word becomes available before the previous data word has been read from I2SC_RHR. In this case, the Receive Overrun bit in I2SC_SR and bit i of the RXORCH field in I2SC_SR are set, where i is the current receive channel number.

When I2SC_THR is empty, the Transmit Ready bit (TXRDY) in I2SC_SR is set. Writing to I2SC_THR clears this bit.

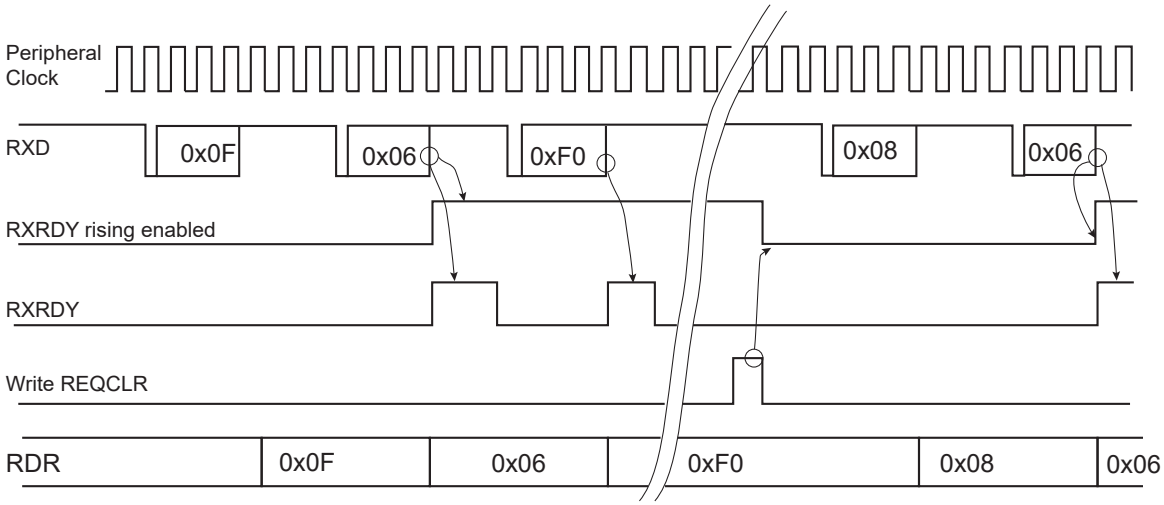
A transmit underrun condition occurs if a new data word needs to be transmitted before it has been written to I2SC_THR. In this case, the Transmit Underrun (TXUR) bit and bit i of the TXORCH field in I2SC_SR are set, where i is the current transmit channel number. If the TXSAME bit in I2SC_MR is '0',

- If VAL1 is strictly higher than VAL2, then the flag CMP is set to 1 if either received character equals VAL1 or VAL2.

By programming the CMPMODE bit to 1, the comparison function result triggers the start of the loading of UART_RHR (see the figure below). The trigger condition occurs as soon as the received character value matches the condition defined by the programming of VAL1, VAL2 and CMPPAR in UART_CMPR. The comparison trigger event can be restarted by writing a one to the REQCLR bit in UART_CR.

Figure 47-11. Receive Holding Register Management

CMPMODE = 1, VAL1 = VAL2 = 0x06



47.5.6 Asynchronous and Partial Wake-up (SleepWalking)

Asynchronous and partial wake-up (SleepWalking) is a means of data pre-processing that qualifies an incoming event, thus allowing the UART to decide whether or not to wake up the system. SleepWalking is used primarily when the system is in Wait mode (refer to section “Power Management Controller (PMC)”) but can also be enabled when the system is fully running.

No access must be performed in the UART between the enable of asynchronous partial wake-up and the wake-up performed by the UART.

If the system is in Wait mode and asynchronous and partial wake-up is enabled, the maximum baud rate that can be achieved equals 19200.

If the system is running or in Sleep mode, the maximum baud rate that can be achieved equals 115200 or higher. This limit is bounded by the peripheral clock frequency divided by 16.

The UART_RHR must be read before enabling asynchronous and partial wake-up.

When SleepWalking is enabled for the UART (refer to section “Power Management Controller (PMC)”), the PMC decodes a clock request from the UART. The request is generated as soon as there is a falling edge on the RXD line as this may indicate the beginning of a start bit. If the system is in Wait mode (processor and peripheral clocks switched off), the PMC restarts the fast RC oscillator and provides the clock only to the UART.

As soon as the clock is provided by the PMC, the UART processes the received frame and compares the received character with VAL1 and VAL2 in UART_CMPR (UART Comparison Register).

The UART instructs the PMC to disable the clock if the received character value does not meet the conditions defined by VAL1 and VAL2 fields in UART_CMPR (see Asynchronous Event Generating Only Partial Wake-up).

Bit 18 – TOOE Timeout Occurred Interrupt Enable

Bit 17 – MRAFE Message RAM Access Failure Interrupt Enable

Bit 16 – TSWE Timestamp Wraparound Interrupt Enable

Bit 15 – TEFLE Tx Event FIFO Event Lost Interrupt Enable

Bit 14 – TEFFE Tx Event FIFO Full Interrupt Enable

Bit 13 – TEFWE Tx Event FIFO Watermark Reached Interrupt Enable

Bit 12 – TEFNE Tx Event FIFO New Entry Interrupt Enable

Bit 11 – TFEE Tx FIFO Empty Interrupt Enable

Bit 10 – TCFE Transmission Cancellation Finished Interrupt Enable

Bit 9 – TCE Transmission Completed Interrupt Enable

Bit 8 – HPME High Priority Message Interrupt Enable

Bit 7 – RF1LE Receive FIFO 1 Message Lost Interrupt Enable

Bit 6 – RF1FE Receive FIFO 1 Full Interrupt Enable

Bit 5 – RF1WE Receive FIFO 1 Watermark Reached Interrupt Enable

Bit 4 – RF1NE Receive FIFO 1 New Message Interrupt Enable

Bit 3 – RF0LE Receive FIFO 0 Message Lost Interrupt Enable

Bit 2 – RF0FE Receive FIFO 0 Full Interrupt Enable

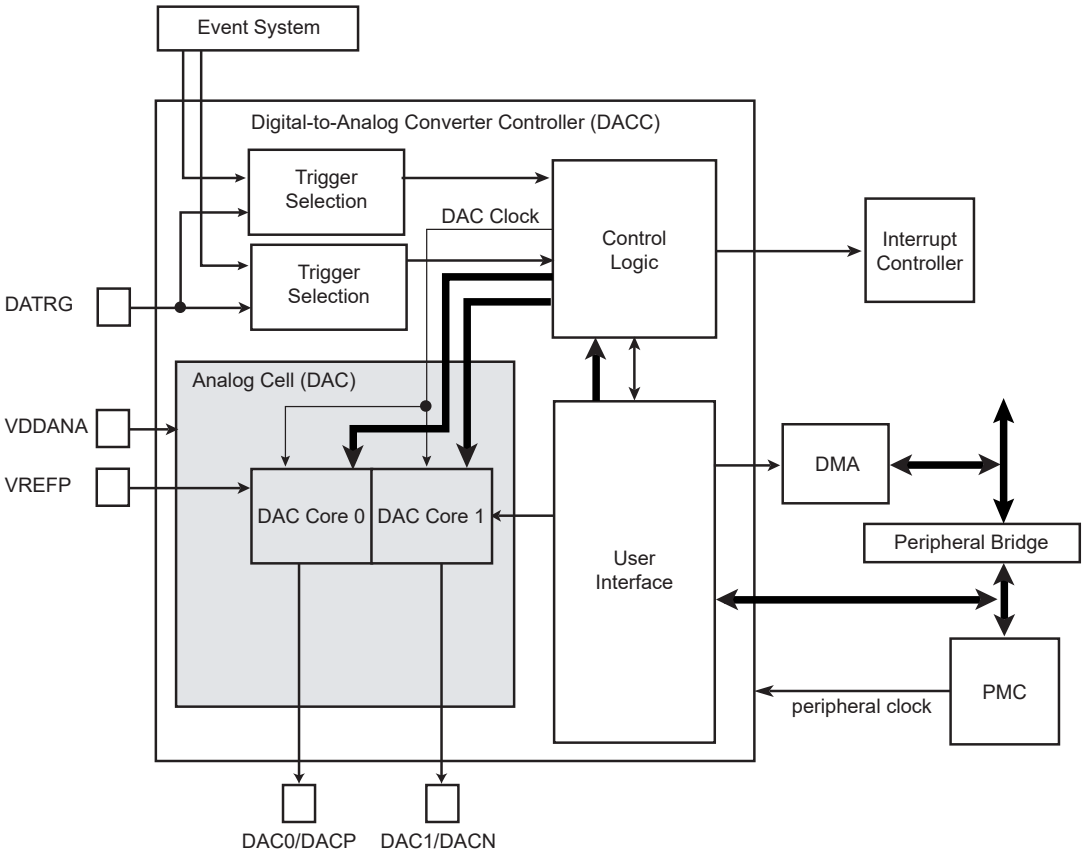
Bit 1 – RF0WE Receive FIFO 0 Watermark Reached Interrupt Enable

Bit 0 – RF0NE Receive FIFO 0 New Message Interrupt Enable

Value	Name	Description
	MCK	Peripheral clock
1	MCK_DIV_2	Peripheral clock/2
2	MCK_DIV_4	Peripheral clock/4
3	MCK_DIV_8	Peripheral clock/8
4	MCK_DIV_16	Peripheral clock/16
5	MCK_DIV_32	Peripheral clock/32
6	MCK_DIV_64	Peripheral clock/64
7	MCK_DIV_128	Peripheral clock/128
8	MCK_DIV_256	Peripheral clock/256
9	MCK_DIV_512	Peripheral clock/512
10	MCK_DIV_1024	Peripheral clock/1024
11	CLKA	Clock A
12	CLKB	Clock B

53.3 Block Diagram

Figure 53-1. Block Diagram



53.4 Signal Description

Table 53-1. DACC Signal Description

Name	Description	Direction
DAC0/DACP	Single-ended analog output channel 0 / Positive channel of differential analog output channel	Output
DAC1/DACN	Single-ended analog output channel 1 / Negative channel of differential analog output channel	Output
DATRG	Trigger	Input
VREFP	Positive reference voltage connected to VREFP	Input
VREFN	Negative reference voltage connected to VREFN	Input

- Hash Area—predefined memory space where the region hash results (digest) are stored

55.2 Embedded Characteristics

- DMA AHB Master Interface
- Supports Monitoring of up to 4 Non-Contiguous Memory Regions
- Supports Block Gathering Using Linked Lists
- Supports Secure Hash Algorithm (SHA1, SHA224, SHA256)
- Compliant with FIPS Publication 180-2
- Configurable Processing Period:
  - When SHA1 algorithm is processed, the runtime period is either 85 or 209 clock cycles.
  - When SHA256 or SHA224 algorithm is processed, the runtime period is either 72 or 194 clock cycles.
- Programmable Bus Burden

55.6.5 ICM Interrupt Disable Register

Name: ICM_IDR
Offset: 0x14
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
								URAD
Access								W
Reset								–

Bit	23	22	21	20	19	18	17	16
	RSU[3:0]				REC[3:0]			
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	–	0	0	0	–

Bit	15	14	13	12	11	10	9	8
	RWC[3:0]				RBE[3:0]			
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	–	0	0	0	–

Bit	7	6	5	4	3	2	1	0
	RDM[3:0]				RHC[3:0]			
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	–	0	0	0	–

Bit 24 – URAD Undefined Register Access Detection Interrupt Disable

Value	Description
0	No effect.
1	Undefined Register Access Detection interrupt is disabled.

Bits 23:20 – RSU[3:0] Region Status Updated Interrupt Disable

Value	Description
0	No effect.
1	When RSU[i] is set to one, the region i Status Updated interrupt is disabled.

Bits 19:16 – REC[3:0] Region End bit Condition detected Interrupt Disable

Value	Description
0	No effect.
1	When REC[i] is set to one, the region i End bit Condition interrupt is disabled.

Bits 15:12 – RWC[3:0] Region Wrap Condition Detected Interrupt Disable

Value	Description
0	No effect.
1	When RWC[i] is set to one, the Region i Wrap Condition interrupt is disabled.

57.5 Register Summary

Offset	Name	Bit Pos.								
0x00	AES_CR	7:0								START
		15:8								SWRST
		23:16								
		31:24								
0x04	AES_MR	7:0	PROCDLY[3:0]				DUALBUFF		GTAGEN	CIPHER
		15:8	LOD	OPMOD[2:0]			KEYSIZE[1:0]		SMOD[1:0]	
		23:16	CKEY[3:0]					CFBS[2:0]		
		31:24								
0x08 ... 0x0F	Reserved									
0x10	AES_IER	7:0								DATRDY
		15:8								URAD
		23:16								TAGRDY
		31:24								
0x14	AES_IDR	7:0								DATRDY
		15:8								URAD
		23:16								TAGRDY
		31:24								
0x18	AES_IMR	7:0								DATRDY
		15:8								URAD
		23:16								TAGRDY
		31:24								
0x1C	AES_ISR	7:0								DATRDY
		15:8	URAT[3:0]							URAD
		23:16								TAGRDY
		31:24								
0x20	AES_KEYWR0	7:0	KEYW[7:0]							
		15:8	KEYW[15:8]							
		23:16	KEYW[23:16]							
		31:24	KEYW[31:24]							
0x24	AES_KEYWR1	7:0	KEYW[7:0]							
		15:8	KEYW[15:8]							
		23:16	KEYW[23:16]							
		31:24	KEYW[31:24]							
0x28	AES_KEYWR2	7:0	KEYW[7:0]							
		15:8	KEYW[15:8]							
		23:16	KEYW[23:16]							
		31:24	KEYW[31:24]							
0x2C	AES_KEYWR3	7:0	KEYW[7:0]							
		15:8	KEYW[15:8]							
		23:16	KEYW[23:16]							
		31:24	KEYW[31:24]							

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level Input Voltage	GPIO_MLB	1.80	–	V_{DDIO} + 0.3	V
		GPIO_AD, GPIO_CLK	2		V_{DDIO} + 0.3	
		GPIO, CLOCK, RST, TEST	V_{DDIO} x 0.7	–	V_{DDIO} + 0.3	
V_{OH}	High-level Output Voltage	GPIO_MLB	2	–	–	V
		GPIO_AD, GPIO, RST, TEST, CLOCK , Low drive	V_{DDIO} - 0.4	–	–	
		GPIO_AD, GPIO, RST, TEST, CLOCK , High drive	V_{DDIO} - 0.4	–	–	
		GPIO_CLK, Low drive	V_{DDIO} - 0.4			
		GPIO_CLK, High drive	V_{DDIO} - 0.4	–	–	
V_{OL}	Low-level Output Voltage	GPIO_MLB,	–	–	0.4	V
		GPIO_AD, GPIO, RST, TEST, CLOCK, Low drive	–	–	0.4	
		GPIO_AD, GPIO, RST, TEST, CLOCK, High drive	–	–	0.4	
		GPIO_CLK, Low drive	–	–	0.4	
		GPIO_CLK, High drive	–	–	0.4	
V_{hys}	Hysteresis Voltage	GPIO with Hysteresis mode enabled	150	–	–	mV
I_{IL}	Low-level Input Current	Pullup OFF	-1	–	1	µA
		Pullup ON	10	–	55	
I_{IH}	High-level Input Current	Pulldown OFF	-1	–	1	µA
		Pulldown ON	10	–	55	
R_{SERIAL}	Serial Resistor	GPIO_MLB	–	9	–	Ohm
		GPIO_AD, GPIO_CLK	–	14	–	
		GPIO, CLOCK, RST, TEST	–	26	–	

Table 59-5. Voltage Regulator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDOUT}	DC Output Voltage	Normal mode, I_{LOAD} = 100 mA	1.2	1.23	1.26	V
		Standby mode	–	0	–	
I_{LOAD}	Maximum DC Output Current		–	–	150	mA
C_{DIN}	Input Decoupling Capacitor	(1)	–	4.7	–	µF
C_{DOUT}	Output Decoupling Capacitor	(2)	–	1	–	µF