Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	I²C, IrDA, LINbus, SPI, SSC, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	44
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 5x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70j20a-ant

LQFP Pin	LFBGA/ TFBGA Ball	UFBGA Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		PIO Peripheral D		Reset State
					Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
101	C12	D13	VDDIO	GPIO_ML B	PD10	I/O	–	–	GCRS	I	PWMC0_ PWML0	O	TD	O	MLBSIG	I/O	PIO, I, PD, ST
98	E11	E13	VDDIO	GPIO_AD	PD11	I/O	–	–	GRX2	I	PWMC0_ PWMH0	O	GTSUCOMP	O	ISI_D5	I	PIO, I, PU, ST
92	G10	G13	VDDIO	GPIO_AD	PD12	I/O	–	–	GRX3	I	CANTX1	O	SPI0_NPCS2	O	ISI_D6	I	PIO, I, PU, ST
88	G9	H11	VDDIO	GPIO_CLK	PD13	I/O	–	–	GCOL	I	–	–	SDA10	O	–	–	PIO, I, PU, ST
84	H10	J12	VDDIO	GPIO_AD	PD14	I/O	–	–	GRXCK	I	–	–	SDCKE	O	–	–	PIO, I, PU, ST
106	A11	D11	VDDIO	GPIO_AD	PD15	I/O	–	–	GTX2	O	RXD2	I	NWR1/NBS1	O	–	–	PIO, I, PU, ST
78	K11	K10	VDDIO	GPIO_AD	PD16	I/O	–	–	GTX3	O	TXD2	I/O	RAS	O	–	–	PIO, I, PU, ST
74	L11	M13	VDDIO	GPIO_AD	PD17	I/O	–	–	GTXER	O	SCK2	I/O	CAS	O	–	–	PIO, I, PU, ST
69	M10	M11	VDDIO	GPIO_AD	PD18	I/O	–	–	NCS1/SDCS	O	RTS2	O	URXD4	I	–	–	PIO, I, PU, ST
67	M9	L10	VDDIO	GPIO_AD	PD19	I/O	–	–	NCS3	O	CTS2	I	UTXD4	O	–	–	PIO, I, PU, ST
65	K9	K9	VDDIO	GPIO	PD20	I/O	–	–	PWMC0_ PWMH0	O	SPI0_MIS O	I/O	GTSUCOMP	O	–	–	PIO, I, PU, ST
63	H9	L9	VDDIO	GPIO_AD	PD21	I/O	–	–	PWMC0_ PWMH1	O	SPI0_MOSI	I/O	TIOA11	I/O	ISI_D1	I	PIO, I, PU, ST
60	M8	N9	VDDIO	GPIO_AD	PD22	I/O	–	–	PWMC0_ PWMH2	O	SPI0_SPCK	O	TIOB11	I/O	ISI_D0	I	PIO, I, PU, ST
57	M7	N7	VDDIO	GPIO_CLK	PD23	I/O	–	–	PWMC0_ PWMH3	O	–	–	SDCK	O	–	–	PIO, I, PU, ST
55	M6	K7	VDDIO	GPIO_AD	PD24	I/O	–	–	PWMC0_ PWML0	O	RF	I/O	TCLK11	I	ISI_HSYN C	I	PIO, I, PU, ST
52	M5	L6	VDDIO	GPIO_AD	PD25	I/O	–	–	PWMC0_ PWML1	O	SPI0_NPCS1	I/O	URXD2	I	ISI_VSYN C	I	PIO, I, PU, ST
53	L6	M7	VDDIO	GPIO	PD26	I/O	–	–	PWMC0_ PWML2	O	TD	O	UTXD2	O	UTXD1	O	PIO, I, PU, ST
47	J6	M5	VDDIO	GPIO_AD	PD27	I/O	–	–	PWMC0_ PWML3	O	SPI0_NPCS3	O	TWD2	O	ISI_D8	I	PIO, I, PU, ST
71	K10	M12	VDDIO	GPIO_AD	PD28	I/O	WKUP5(1)	I	URXD3	I	CANRX1	I	TWCK2	O	ISI_D9	I	PIO, I, PU, ST
108	D10	B13	VDDIO	GPIO_AD	PD29	I/O	–	–	–	–	–	–	SDWE	O	–	–	PIO, I, PU, ST
34	M1	L2	VDDIO	GPIO_AD	PD30	I/O	AFE0_AD 0(5)	I	UTXD3	O	–	–	–	–	ISI_D10	I	PIO, I, PU, ST
2	D3	C3	VDDIO	GPIO_AD	PD31	I/O	–	–	QIO3	I/O	UTXD3	O	PCK2	O	ISI_D11	I	PIO, I, PU, ST
4	C2	C2	VDDIO	GPIO_AD	PE0	I/O	AFE1_AD 11(5)	I	D8	I/O	TIOA9	I/O	I2SC1_WS	I/O	–	–	PIO, I, PU, ST
6	A1	D2	VDDIO	GPIO_AD	PE1	I/O	–	–	D9	I/O	TIOB9	I/O	I2SC1_DO	O	–	–	PIO, I, PU, ST
7	B1	D1	VDDIO	GPIO_AD	PE2	I/O	–	–	D10	I/O	TCLK9	I	I2SC1_DI	I	–	–	PIO, I, PU, ST
10	E3	F1	VDDIO	GPIO_AD	PE3	I/O	AFE1_AD 10(5)	I	D11	I/O	TIOA10	I/O	–	–	–	–	PIO, I, PU, ST
27	K1	K2	VDDIO	GPIO_AD	PE4	I/O	AFE0_AD 4(5)	I	D12	I/O	TIOB10	I/O	–	–	–	–	PIO, I, PU, ST
28	L1	K3	VDDIO	GPIO_AD	PE5	I/O	AFE0_AD 3(5)	I	D13	I/O	TCLK10	I/O	–	–	–	–	PIO, I, PU, ST
3	C3	E4	VDDOUT	Power	VDDOUT	–	–	–	–	–	–	–	–	–	–	–	–
5	C1	C1	VDDIN	Power	VDDIN	–	–	–	–	–	–	–	–	–	–	–	–

24.4 Functional Description

The Watchdog Timer is used to prevent system lock-up if the software becomes trapped in a deadlock. It is supplied with VDDCORE. It restarts with initial values on processor reset.

The watchdog is built around a 12-bit down counter, which is loaded with the value defined in the field WDV of the Mode Register (WDT_MR). The Watchdog Timer uses the slow clock divided by 128 to establish the maximum watchdog period to be 16 seconds (with a typical slow clock of 32.768 kHz).

After a processor reset, the value of WDV is 0xFFF, corresponding to the maximum value of the counter with the external reset generation enabled (field WDRSTEN at 1 after a backup reset). This means that a default watchdog is running at reset, i.e., at power-up. The user can either disable the WDT by setting bit WDT_MR.WDDIS or reprogram the WDT to meet the maximum watchdog period the application requires.

When setting the WDDIS bit, and while it is set, the fields WDV and WDD must not be modified.

If the watchdog is restarted by writing into the Control Register (WDT_CR), WDT_MR must not be programmed during a period of time of three slow clock periods following the WDT_CR write access. In any case, programming a new value in WDT_MR automatically initiates a restart instruction.

WDT_MR can be written only once. Only a processor reset resets it. Writing WDT_MR reloads the timer with the newly programmed mode parameters.

In normal operation, the user reloads the watchdog at regular intervals before the timer underflow occurs, by setting bit WDT_CR.WDRSTT. The watchdog counter is then immediately reloaded from WDT_MR and restarted, and the slow clock 128 divider is reset and restarted. WDT_CR is write-protected. As a result, writing WDT_CR without the correct hard-coded key has no effect. If an underflow does occur, the “wdt_fault” signal to the Reset Controller is asserted if bit WDT_MR.WDRSTEN is set. Moreover, the bit WDUNF is set in the Status Register (WDT_SR).

The reload of the watchdog must occur while the watchdog counter is within a window between 0 and WDD. WDD is defined in WDT_MR.

Any attempt to restart the watchdog while the watchdog counter is between WDV and WDD results in a watchdog error, even if the watchdog is disabled. The bit WDT_SR.WDERR is updated and the “wdt_fault” signal to the Reset Controller is asserted.

Note that this feature can be disabled by programming a WDD value greater than or equal to the WDV value. In such a configuration, restarting the Watchdog Timer is permitted in the whole range [0; WDV] and does not generate an error. This is the default configuration on reset (the WDD and WDV values are equal).

The status bits WDUNF (Watchdog Underflow) and WDERR (Watchdog Error) trigger an interrupt, provided the bit WDT_MR.WDFIEN is set. The signal “wdt_fault” to the Reset Controller causes a watchdog reset if the WDRSTEN bit is set as already explained in the Reset Controller documentation. In this case, the processor and the Watchdog Timer are reset, and the WDERR and WDUNF flags are reset.

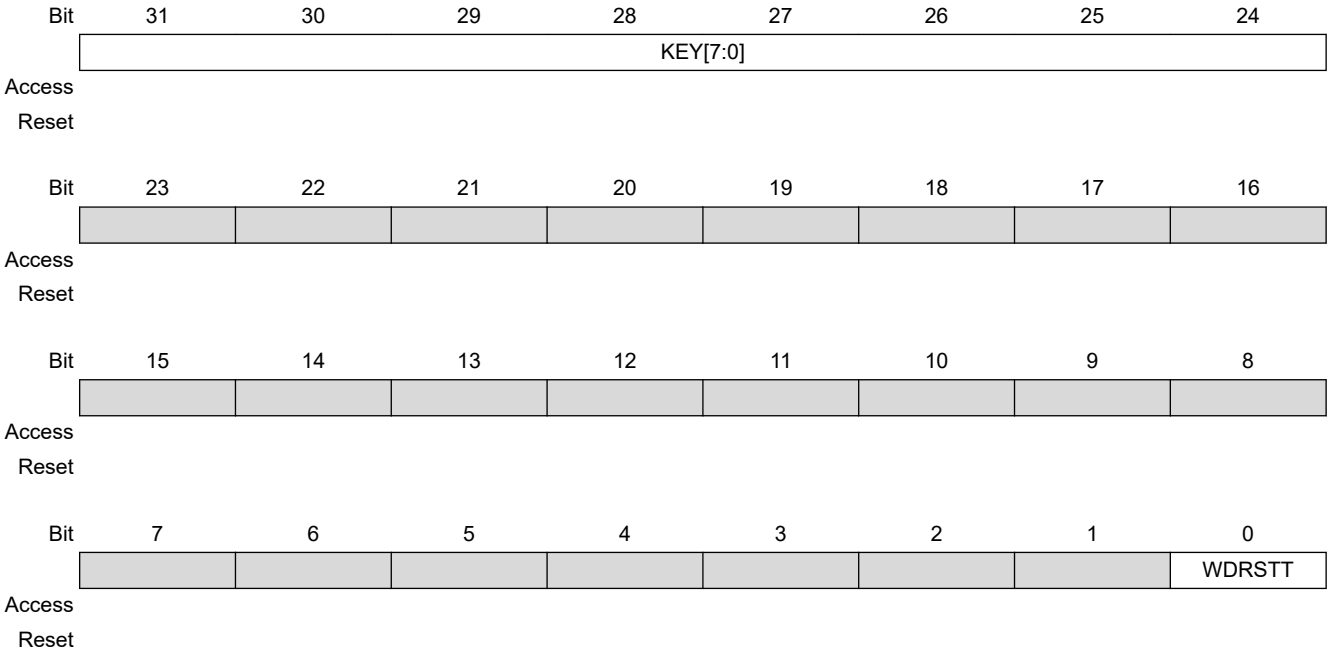
If a reset is generated or if WDT_SR is read, the status bits are reset, the interrupt is cleared, and the “wdt_fault” signal to the reset controller is deasserted.

Writing WDT_MR reloads and restarts the down counter.

While the processor is in debug state or in Sleep mode, the counter may be stopped depending on the value programmed for the bits WDIDLEHLT and WDDBGHLT in WDT_MR.

25.5.1 Reinforced Safety Watchdog Timer Control Register

Name: RSWDT_CR
Offset: 0x00
Property: Write-only



Bits 31:24 – KEY[7:0] Password

Value	Name	Description
0xC4	PASSWD	Writing any other value in this field aborts the write operation.

Bit 0 – WDRSTT Watchdog Restart

Value	Description
0	No effect.
1	Restarts the watchdog.

Read CKGR_MCFR until the MAINFRDY field is set, after which the user can read CKGR_MCFR.MAINF by performing an additional read. This provides the number of Main clock cycles that have been counted during a period of 16 SLCK cycles.

If MAINF = 0, switch MAINCK to the Main RC Oscillator by clearing CKGR_MOR.MOSCSEL. If MAINF ≠ 0, proceed to Step 6.

6. Set PLLA and Divider (if not required, proceed to Step 7.):
   All parameters needed to configure PLLA and the divider are located in CKGR_PLLAR.

   CKGR_PLLAR.DIVA is used to control the divider. This parameter can be programmed between 0 and 127. Divider output is divider input divided by DIVA parameter. By default, DIVA field is cleared which means that the divider and PLLA are turned off.

   CKGR_PLLAR.MULA is the PLLA multiplier factor. This parameter can be programmed between 0 and 62. If MULA is cleared, PLLA will be turned off, otherwise the PLLA output frequency is PLLA input frequency multiplied by (MULA + 1).

   CKGR_PLLAR.PLLACOUNT specifies the number of SLCK cycles before PMC_SR.LOCKA is set after CKGR_PLLAR has been written.

   Once CKGR_PLLAR has been written, the user must wait for PMC_SR.LOCKA to be set. This can be done either by polling PMC_SR.LOCKA or by waiting for the interrupt line to be raised if the associated interrupt source (LOCKA) has been enabled in PMC_IER. All fields in CKGR_PLLAR can be programmed in a single write operation. If MULA or DIVA is modified, the LOCKA bit goes low to indicate that PLLA is not yet ready. When PLLA is locked, LOCKA is set again. The user must wait for the LOCKA bit to be set before using the PLLA output clock.
7. Select MCK and HCLK:
   MCK and HCLK are configurable via PMC_MCKR.

   CSS is used to select the clock source of MCK and HCLK. By default, the selected clock source is MAINCK.

   PRES is used to define the HCLK and MCK prescaler.s The user can choose between different values (1, 2, 3, 4, 8, 16, 32, 64). Prescaler output is the selected clock source frequency divided by the PRES value.

   MDIV is used to define the MCK divider. It is possible to choose between different values (0, 1, 2, 3). MCK output is the HCLK frequency divided by 1, 2, 3 or 4, depending on the value programmed in MDIV.

   By default, MDIV is cleared, which indicates that the HCLK is equal to MCK.

   Once the PMC_MCKR has been written, the user must wait for PMC_SR.MCKRDY to be set. This can be done either by polling PMC_SR.MCKRDY or by waiting for the interrupt line to be raised if the associated interrupt source (MCKRDY) has been enabled in PMC_IER. PMC_MCKR must not be programmed in a single write operation. The programming sequence for PMC_MCKR is as follows:

   If a new value for PMC_MCKR.CSS corresponds to any of the available PLL clocks:

   a. Program PMC_MCKR.PRES.

   b. Wait for PMC_SR.MCKRDY to be set.

   c. Program PMC_MCKR.MDIV.

   d. Wait for PMC_SR.MCKRDY to be set.

Related Links

58. Electrical Characteristics for SAM V70/V71
59. Electrical Characteristics for SAM E70/S70

32.5.13 Programmable Schmitt Trigger

It is possible to configure each input for the Schmitt trigger. By default the Schmitt trigger is active. Disabling the Schmitt trigger is requested when using the QTouch® Library.

32.5.14 Parallel Capture Mode

32.5.14.1 Overview

The PIO Controller integrates an interface able to read data from a CMOS digital image sensor, a high-speed parallel ADC, a DSP synchronous port in Synchronous mode, etc. For better understanding and to ease reading, the following description uses an example with a CMOS digital image sensor.

32.5.14.2 Functional Description

The CMOS digital image sensor provides a sensor clock, an 8-bit data synchronous with the sensor clock and two data enables which are also synchronous with the sensor clock.

Figure 32-8. PIO Controller Connection with CMOS Digital Image Sensor

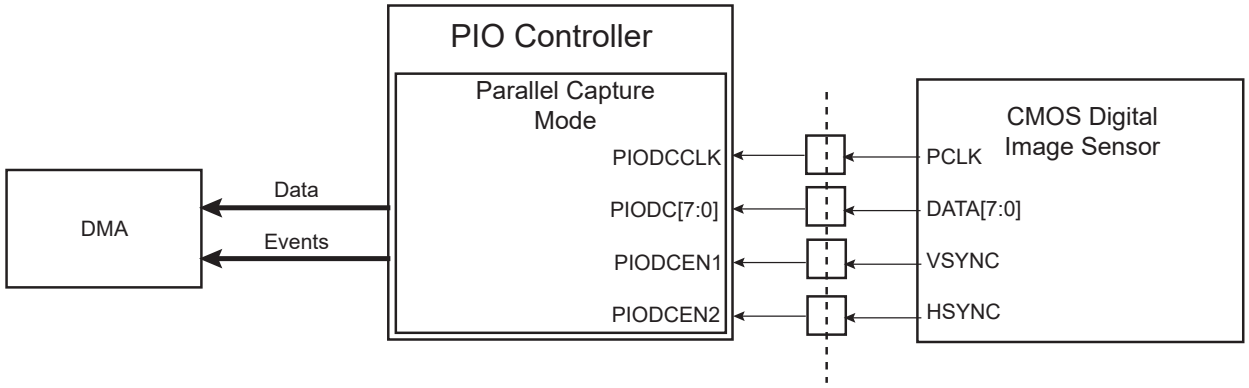
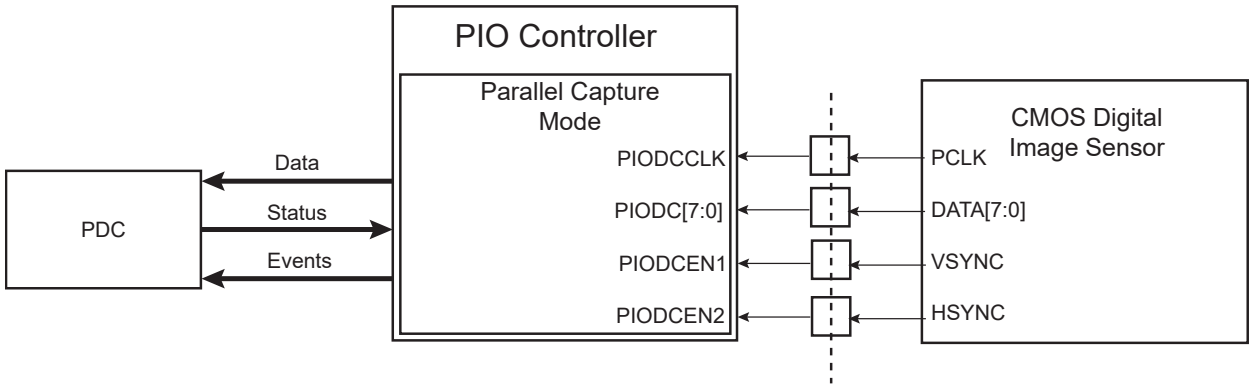


Figure 32-9.



As soon as the Parallel Capture mode is enabled by writing a one to the PCEN bit in PIO_PCMR, the I/O lines connected to the sensor clock (PIODCCLK), the sensor data (PIODC[7:0]) and the sensor data enable signals (PIODCEN1 and PIODCEN2) are configured automatically as inputs. To know which I/O lines are associated with the sensor clock, the sensor data and the sensor data enable signals, refer to the I/O multiplexing table(s) in the section “Package and Pinout”.

Once enabled, the Parallel Capture mode samples the data at rising edge of the sensor clock and resynchronizes it with the peripheral clock domain.

36.9.10 XDMAC Global Channel Status Register

Name: XDMAC_GS
Offset: 0x24
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 – ST XDMAC Channel x Status

Value	Description
0	This bit indicates that the channel x is disabled.
1	This bit indicates that the channel x is enabled. If a channel disable request is issued, this bit remains asserted until pending transaction is completed.

2. Configure the Slave mode.
3. Enable the DMA.
4. Wait for the DMA status flag indicating that the buffer transfer is complete.
5. Disable the DMA.
6. (Only if peripheral clock must be disabled) Wait for the TXCOMP flag to be raised in TWIHS_SR.

43.6.5.5.2 Data Receive with the DMA in Slave Mode

The following procedure shows an example to transmit data with DMA where the number of characters to receive is known.

1. Initialize the DMA (channels, memory pointers, size, etc.).
2. Configure the Slave mode.
3. Enable the DMA.
4. Wait for the DMA status flag indicating that the buffer transfer is complete.
5. Disable the DMA.
6. (Only if peripheral clock must be disabled) Wait for the TXCOMP flag to be raised in TWIHS_SR.

43.6.5.6 SMBus Mode

SMBus mode is enabled when a one is written to TWIHS_CR.SMBEN. SMBus mode operation is similar to I²C operation with the following exceptions:

- Only 7-bit addressing can be used.
- The SMBus standard describes a set of timeout values to ensure progress and throughput on the bus. These timeout values must be programmed into the TWIHS_SMBTR.
- Transmissions can optionally include a CRC byte, called Packet Error Check (PEC).
- A set of addresses have been reserved for protocol handling, such as alert response address (ARA) and host header (HH) address. Address matching on these addresses can be enabled by configuring the TWIHS_CR.

43.6.5.6.1 Packet Error Checking

Each SMBus transfer can optionally end with a CRC byte, called the PEC byte. Writing a one to TWIHS_CR.PECEN will send/check the PEC field in the current transfer. The PEC generator is always updated on every bit transmitted or received, so that PEC handling on the following linked transfers is correct.

In Slave Receiver mode, the master calculates a PEC value and transmits it to the slave after all data bytes have been transmitted. Upon reception of this PEC byte, the slave compares it to the PEC value it has computed itself. If the values match, the data was received correctly, and the slave returns an ACK to the master. If the PEC values differ, data was corrupted, and the slave returns a NACK value. TWIHS_SR.PECERR is set automatically if a PEC error occurred.

In Slave Transmitter mode, the slave calculates a PEC value and transmits it to the master after all data bytes have been transmitted. Upon reception of this PEC byte, the master compares it to the PEC value it has computed itself. If the values match, the data was received correctly. If the PEC values differ, data was corrupted, and the master must take appropriate action.

See Slave Read Write Flowcharts for detailed flowcharts.

43.6.5.6.2 Timeouts

The TWIHS SMBus Timing Register (TWIHS_SMBTR) configures the SMBus timeout values. If a timeout occurs, the slave leaves the bus. The TOUT bit is also set in TWIHS_SR.

Before using the SSC transmitter, the PIO controller must be configured to dedicate the SSC transmitter I/O lines to the SSC Peripheral mode.

44.7.2 Power Management

The SSC is not continuously clocked. The SSC interface may be clocked through the Power Management Controller (PMC), therefore the programmer must first configure the PMC to enable the SSC clock.

44.7.3 Interrupt

The SSC interface has an interrupt line connected to the interrupt controller. Handling interrupts requires programming the interrupt controller before configuring the SSC.

All SSC interrupts can be enabled/disabled configuring the SSC Interrupt Mask Register. Each pending and unmasked SSC interrupt asserts the SSC interrupt line. The SSC interrupt service routine can get the interrupt origin by reading the SSC Interrupt Status Register.

44.8 Functional Description

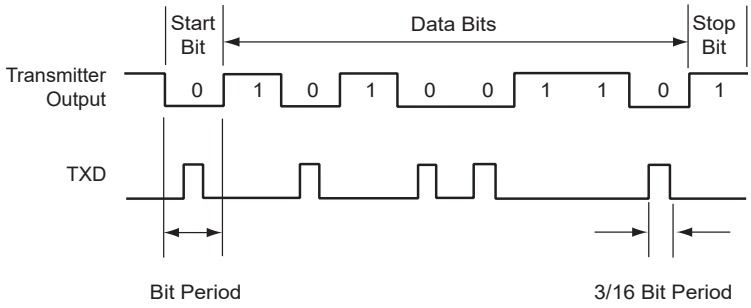
This section contains the functional description of the following: SSC Functional Block, Clock Management, Data Format, Start, Transmit, Receive and Frame Synchronization.

The receiver and transmitter operate separately. However, they can work synchronously by programming the receiver to use the transmit clock and/or to start a data transfer when transmission starts. Alternatively, this can be done by programming the transmitter to use the receive clock and/or to start a data transfer when reception starts. The transmitter and the receiver can be programmed to operate with the clock signals provided on either the TK or RK pins. This allows the SSC to support many Slave mode data transfers. The maximum clock speed allowed on the TK and RK pins is the peripheral clock divided by 2.

Baud Rate	Pulse Duration (3/16)
57.6 kbit/s	3.26 µs
115.2 kbit/s	1.63 µs

The following figure shows an example of character transmission.

Figure 46-33. IrDA Modulation



46.6.5.2 IrDA Baud Rate

The following table provides examples of CD values, baud rate error, and pulse duration. Note that the requirement on the maximum acceptable error of ±1.87% must be met.

Table 46-10. IrDA Baud Rate Error

Peripheral Clock	Baud Rate (bit/s)	CD	Baud Rate Error	Pulse Time (µs)
3,686,400	115,200	2	0.00%	1.63
20,000,000	115,200	11	1.38%	1.63
32,768,000	115,200	18	1.25%	1.63
40,000,000	115,200	22	1.38%	1.63
3,686,400	57,600	4	0.00%	3.26
20,000,000	57,600	22	1.38%	3.26
32,768,000	57,600	36	1.25%	3.26
40,000,000	57,600	43	0.93%	3.26
3,686,400	38,400	6	0.00%	4.88
20,000,000	38,400	33	1.38%	4.88
32,768,000	38,400	53	0.63%	4.88
40,000,000	38,400	65	0.16%	4.88
3,686,400	19,200	12	0.00%	9.77
20,000,000	19,200	65	0.16%	9.77
32,768,000	19,200	107	0.31%	9.77
40,000,000	19,200	130	0.16%	9.77
3,686,400	9,600	24	0.00%	19.53

47.6.1 UART Control Register

Name: UART_CR
Offset: 0x00
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				REQCLR				RSTSTA
Access				W				W
Reset				–				–

Bit	7	6	5	4	3	2	1	0
	TXDIS	TXEN	RXDIS	RXEN	RSTTX	RSTRX		
Access	W	W	W	W	W	W		
Reset	–	–	–	–	–	–		

Bit 12 – REQCLR Request Clear

- SleepWalking enabled:

0: No effect.

1: Bit REQCLR clears the potential clock request currently issued by UART, thus the potential system wake-up is cancelled.

- SleepWalking disabled:

0: No effect.

1: Bit REQCLR restarts the comparison trigger to enable receive holding register loading.

Bit 8 – RSTSTA Reset Status

Value	Description
0	No effect.
1	Resets the status bits PARE, FRAME, CMP and OVRE in the UART_SR.

Bit 7 – TXDIS Transmitter Disable

Value	Description
0	No effect.
1	The transmitter is disabled. If a character is being processed and a character has been written in the UART_THR and RSTTX is not set, both characters are completed before the transmitter is stopped.

Bit 6 – TXEN Transmitter Enable

Value	Description
0	No effect.
1	The transmitter is enabled if TXDIS is 0.

Bit 5 – RXDIS Receiver Disable

Value	Description
0	No effect.
1	The receiver is disabled. If a character is being processed and RSTRX is not set, the character is completed before the receiver is stopped.

Bit 4 – RXEN Receiver Enable

Value	Description
0	No effect.
1	The receiver is enabled if RXDIS is 0.

Bit 3 – RSTTX Reset Transmitter

Value	Description
0	No effect.
1	The transmitter logic is reset and disabled. If a character is being transmitted, the transmission is aborted.

Bit 2 – RSTRX Reset Receiver

Value	Description
0	No effect.
1	The receiver logic is reset and disabled. If a character is being received, the reception is aborted.

49.6.37 MCAN Tx Buffer Element Size Configuration

Name: MCAN_TXESC
Offset: 0xC8
Reset: 0x00000000
Property: Read/Write

This register can only be written if the bits CCE and INIT are set in MCAN CC Control Register.

Configures the number of data bytes belonging to a Tx Buffer element. Data field sizes > 8 bytes are intended for CAN FD operation only.

In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size MCAN_TXESC.TBDS, the bytes not defined by the Tx Buffer are transmitted as “0xCC” (padding bytes).

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						TBDS[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – TBDS[2:0] Tx Buffer Data Field Size

Value	Name	Description
0	8_BYTE	8-byte data field
1	12_BYTE	12-byte data field
2	16_BYTE	16-byte data field
3	20_BYTE	20-byte data field
4	24_BYTE	24-byte data field
5	32_BYTE	32-byte data field
6	48_BYTE	48- byte data field
7	64_BYTE	64-byte data field

49.6.44 MCAN Transmit Buffer Cancellation Finished Interrupt Enable

Name: MCAN_TXBCIE
Offset: 0xE4
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – CFIEx Cancellation Finished Interrupt Enable for Transmit Buffer x
Each Transmit Buffer has its own Cancellation Finished Interrupt Enable bit.

Value	Description
0	Cancellation finished interrupt disabled.
1	Cancellation finished interrupt enabled.

53.7.9 DACC Interrupt Disable Register

Name: DACC_IDR
Offset: 0x28
Reset: –
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			EOC1	EOC0			TXRDY1	TXRDY0
Access			W	W			W	W
Reset			0	–			0	–

Bits 4, 5 – EOCx End of Conversion Interrupt Disable of channel x

Bits 0, 1 – TXRDYx Transmit Ready Interrupt Disable of channel x

Master Read Mode

Slave Read Mode

In slave mode, SPCK is the input clock for the SPI. The max SPCK frequency is given by setup and hold timings SPI_7/SPI_8(or SPI_{10}/SPI_{11}). Since this gives a frequency well above the pad limit, the limit in slave read mode is given by SPCK pad.

Slave Write Mode

58.13.1.6.2 SPI Timings

Timings are given in the following domains:

- 1.8V domain: V_{DDIO} from 1.7V to 1.95V, maximum external capacitor = 20 pF
- 3.3V domain: V_{DDIO} from 2.85V to 3.6V, maximum external capacitor = 40 pF

Table 58-56. SPI Timings

Symbol	Parameter	Conditions	Min	Max	Unit
SPI_0	MISO Setup time before SPCK rises (master)	3.3V domain	12.4	–	ns
		1.8V domain	14.6	–	ns
SPI_1	MISO Hold time after SPCK rises (master)	3.3V domain	0	–	ns
		1.8V domain	0	–	ns
SPI_2	SPCK rising to MOSI Delay (master)	3.3V domain	-3.7	2.2	ns
		1.8V domain	-3.8	2.7	ns
SPI_3	MISO Setup time before SPCK falls (master)	3.3V domain	12.6	–	ns
		1.8V domain	15.13	–	ns
SPI_4	MISO Hold time after SPCK falls (master)	3.3V domain	0	–	ns
		1.8V domain	0	–	ns
SPI_5	SPCK falling to MOSI Delay (master)	3.3V domain	-3.6	2.0	ns
		1.8V domain	-3.3	2.8	ns
SPI_6	SPCK falling to MISO Delay (slave)	3.3V domain	3.0	11.9	ns
		1.8V domain	3.5	13.9	ns
SPI_7	MOSI Setup time before SPCK rises (slave)	3.3V domain	1.2	–	ns
		1.8V domain	1.5	–	ns
SPI_8	MOSI Hold time after SPCK rises (slave)	3.3V domain	0.6	–	ns
		1.8V domain	0.8	–	ns
SPI_9	SPCK rising to MISO Delay (slave)	3.3V domain	3.0	12.0	ns
		1.8V domain	3.4	13.7	ns
SPI_{10}	MOSI Setup time before SPCK falls (slave)	3.3V domain	1.2	–	ns
		1.8V domain	1.5	–	ns
SPI_{11}	MOSI Hold time after SPCK falls (slave)	3.3V domain	0.6	–	ns

  - Calculated as the difference in current measurement after enabling then disabling the corresponding clock.
  - Measured when the peripheral is active an doing transfers
- Static and dynamic power consumption of the I/Os

59.3.1 Backup Mode Current Consumption and Wake-Up Time

The Backup mode configurations and measurements are defined as follows:

- Embedded slow clock RC oscillator is enabled
- Supply Monitor on V_{DDIO} is disabled
- RTC is running
- RTT is enabled on 1 Hz mode
- BOD is disabled
- One WKUPx enabled
- Current measurement on AMP1 with and without the 1 Kbyte backup SRAM
- Measurements are made at ambient temperature

Figure 59-5. Measurement Setup

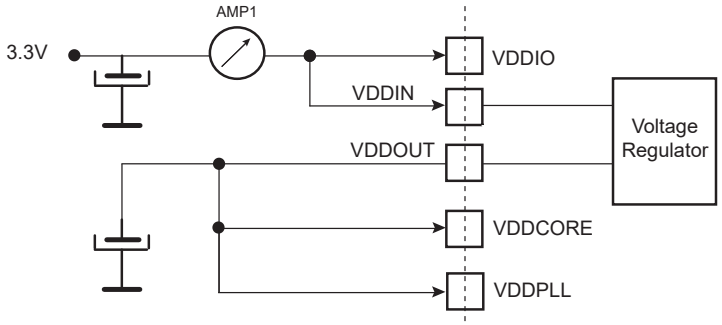


Table 59-11. Worst Case Power Consumption for Backup Mode with 1 Kbyte BACKUP SRAM On

Total Consumption	Worst Case Value			Unit
	at 25°C	at 85°C	at 105°C	
Conditions	AMP1	AMP1	AMP1	
V_{DDIO} = 3.6V	8.4	42	64	µA
V_{DDIO} = 3.3V	8	39	61	µA
V_{DDIO} = 3.0V	7.6	38	59	µA
V_{DDIO} = 2.5V	5.2	37	58	µA
V_{DDIO} = 1.7V	3.8	35	56	µA

Date	Changes
	Section 10.1.5.9 “Fast Flash Programming Interface”: removed ‘serial JTAG interface’.
	Section 11. “Event System” Table 11-1 “ Event Mapping List“: in row “Audio clock recovery from Ethernet’ changed the text in Description column.
	Section 13. “Peripherals” Table 13-1 “Peripheral Identifiers“: modfied content of column ‘Description’ for clarity. Section 13.2 “Peripheral Signal Multiplexing on I/O Lines”: corrected PIOC to PIOD for 100-pin version. Moved Section 13.3 “Peripheral Mapping to DMA” to Section 35.3 “DMA Controller Peripheral Connections”.
24-Feb-15	Section 15. “Debug and Test Features” Section 15.1 “Description”: removed references to JTAG Debug Port and JTAG-DP. Updated Figure 15-1 “Debug and Test Block Diagram”: added Cortex-M7, ETM and PCK3 blocks and trace pins. Renamed block ‘SWJ-DP’ to ‘SW-DP’. Table 15-1 “Debug and Test Signal List”: removed TRACECTL. Updated Figure 15-4 “Debug Architecture”. added ETM and Trace Port blocks. Removed TPIU. Section 15.6.5 “Serial Wire Debug Port (SW-DP) Pins”: removed all references to JTAG Debug Port and JTAG-DP. Section 15.6.6 “Embedded Trace Module (ETM) Pins”: removed TRACECTL from bullet points. Updated Section 15.6.7 “Flash Patch Breakpoint (FPB)” . Section 15.6.9.2 “Asynchronous Mode”: removed reference to JTAG Debug Port and JTAG debug mode.
	Section 16. “SAM-BA Boot Program” Section 16.6.4 “In Application Programming (IAP) Feature”: replaced software code example.
	Section 18. “Bus Matrix (MATRIX)” Table 18-3 “Master to Slave Access”: changed Master 4/Slave 4 access from possible (“x”) to not possble (‘-”) Table 18-4 “Register Mapping”: changed reset value for CCFG_SYSIO register. Section 18.12.7 “System I/O and CAN1 Configuration Register”: corrected typo in CAN1DMABA bit name. Section 18.11 “Register Write Protection”: replaced “The WPVS bit is automatically cleared after reading the MATRIX_WPSR” with “The WPVS flag is reset by writing the MATRIX_WPMR with the appropriate access key WPKEY”

Date	Changes
24-Feb-15	Section 55. “Advanced Encryption Standard (AES)” Section 55.4.5.2 “DMA Mode”: removed references to ‘BTC’ throughout.
	Section 56. “Electrical Characteristics” Table 56-1 “Absolute Maximum Ratings*“: added reference to Note 1 for 64-pin QFN package. Table 56-2 “DC Characteristics”: updated conditions for V_{IL}, V_{IH}, V_{OH}, V_{OL}, I_O, R_{PULLUP}, $R_{PULLDOWN}$, $R_{SERIAL.}$ Added parameter Flash Active Current characteristics. Added parameter Static Current. Modified Note (1) below table. Table 56-3 “1.2V Voltage Regulator Characteristics”: removed note on VDDIO voltage at power-up (was Note 3). Updated note on VDDIO voltage value. Changed values of CD_{OUT}. Changed conditions for parameter t_{START} and CD_{OUT} value in Note 2. Table 56-4 “Core Power Supply Brownout Detector Characteristics”: updated all values. Changed Note 1. Table 56-6 “VDDIO Supply Monitor”: updated values for $T_{ACCURACY}$ Table 56-9. “DC Flash Characteristics” moved to Table 56-2 “DC Characteristics”. Section 56.3.2.1 “Sleep Mode Conditions”: corrected number of WKUP pins. Added Section 56.3.6 “I/O Switching Power Consumption”. Table 56-21 “32 kHz RC Oscillator Characteristics”: changed max values to TBD for t_{START}, I_{DDON} and $I_{DDON\_STANDBY}$. Table 56-25 “3 to 20 MHz Crystal Oscillator Characteristics”: for t_{START} and $I_{DD_ON,}$changed max values to TBD. Added parameter $I_{DD.\_STANDBY.}$ Table 56-26 “Crystal Characteristics”: ESR: added new row with condition Fundamental at 3 MHz. Changed max values for 8 and 12 MHz. Table 56-29 “PLLA Characteristics”: changed max value of f_{IN}. Added parameter I_{DD_STDBY} Added Section 56.6 “PLLUSB Characteristics”> Updated section Section 56.7 “USB Transceiver Characteristics”. Moved Section 56.8 MediaLB to Section 56.8. Section 56.9 “AFE Characteristics”: changed numbering of sub-sections throughout. - Removed bullet on min and max data. - Changed all occurrences of ADVREFP to VREP, and of ADVREFN to VREFN throughout section. - Changed all occurrences of ADC to AFE, where relevant. - Modified Figure 56-11 “Single-ended Mode AFE” and Figure 56-12 “Differential Mode AFE”. - Table 56-36 “Power Supply Characteristics”: updated I_{VDDIN} conditions in and changed max values. Changed max values for $I_{VDDCORE.}$ Removed Note 1 due to incorrect cross-reference. Added Note 3 on current consumption.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: http://www.microchip.com/support Web Address: www.microchip.com **Atlanta** Duluth, GA Tel: 678-957-9614 Fax: 678-957-1455 **Austin, TX** Tel: 512-257-3370 **Boston** Westborough, MA Tel: 774-760-0087 Fax: 774-760-0088 **Chicago** Itasca, IL Tel: 630-285-0071 Fax: 630-285-0075 **Dallas** Addison, TX Tel: 972-818-7423 Fax: 972-818-2924 **Detroit** Novi, MI Tel: 248-848-4000 **Houston, TX** Tel: 281-894-5983 **Indianapolis** Noblesville, IN Tel: 317-773-8323 Fax: 317-773-5453 Tel: 317-536-2380 **Los Angeles** Mission Viejo, CA Tel: 949-462-9523 Fax: 949-462-9608 Tel: 951-273-7800 **Raleigh, NC** Tel: 919-844-7510 **New York, NY** Tel: 631-435-6000 **San Jose, CA** Tel: 408-735-9110 Tel: 408-436-4270 **Canada - Toronto** Tel: 905-695-1980 Fax: 905-695-2078	**Australia - Sydney** Tel: 61-2-9868-6733 **China - Beijing** Tel: 86-10-8569-7000 **China - Chengdu** Tel: 86-28-8665-5511 **China - Chongqing** Tel: 86-23-8980-9588 **China - Dongguan** Tel: 86-769-8702-9880 **China - Guangzhou** Tel: 86-20-8755-8029 **China - Hangzhou** Tel: 86-571-8792-8115 **China - Hong Kong SAR** Tel: 852-2943-5100 **China - Nanjing** Tel: 86-25-8473-2460 **China - Qingdao** Tel: 86-532-8502-7355 **China - Shanghai** Tel: 86-21-3326-8000 **China - Shenyang** Tel: 86-24-2334-2829 **China - Shenzhen** Tel: 86-755-8864-2200 **China - Suzhou** Tel: 86-186-6233-1526 **China - Wuhan** Tel: 86-27-5980-5300 **China - Xian** Tel: 86-29-8833-7252 **China - Xiamen** Tel: 86-592-2388138 **China - Zhuhai** Tel: 86-756-3210040	**India - Bangalore** Tel: 91-80-3090-4444 **India - New Delhi** Tel: 91-11-4160-8631 **India - Pune** Tel: 91-20-4121-0141 **Japan - Osaka** Tel: 81-6-6152-7160 **Japan - Tokyo** Tel: 81-3-6880- 3770 **Korea - Daegu** Tel: 82-53-744-4301 **Korea - Seoul** Tel: 82-2-554-7200 **Malaysia - Kuala Lumpur** Tel: 60-3-7651-7906 **Malaysia - Penang** Tel: 60-4-227-8870 **Philippines - Manila** Tel: 63-2-634-9065 **Singapore** Tel: 65-6334-8870 **Taiwan - Hsin Chu** Tel: 886-3-577-8366 **Taiwan - Kaohsiung** Tel: 886-7-213-7830 **Taiwan - Taipei** Tel: 886-2-2508-8600 **Thailand - Bangkok** Tel: 66-2-694-1351 **Vietnam - Ho Chi Minh** Tel: 84-28-5448-2100	**Austria - Wels** Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 **Denmark - Copenhagen** Tel: 45-4450-2828 Fax: 45-4485-2829 **Finland - Espoo** Tel: 358-9-4520-820 **France - Paris** Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 **Germany - Garching** Tel: 49-8931-9700 **Germany - Haan** Tel: 49-2129-3766400 **Germany - Heilbronn** Tel: 49-7131-67-3636 **Germany - Karlsruhe** Tel: 49-721-625370 **Germany - Munich** Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 **Germany - Rosenheim** Tel: 49-8031-354-560 **Israel - Ra'anana** Tel: 972-9-744-7705 **Italy - Milan** Tel: 39-0331-742611 Fax: 39-0331-466781 **Italy - Padova** Tel: 39-049-7625286 **Netherlands - Drunen** Tel: 31-416-690399 Fax: 31-416-690340 **Norway - Trondheim** Tel: 47-7289-7561 **Poland - Warsaw** Tel: 48-22-3325737 **Romania - Bucharest** Tel: 40-21-407-87-50 **Spain - Madrid** Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 **Sweden - Gothenberg** Tel: 46-31-704-60-40 **Sweden - Stockholm** Tel: 46-8-5090-4654 **UK - Wokingham** Tel: 44-118-921-5800 Fax: 44-118-921-5820