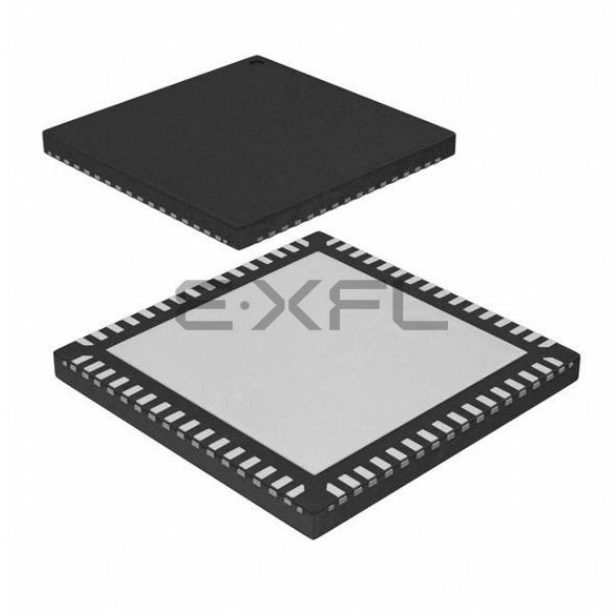


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M7 |
| Core Size | 32-Bit Single-Core |
| Speed | 300MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, SSC, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 44 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 384K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 5x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsams70j20b-mnt |

**Table 8-1. System I/O Configuration Pin List**

| CCFG_SYSIO Bit Number | Default Function After Reset | Other Function | Constraints for Normal Start | Configuration |
|---|---|---|---|---|
| 12 | ERASE | PB12 | Low Level at startup (see **Note 1**) | In Matrix User Interface Registers (Refer to the 19.4.7 CCFG_SYSIO register) |
| 7 | TCK/SWCLK | PB7 | – | |
| 6 | TMS/SWDIO | PB6 | – | |
| 5 | TDO/ TRACESWO | PB5 | – | |
| 4 | TDI | PB4 | – | |
| – | PA7 | XIN32 | – | (see **Note 2**) |
| – | PA8 | XOUT32 | – | |
| – | PB9 | XIN | – | (see **Note 3**) |
| – | PB8 | XOUT | – | |

**Note:**

1. If PB12 is used as PIO input in user applications, a low level must be ensured at startup to prevent Flash erase before the user application sets PB12 into PIO mode.
2. Refer to 23.4.2 Slow Clock Generator.
3. Refer to 30.5.3 Main Crystal Oscillator.

### 8.2.1 Serial Wire Debug Port (SW-DP) Pins

The SW-DP pins SWCLK and SWDIO are commonly provided on a standard 20-pin JTAG connector defined by ARM. For more details about voltage reference and reset state, refer to Table 4-1.

At startup, SW-DP pins are configured in SW-DP mode to allow connection with debugging probe. For more details, refer to 16. Debug and Test Features.

SW-DP pins can be used as standard I/Os to provide users more general input/output pins when the debug port is not needed in the end application. Mode selection between SW-DP mode (System IO mode) and general IO mode is performed through the AHB Matrix Special Function Registers (MATRIX_SFR). Configuration of the pad for pull-up, triggers, debouncing and glitch filters is possible regardless of the mode.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pulldown resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

The JTAG Debug Port TDI, TDO, TMS and TCK is inactive. It is provided for Boundary Scan Manufacturing Test purpose only.

### 8.2.2 Embedded Trace Module (ETM) Pins

The Embedded Trace Module (ETM) depends on the Trace Port Interface Unit (TPIU) to export data out of the system.

The TPUI features the following pins:

| Instance ID | Instance Name | NVIC Interrupt | PMC Clock Control | Description |
|---|---|---|---|---|
| 20 | TWIHS1 | X | X | Two-wire Interface (I2C-compatible) |
| 21 | SPI0 | X | X | Serial Peripheral Interface |
| 22 | SSC | X | X | Synchronous Serial Controller |
| 23 | TC0_CHANNEL0 | X | X | 16-bit Timer Counter 0, Channel 0 |
| 24 | TC0_CHANNEL1 | X | X | 16-bit Timer Counter 0, Channel 1 |
| 25 | TC0_CHANNEL2 | X | X | 16-bit Timer Counter 0, Channel 2 |
| 26 | TC1_CHANNEL0 | X | X | 16-bit Timer Counter 1, Channel 0 |
| 27 | TC1_CHANNEL1 | X | X | 16-bit Timer Counter 1, Channel 1 |
| 28 | TC1_CHANNEL2 | X | X | 16-bit Timer Counter 1, Channel 2 |
| 29 | AFEC0 | X | X | Analog Front-End Controller |
| 30 | DACC | X | X | Digital-to-Analog Converter |
| 31 | PWM0 | X | X | Pulse Width Modulation Controller |
| 32 | ICM | X | X | Integrity Check Monitor |
| 33 | ACC | X | X | Analog Comparator Controller |
| 34 | USBHS | X | X | USB Host / Device Controller |
| 35 | MCAN0 | X | X | CAN IRQ Line 0 |
| 36 | MCAN0 | INT1 | – | CAN IRQ Line 1 |
| 37 | MCAN1 | X | X | CAN IRQ Line 0 |
| 38 | MCAN1 | INT1 | – | CAN IRQ Line 1 |
| 39 | GMAC | X | X | Ethernet MAC |
| 35 | – | – | – | Reserved |
| 36 | – | – | – | Reserved |
| 37 | – | – | – | Reserved |
| 38 | – | – | – | Reserved |
| 39 | – | – | – | Reserved |
| 40 | AFEC1 | X | X | Analog Front End Controller |
| 41 | TWIHS2 | X | X | Two-wire Interface |
| 42 | SPI1 | X | X | Serial Peripheral Interface |
| 43 | QSPI | X | X | Quad I/O Serial Peripheral Interface |
| 44 | UART2 | X | X | Universal Asynchronous Receiver/ Transmitter |

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 15:8 | | | M3PR[1:0] | | | | M2PR[1:0] | |
| | | 23:16 | | | M5PR[1:0] | | | | M4PR[1:0] | |
| | | 31:24 | | | M7PR[1:0] | | | | M6PR[1:0] | |
| 0xAC | MATRIX_PRBS5 | 7:0 | | | M9PR[1:0] | | | | M8PR[1:0] | |
| | | 15:8 | | | M11PR[1:0] | | | | M10PR[1:0] | |
| | | 23:16 | | | | | | | M12PR[1:0] | |
| | | 31:24 | | | | | | | | |
| 0xB0 | MATRIX_PRAS6 | 7:0 | | | M1PR[1:0] | | | | M0PR[1:0] | |
| | | 15:8 | | | M3PR[1:0] | | | | M2PR[1:0] | |
| | | 23:16 | | | M5PR[1:0] | | | | M4PR[1:0] | |
| | | 31:24 | | | M7PR[1:0] | | | | M6PR[1:0] | |
| 0xB4 | MATRIX_PRBS6 | 7:0 | | | M9PR[1:0] | | | | M8PR[1:0] | |
| | | 15:8 | | | M11PR[1:0] | | | | M10PR[1:0] | |
| | | 23:16 | | | | | | | M12PR[1:0] | |
| | | 31:24 | | | | | | | | |
| 0xB8 | MATRIX_PRAS7 | 7:0 | | | M1PR[1:0] | | | | M0PR[1:0] | |
| | | 15:8 | | | M3PR[1:0] | | | | M2PR[1:0] | |
| | | 23:16 | | | M5PR[1:0] | | | | M4PR[1:0] | |
| | | 31:24 | | | M7PR[1:0] | | | | M6PR[1:0] | |
| 0xBC | MATRIX_PRBS7 | 7:0 | | | M9PR[1:0] | | | | M8PR[1:0] | |
| | | 15:8 | | | M11PR[1:0] | | | | M10PR[1:0] | |
| | | 23:16 | | | | | | | M12PR[1:0] | |
| | | 31:24 | | | | | | | | |
| 0xC0 | MATRIX_PRAS8 | 7:0 | | | M1PR[1:0] | | | | M0PR[1:0] | |
| | | 15:8 | | | M3PR[1:0] | | | | M2PR[1:0] | |
| | | 23:16 | | | M5PR[1:0] | | | | M4PR[1:0] | |
| | | 31:24 | | | M7PR[1:0] | | | | M6PR[1:0] | |
| 0xC4 | MATRIX_PRBS8 | 7:0 | | | M9PR[1:0] | | | | M8PR[1:0] | |
| | | 15:8 | | | M11PR[1:0] | | | | M10PR[1:0] | |
| | | 23:16 | | | | | | | M12PR[1:0] | |
| | | 31:24 | | | | | | | | |
| 0xC8 ... 0xFF | Reserved | | | | | | | | | |
| 0x0100 | MATRIX_MRCR | 7:0 | RCB7 | RCB6 | RCB5 | RCB4 | RCB3 | RCB2 | RCB1 | RCB0 |
| | | 15:8 | | | | RCB12 | RCB11 | RCB10 | RCB9 | RCB8 |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0104 ... 0x010F | Reserved | | | | | | | | | |
| 0x0110 | CCFG_CAN0 | 7:0 | Reserved[7:0] | | | | | | | |
| | | 15:8 | | | | | | | | Reserved[8:8] |
| | | 23:16 | CAN0DMABA[7:0] | | | | | | | |
| | | 31:24 | CAN0DMABA[15:8] | | | | | | | |
| 0x0114 | CCFG_SYSIO | 7:0 | SYSIO7 | SYSIO6 | SYSIO5 | SYSIO4 | | | | |

#### 32.6.1.48 PIO Schmitt Trigger Register

**Name:** PIO_SCHMITT
**Offset:** 0x0100
**Reset:** 0x00000000
**Property:** Read/Write

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | SCHMITT31 | SCHMITT30 | SCHMITT29 | SCHMITT28 | SCHMITT27 | SCHMITT26 | SCHMITT25 | SCHMITT24 |
| Access | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | SCHMITT23 | SCHMITT22 | SCHMITT21 | SCHMITT20 | SCHMITT19 | SCHMITT18 | SCHMITT17 | SCHMITT16 |
| Access | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | SCHMITT15 | SCHMITT14 | SCHMITT13 | SCHMITT12 | SCHMITT11 | SCHMITT10 | SCHMITT9 | SCHMITT8 |
| Access | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SCHMITT7 | SCHMITT6 | SCHMITT5 | SCHMITT4 | SCHMITT3 | SCHMITT2 | SCHMITT1 | SCHMITT0 |
| Access | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – SCHMITT** PIO Schmitt Trigger Control

| Value | Description |
|---|---|
| 0 | Schmitt trigger is enabled. |
| 1 | Schmitt trigger is disabled. |

#### 36.6.2.1 Descriptor Structure Microblock Control Member

**Name:** MBR_UBC
**Property:** Read-only

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | NVIEW[1:0] | | NDEN | NSEN | NDE |
| Access | | | | R | R | R | R | R |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | UBLEN[23:16] | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | UBLEN[15:8] | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | | | | | | | | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | UBLEN[7:0] | | | | | | | |
| Access | R | R | R | R | R | R | R | R |
| Reset | | | | | | | | |

**Bits 28:27 – NVIEW[1:0]** Next Descriptor View

| Value | Name | Description |
|---|---|---|
| 0 | NDV0 | Next Descriptor View 0 |
| 1 | NDV1 | Next Descriptor View 1 |
| 2 | NDV2 | Next Descriptor View 2 |
| 3 | NDV3 | Next Descriptor View 3 |

**Bit 26 – NDEN** Next Descriptor Destination Update

| Value | Description |
|---|---|
| 0 | Destination parameters remain unchanged. |
| 1 | Destination parameters are updated when the descriptor is retrieved. |

**Bit 25 – NSEN** Next Descriptor Source Update

| Value | Description |
|---|---|
| 0 | Source parameters remain unchanged. |
| 1 | Source parameters are updated when the descriptor is retrieved. |

**Bit 24 – NDE** Next Descriptor Enable

| Value | Description |
|---|---|
| 0 | Descriptor fetch is disabled. |
| 1 | Descriptor fetch is enabled. |

### 36.9.14 XDMAC Global Channel Read Write Resume Register

**Name:** XDMAC_GRWR
**Offset:** 0x34
**Reset:** –
**Property:** Write-only

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | RWR23 | RWR22 | RWR21 | RWR20 | RWR19 | RWR18 | RWR17 | RWR16 |
| Access | W | W | W | W | W | W | W | W |
| Reset | – | – | – | – | – | – | – | – |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | RWR15 | RWR14 | RWR13 | RWR12 | RWR11 | RWR10 | RWR9 | RWR8 |
| Access | W | W | W | W | W | W | W | W |
| Reset | – | – | – | – | – | – | – | – |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | RWR7 | RWR6 | RWR5 | RWR4 | RWR3 | RWR2 | RWR1 | RWR0 |
| Access | W | W | W | W | W | W | W | W |
| Reset | – | – | – | – | – | – | – | – |

**Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 – RWRx** XDMAC Channel x Read Write Resume

| Value | Description |
|---|---|
| 0 | No effect. |
| 1 | Read and write requests are serviced. |

### 36.9.24 XDMAC Channel x Next Descriptor Address Register [x = 0..23]

**Name:** XDMAC_CNDA
**Offset:** 0x68 + n*0x40 [n=0..23]
**Reset:** 0x00000000
**Property:** Read/Write

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | NDA[29:22] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | NDA[21:14] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | NDA[13:6] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | NDA[5:0] | | | | | | | NDAIF |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | | 0 |

**Bits 31:2 – NDA[29:0]** Channel x Next Descriptor Address
The 30-bit width of the NDA field represents the next descriptor address range 31:2. The descriptor is word-aligned and the two least significant register bits 1:0 are ignored.

**Bit 0 – NDAIF** Channel x Next Descriptor Interface

| Value | Description |
|---|---|
| 0 | The channel descriptor is retrieved through system interface 0. |
| 1 | The channel descriptor is retrieved through system interface 1. |

| Value | Name | Description |
|---|---|---|
| | | Byte 3 B/G(MSB) |
| 3 | MODE3 | Byte 0 G(LSB)/B<br>Byte 1 R/G(MSB)<br>Byte 2 G(LSB)/B<br>Byte 3 R/G(MSB) |

**Bits 29:28 – YCC_SWAP[1:0]** YCrCb Format Swap Mode
Defines the YCC image data.

| Value | Name | Description |
|---|---|---|
| 0 | DEFAULT | Byte 0 Cb(i)<br>Byte 1 Y(i)<br>Byte 2 Cr(i)<br>Byte 3 Y(i+1) |
| 1 | MODE1 | Byte 0 Cr(i)<br>Byte 1 Y(i)<br>Byte 2 Cb(i)<br>Byte 3 Y(i+1) |
| 2 | MODE2 | Byte 0 Y(i)<br>Byte 1 Cb(i)<br>Byte 2 Y(i+1)<br>Byte 3 Cr(i) |
| 3 | MODE3 | Byte 0 Y(i)<br>Byte 1 Cr(i)<br>Byte 2 Y(i+1)<br>Byte 3 Cb(i) |

**Bits 26:16 – IM_HSIZE[10:0]** Horizontal Size of the Image Sensor [0..2047]
If 8-bit Grayscale mode is enabled, IM_HSIZE = (Horizontal size/2) - 1.

Else IM_HSIZE = Horizontal size - 1.

**Bit 15 – COL_SPACE** Color Space for the Image Data

| Value | Description |
|---|---|
| 0 | YCbCr. |
| 1 | RGB. |

**Bit 14 – RGB_SWAP** RGB Format Swap Mode
The RGB_SWAP has no effect when Grayscale mode is enabled.

### 37.6.12 ISI Interrupt Enable Register

**Name:** ISI_IER
**Offset:** 0x2C
**Reset:** –
**Property:** Write-only

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | FR_OVR | CRC_ERR | C_OVR | P_OVR |
| Access | | | | | W | W | W | W |
| Reset | | | | | – | – | – | – |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | CXFR_DONE | PXFR_DONE |
| Access | | | | | | | W | W |
| Reset | | | | | | | – | – |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | VSYNC | | |
| Access | | | | | | W | | |
| Reset | | | | | | – | | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | SRST | DIS_DONE | |
| Access | | | | | | W | W | |
| Reset | | | | | | – | – | |

**Bit 27 – FR_OVR** Frame Rate Overflow Interrupt Enable

| Value | Description |
|---|---|
| 0 | No effect. |
| 1 | Enables the corresponding interrupt. |

**Bit 26 – CRC_ERR** Embedded Synchronization CRC Error Interrupt Enable

| Value | Description |
|---|---|
| 0 | No effect. |
| 1 | Enables the corresponding interrupt. |

**Bit 25 – C_OVR** Codec Datapath Overflow Interrupt Enable

| Value | Description |
|---|---|
| 0 | No effect. |
| 1 | Enables the corresponding interrupt. |

**Bit 24 – P_OVR** Preview Datapath Overflow Interrupt Enable

| Value | Description |
|---|---|
| 0 | No effect. |
| 1 | Enables the corresponding interrupt. |

### 38.8.19 GMAC RX Jumbo Frame Max Length Register

**Name:** GMAC_RJFML
**Offset:** 0x048
**Reset:** 0x00003FFF
**Property:** Read/Write

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | | | FML[13:8] | | | | | |
| Access | | | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | | | 1 | 1 | 1 | 1 | 1 | 1 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | FML[7:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Bits 13:0 – FML[13:0]** Frame Max Length
Rx jumbo frame maximum length.

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x016C | USBHS_DEVEPTICR3 (ISOENPT) | 7:0 | SHORTPACKETC | CRCERRIC | OVERFIC | HBISOFLUSHIC | HBISOINERRIC | UNDERFIC | RXOUTIC | TXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0170 | USBHS_DEVEPTICR4 | 7:0 | SHORTPACKETC | STALLEDIC | OVERFIC | NAKINIC | NAKOUTIC | RXSTPIC | RXOUTIC | TXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0170 | USBHS_DEVEPTICR4 (ISOENPT) | 7:0 | SHORTPACKETC | CRCERRIC | OVERFIC | HBISOFLUSHIC | HBISOINERRIC | UNDERFIC | RXOUTIC | TXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0174 | USBHS_DEVEPTICR5 | 7:0 | SHORTPACKETC | STALLEDIC | OVERFIC | NAKINIC | NAKOUTIC | RXSTPIC | RXOUTIC | TXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0174 | USBHS_DEVEPTICR5 (ISOENPT) | 7:0 | SHORTPACKETC | CRCERRIC | OVERFIC | HBISOFLUSHIC | HBISOINERRIC | UNDERFIC | RXOUTIC | TXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0178 | USBHS_DEVEPTICR6 | 7:0 | SHORTPACKETC | STALLEDIC | OVERFIC | NAKINIC | NAKOUTIC | RXSTPIC | RXOUTIC | TXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0178 | USBHS_DEVEPTICR6 (ISOENPT) | 7:0 | SHORTPACKETC | CRCERRIC | OVERFIC | HBISOFLUSHIC | HBISOINERRIC | UNDERFIC | RXOUTIC | TXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x017C | USBHS_DEVEPTICR7 | 7:0 | SHORTPACKETC | STALLEDIC | OVERFIC | NAKINIC | NAKOUTIC | RXSTPIC | RXOUTIC | TXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x017C | USBHS_DEVEPTICR7 (ISOENPT) | 7:0 | SHORTPACKETC | CRCERRIC | OVERFIC | HBISOFLUSHIC | HBISOINERRIC | UNDERFIC | RXOUTIC | TXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |

### 39.6.28 Device DMA Channel x Address Register

**Name:** USBHS_DEVDMAADDRESSx
**Offset:** 0x0304 + x*0x10 [x=0..6]
**Reset:** 0
**Property:** Read/Write

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | BUFF_ADD[31:24] | | | | | | | |
| Access | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | BUFF_ADD[23:16] | | | | | | | |
| Access | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | BUFF_ADD[15:8] | | | | | | | |
| Access | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | BUFF_ADD[7:0] | | | | | | | |
| Access | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 31:0 – BUFF_ADD[31:0]** Buffer Address
This field determines the AHB bus starting address of a DMA channel transfer.

Channel start and end addresses may be aligned on any byte boundary.

The firmware can write this field only when the USBHS_DEVDMASTATUS.CHANN_ENB bit is clear.

This field is updated at the end of the address phase of the current access to the AHB bus. It is incremented by the access byte width. The access width is 4 bytes (or less) at packet start or end, if the start or end address is not aligned on a word boundary.

The packet start address is either the channel start address or the next channel address to be accessed in the channel buffer. The packet end address is either the channel end address or the latest channel address accessed in the channel buffer.

The channel start address is written by software or loaded from the descriptor. The channel end address is either determined by the end of buffer or the USB device, or by the USB end of transfer if the USBHS_DEVDMACONTROLx.END_TR_EN bit is set.

– The SPCK pin is driven by the transmitter to synchronize the receiver.
– The NPCS0 pin becomes an input, and is used as a slave select signal (NSS)
– The NPCS1 to NPCS3 pins are not driven and can be used for other purposes.

The data transfers are identically programmable for both modes of operation. The baud rate generator is activated only in Master mode.

### 41.7.2 Data Transfer

Four combinations of polarity and phase are available for data transfers. The clock polarity is programmed with the CPOL bit in the SPI Chip Select registers (SPI_CSRx). The clock phase is programmed with the NCPHA bit. These two parameters determine the edges of the clock signal on which data is driven and sampled. Each of the two parameters has two possible states, resulting in four possible combinations that are incompatible with one another. Consequently, a master/slave pair must use the same parameter pair values to communicate. If multiple slaves are connected and require different configurations, the master must reconfigure itself each time it needs to communicate with a different slave.

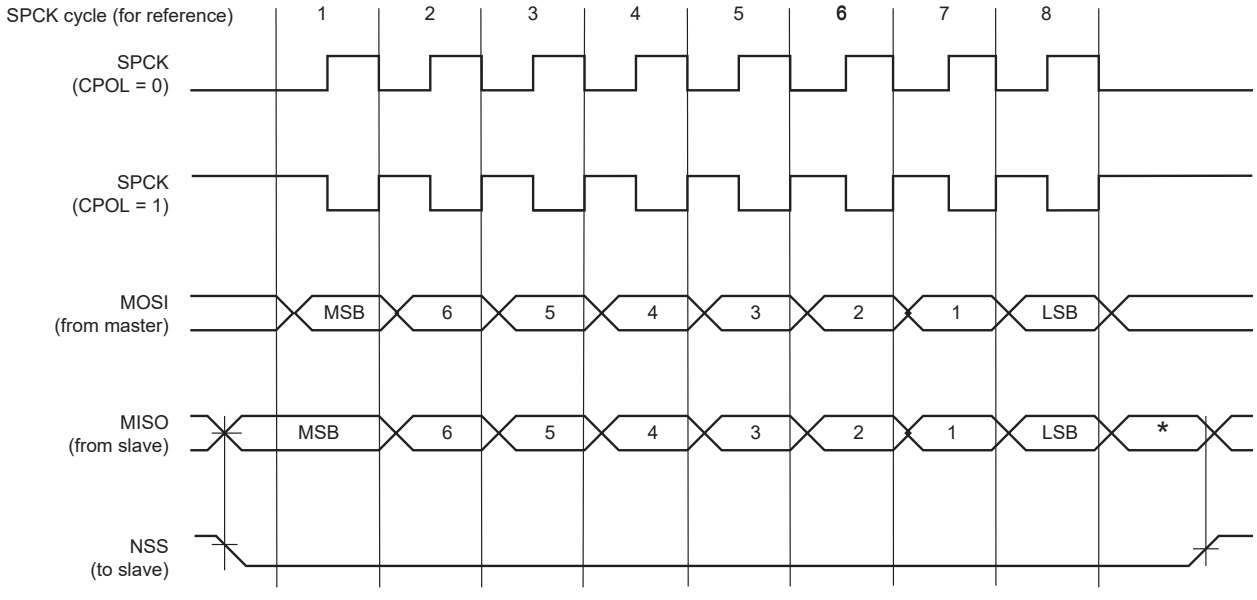
The table below shows the four modes and corresponding parameter settings.

**Table 41-2. SPI Bus Protocol Modes**

| SPI Mode | CPOL | NCPHA | Shift SPCK Edge | Capture SPCK Edge | SPCK Inactive Level |
|---|---|---|---|---|---|
| 0 | 0 | 1 | Falling | Rising | Low |
| 1 | 0 | 0 | Rising | Falling | Low |
| 2 | 1 | 1 | Rising | Falling | High |
| 3 | 1 | 0 | Falling | Rising | High |

The following figures show examples of data transfers.

**Figure 41-3. SPI Transfer Format (NCPHA = 1, 8 bits per transfer)**




* Not defined.

**Bit 9 – CP1** Compare 1

| Value | Description |
|---|---|
| 0 | A compare 1 has not occurred since the last read of the Status Register. |
| 1 | A compare 1 has occurred since the last read of the Status Register. |

**Bit 8 – CP0** Compare 0

| Value | Description |
|---|---|
| 0 | A compare 0 has not occurred since the last read of the Status Register. |
| 1 | A compare 0 has occurred since the last read of the Status Register. |

**Bit 5 – OVRUN** Receive Overrun

| Value | Description |
|---|---|
| 0 | No data has been loaded in SSC_RHR while previous data has not been read since the last read of the Status Register. |
| 1 | Data has been loaded in SSC_RHR while previous data has not yet been read since the last read of the Status Register. |

**Bit 4 – RXRDY** Receive Ready

| Value | Description |
|---|---|
| 0 | SSC_RHR is empty. |
| 1 | Data has been received and loaded in SSC_RHR. |

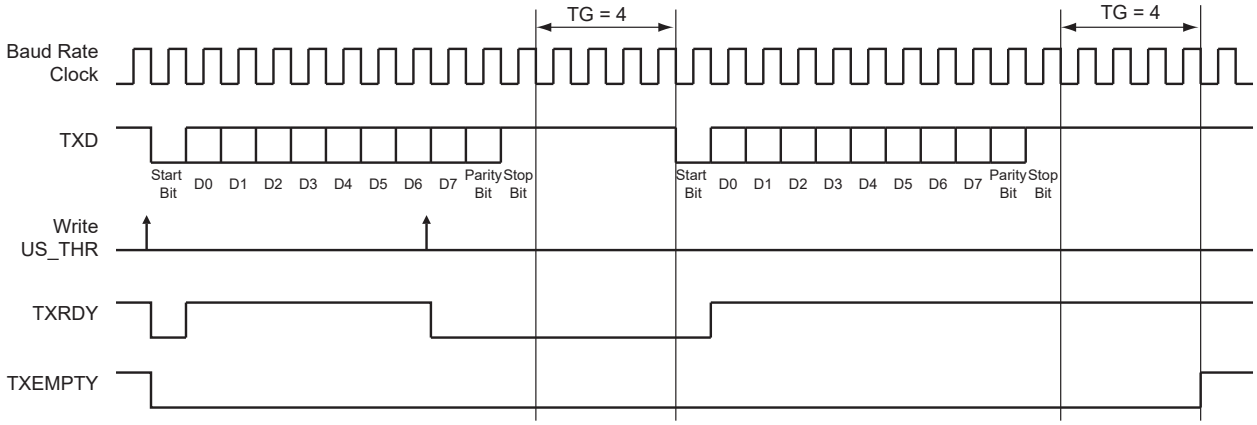
**Bit 1 – TXEMPTY** Transmit Empty

| Value | Description |
|---|---|
| 0 | Data remains in SSC_THR or is currently transmitted from TSR. |
| 1 | Last data written in SSC_THR has been loaded in TSR and last data loaded in TSR has been transmitted. |

**Bit 0 – TXRDY** Transmit Ready

| Value | Description |
|---|---|
| 0 | Data has been loaded in SSC_THR and is waiting to be loaded in the transmit shift register (TSR). |
| 1 | SSC_THR is empty. |

**Figure 46-22. Timeguard Operations**




The following table indicates the maximum length of a timeguard period that the transmitter can handle depending on the baud rate.

**Table 46-7. Maximum Timeguard Length Depending on Baud Rate**

| Baud Rate (bit/s) | Bit Time (µs) | Timeguard (ms) |
|---|---|---|
| 1,200 | 833 | 212.50 |
| 9,600 | 104 | 26.56 |
| 14,400 | 69.4 | 17.71 |
| 19,200 | 52.1 | 13.28 |
| 28,800 | 34.7 | 8.85 |
| 38,400 | 26 | 6.63 |
| 56,000 | 17.9 | 4.55 |
| 57,600 | 17.4 | 4.43 |
| 115,200 | 8.7 | 2.21 |

#### 46.6.3.11 Receiver Timeout

The Receiver Timeout provides support in handling variable-length frames. This feature detects an idle condition on the RXD line. When a timeout is detected, US_CSR.TIMEOUT rises and can generate an interrupt, thus indicating to the driver an end of frame.

The timeout delay period (during which the receiver waits for a new character) is programmed in the TO field of the Receiver Timeout register (US_RTOR). If TO is written to ‘0’, the Receiver Timeout is disabled and no timeout is detected. US_CSR.TIMEOUT remains at ‘0’. Otherwise, the receiver loads a 16-bit counter with the value programmed in US_RTOR.TO. This counter is decremented at each bit period and reloaded each time a new character is received. If the counter reaches 0, TIMEOUT rises. Then, the user can either:

- Stop the counter clock until a new character is received. This is performed by writing a ‘1’ to US_CR.STTTO. In this case, the idle state on RXD before a new character is received will not provide a timeout. This prevents having to handle an interrupt before a character is received and allows waiting for the next idle state on RXD after a frame is received.

**Bit 9 – TXEMPTY** TXEMPTY Interrupt Enable

**Bit 8 – TIMEOUT** Timeout Interrupt Enable

**Bit 7 – PARE** Parity Error Interrupt Enable

**Bit 6 – FRAME** Framing Error Interrupt Enable

**Bit 5 – OVRE** Overrun Error Interrupt Enable

**Bit 2 – RXBRK** Receiver Break Interrupt Enable

**Bit 1 – TXRDY** TXRDY Interrupt Enable

**Bit 0 – RXRDY** RXRDY Interrupt Enable

### 49.6.35 MCAN Tx Buffer Configuration

**Name:** MCAN_TXBC
**Offset:** 0xC0
**Reset:** 0x00000000
**Property:** Read/Write

This register can only be written if the bits CCE and INIT are set in MCAN CC Control Register.

The sum of TFQS and NDTB may not exceed 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers.

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | TFQM | TFQS[5:0] | | | | | |
| Access | | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | NDTB[5:0] | | | | | |
| Access | | | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | | | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | TBSA[13:6] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TBSA[5:0] | | | | | | | |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | | |

**Bit 30 – TFQM** Tx FIFO/Queue Mode

| Value | Description |
|---|---|
| 0 | Tx FIFO operation. |
| 1 | Tx Queue operation. |

**Bits 29:24 – TFQS[5:0]** Transmit FIFO/Queue Size

| Value | Description |
|---|---|
| 0 | No Tx FIFO/Queue. |
| 1-32 | Number of Tx Buffers used for Tx FIFO/Queue. |
| >32 | Values greater than 32 are interpreted as 32. |

**Bits 21:16 – NDTB[5:0]** Number of Dedicated Transmit Buffers

| Value | Description |
|---|---|
| 0 | No dedicated Tx Buffers. |
| 1-32 | Number of dedicated Tx Buffers. |
| >32 | Values greater than 32 are interpreted as 32. |

| Value | Description |
|---|---|
| 0 | No effect. |
| 1 | Enables the interrupt when a rising edge occurs on IDX input. |

### 51.7.50 PWM Leading-Edge Blanking Register

**Name:** PWM_LEBRx
**Offset:** 0x0430 + x*0x20 [x=0..1]
**Reset:** 0x00000000
**Property:** Read/Write

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | | | PWMHREN | PWMHFEN | PWMLREN | PWMLFEN |
| Access | | | | | R/W | R/W | R/W | R/W |
| Reset | | | | | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | LEBDELAY[6:0] | | | | | | |
| Access | | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bit 19 – PWMHREN** PWMH Rising Edge Enable
Leading-edge blanking is enabled on PWMHx output rising edge.

| Value | Description |
|---|---|
| 0 | Leading-edge blanking is disabled on PWMHx output rising edge. |
| 1 | Leading-edge blanking is enabled on PWMHx output rising edge. |

**Bit 18 – PWMHFEN** PWMH Falling Edge Enable

| Value | Description |
|---|---|
| 0 | Leading-edge blanking is disabled on PWMHx output falling edge. |
| 1 | Leading-edge blanking is enabled on PWMHx output falling edge. |

**Bit 17 – PWMLREN** PWML Rising Edge Enable

| Value | Description |
|---|---|
| 0 | Leading-edge blanking is disabled on PWMLx output rising edge. |
| 1 | Leading-edge blanking is enabled on PWMLx output rising edge. |

**Bit 16 – PWMLFEN** PWML Falling Edge Enable

#### 53.6.4.4 Bypass Mode

Bypass mode disables the DAC output buffer and thus minimizes power consumption. This mode can be used to generate slow varying signals. Refer to the DAC Characteristics in the section “Electrical Characteristics” of this datasheet.

To enter this mode, Free-running mode must be selected and the DACC_ACR.IBCTLCHx field configured in Bypass mode.

**Related Links**

58. Electrical Characteristics for SAM V70/V71

#### 53.6.4.5 Interpolation Mode

The DACC integrates interpolation filters that allow OSR of 2×, 4×, 8×, 16× or 32×. This mode can be used only if Trigger mode is enabled and value in the field OSRx is not ‘0’. The OSR of the interpolator is configured in the OSRx field in the DACC Trigger Register (DACC_TRIGR).

The data is sampled once every OSR trigger event and then recomputed at the trigger sample rate using a third-order SINC filter. This reduces the number of accesses to the DACC and increases the signal-to-noise ratio (SNR) of the converted output signal.

The figures below show the spectral mask of the SINC filter depending on the selected OSR. $f_s$ is the sampling frequency of the input signal which corresponds to the trigger frequency divided by OSR.

**Figure 53-5. Interpolator Spectral Mask for OSR = 2**

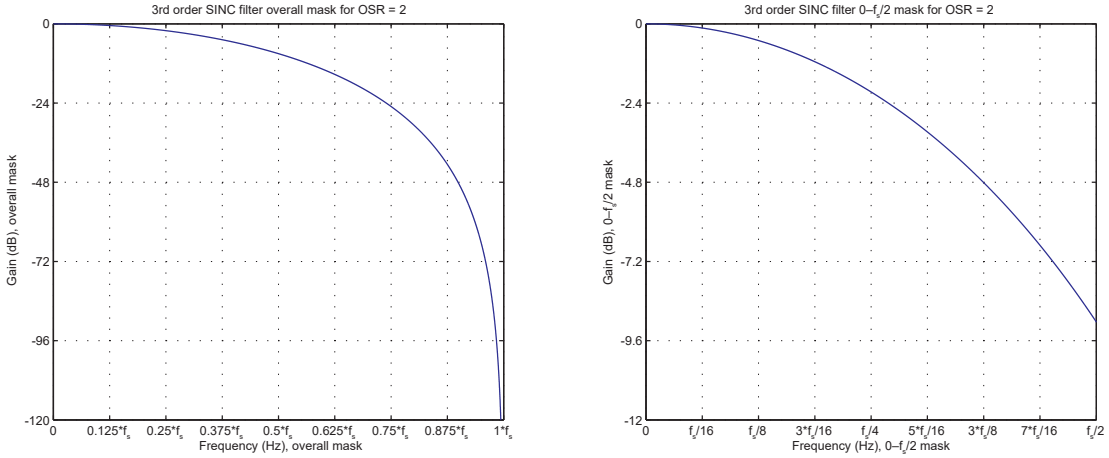



**Figure 53-6. Interpolator Spectral Mask for OSR = 4**