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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70n19a-an

3. Write 0x1 into the Trace Enable register:
   – Enable the Stimulus port 0.
4. Write 0x1 into the Trace Privilege register:
   – Stimulus port 0 only accessed in privileged mode (Clearing a bit in this register will result in the corresponding stimulus port being accessible in user mode.)
5. Write into the Stimulus port 0 register: TPIU (Trace Port Interface Unit)
   The TPIU acts as a bridge between the on-chip trace data and the Instruction Trace Macrocell (ITM).

   The TPIU formats and transmits trace data off-chip at frequencies asynchronous to the core.

16.7.7.2 Asynchronous Mode

The TPIU is configured in asynchronous mode, trace data are output using the single TRACESWO pin. The TRACESWO signal is multiplexed with the TDO signal. As a consequence, asynchronous trace mode is only available when the Serial Wire Debug mode is selected.

Two encoding formats are available for the single pin output:

- Manchester encoded stream. This is the reset value.
- NRZ_based UART byte structure

16.7.7.3 How to Configure the TPIU

This example only concerns the asynchronous trace mode.

Set the TRCENA bit to 1 into the Debug Exception and Monitor Register (0xE000EDFC) to enable the use of trace and debug blocks.

1. Write 0x2 into the Selected Pin Protocol Register.
   – Select the Serial Wire output – NRZ
2. Write 0x100 into the Formatter and Flush Control Register.
3. Set the suitable clock prescaler value into the Async Clock Prescaler Register to scale the baud rate of the asynchronous output (this can be done automatically by the debugging tool).

16.7.8 IEEE1149.1 JTAG Boundary Scan

IEEE1149.1 JTAG Boundary Scan allows pin-level access independent of the device packaging technology.

IEEE1149.1 JTAG Boundary Scan is enabled when TST is tied to high, PD0 tied to low, and JTAGSEL tied to high during powerup. These pins must be maintained in their respective states for the duration of the boundary scan operation. The SAMPLE, EXTEST and BYPASS functions are implemented. In Serial Wire Debug mode, the ARM processor responds with a non-JTAG chip ID that identifies the processor. This is not IEEE1149.1 JTAG-compliant.

It is not possible to switch directly between JTAG Boundary Scan and SWJ Debug Port operations. A chip reset must be performed after JTAGSEL is changed.

A Boundary Scan Descriptor Language (BSDL) file to set up the test is provided on www.microchip.com.

16.7.8.1 JTAG Boundary Scan Register

The Boundary Scan Register (BSR) contains a number of bits which correspond to active pins and associated control signals.

Each input/output pin corresponds to a 3-bit register in the BSR. The OUTPUT bit contains data that can be forced on the pad. The INPUT bit facilitates the observability of data applied to the pad. The CONTROL bit selects the direction of the pad.

Table 17-2. Commands Available through the SAM-BA Boot

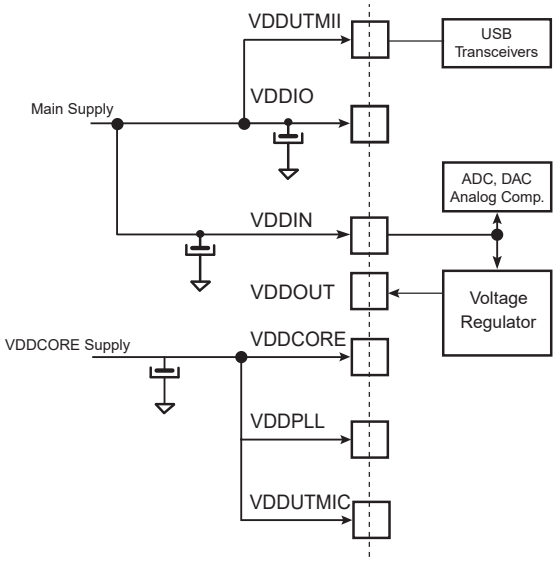
Command	Action	Arguments	Example
N	Set Normal mode	No argument	N#
T	Set Terminal mode	No argument	T#
O	Write a byte	Address, Value#	O200001,CA#
o	Read a byte	Address,#	o200001,#
H	Write a half word	Address, Value#	H200002,CAFE#
h	Read a half word	Address,#	h200002,#
W	Write a word	Address, Value#	W200000,CAFEDECA#
w	Read a word	Address,#	w200000,#
S	Send a file	Address,#	S200000,#
R	Receive a file	Address, NbOfBytes#	R200000,1234#
G	Go	Address#	G200200#
V	Display version	No argument	V#

- Mode commands:
  - Normal mode configures SAM-BA Monitor to send/receive data in binary format
  - Terminal mode configures SAM-BA Monitor to send/receive data in ASCII format
- Write commands: Write a byte (O), a halfword (H) or a word (W) to the target
  - Address: Address in hexadecimal
  - Value: Byte, halfword or word to write in hexadecimal
- Read commands: Read a byte (o), a halfword (h) or a word (w) from the target
  - Address: Address in hexadecimal
  - Output: The byte, halfword or word read in hexadecimal
- Send a file (S): Send a file to a specified address
  - Address: Address in hexadecimal
    Note: There is a timeout on this command which is reached when the prompt '>' appears before the end of the command execution.
- Receive a file (R): Receive data into a file from a specified address
  - Address: Address in hexadecimal
  - NbOfBytes: Number of bytes in hexadecimal to receive
- Go (G): Jump to a specified address and execute the code
  - Address: Address to jump in hexadecimal
- Get Version (V): Return the SAM-BA boot version
  Note: In Terminal mode, when the requested command is performed, SAM-BA Monitor adds the following prompt sequence to its answer: <LF>+<CR>+'>'.

17.6.1 UART0 Serial Port

Communication is performed through the UART0 initialized to 115200 Baud, 8, n, 1.

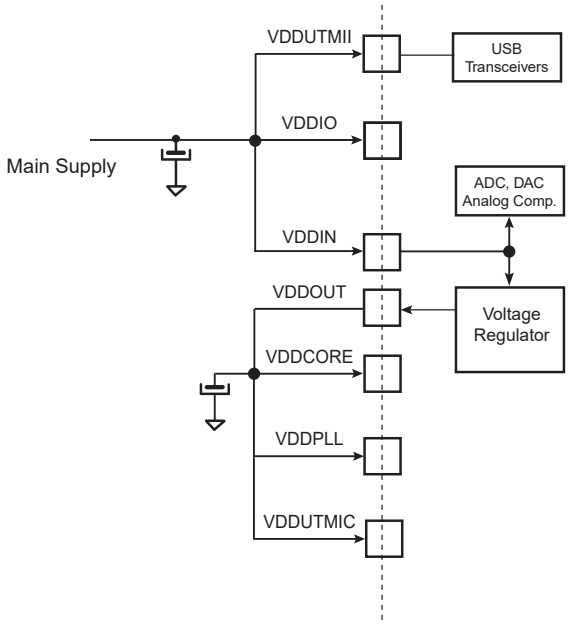
Figure 23-2. Separate Backup Supply Powering Scheme



Note: Restrictions
With main supply < 3.0V, USB is not usable.
With main supply < 2.7V, MediaLB is not usable.
With main supply < 2.0V, ADC, DAC and Analog comparator are not usable.
With main supply and VDDIN > 3V, all peripherals are usable.

When no separate backup supply for VDDIO is used, since the external voltage applied on VDDIO is kept, all of the I/O configurations (i.e., WKUP pin configuration) are maintained in Backup mode. When not using backup batteries, VDDIORDY is set so the user does not need to program it.

Figure 23-3. No Separate Backup Supply Powering Scheme



Note: Restrictions
with main supply < 2.0 V, USB and ADC/DAC and analog comparator are not usable.
With main supply > 2.0V and < 3V, USB is not usable.

25.5.3 Reinforced Safety Watchdog Timer Status Register

Name: RSWDT_SR
Offset: 0x08
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

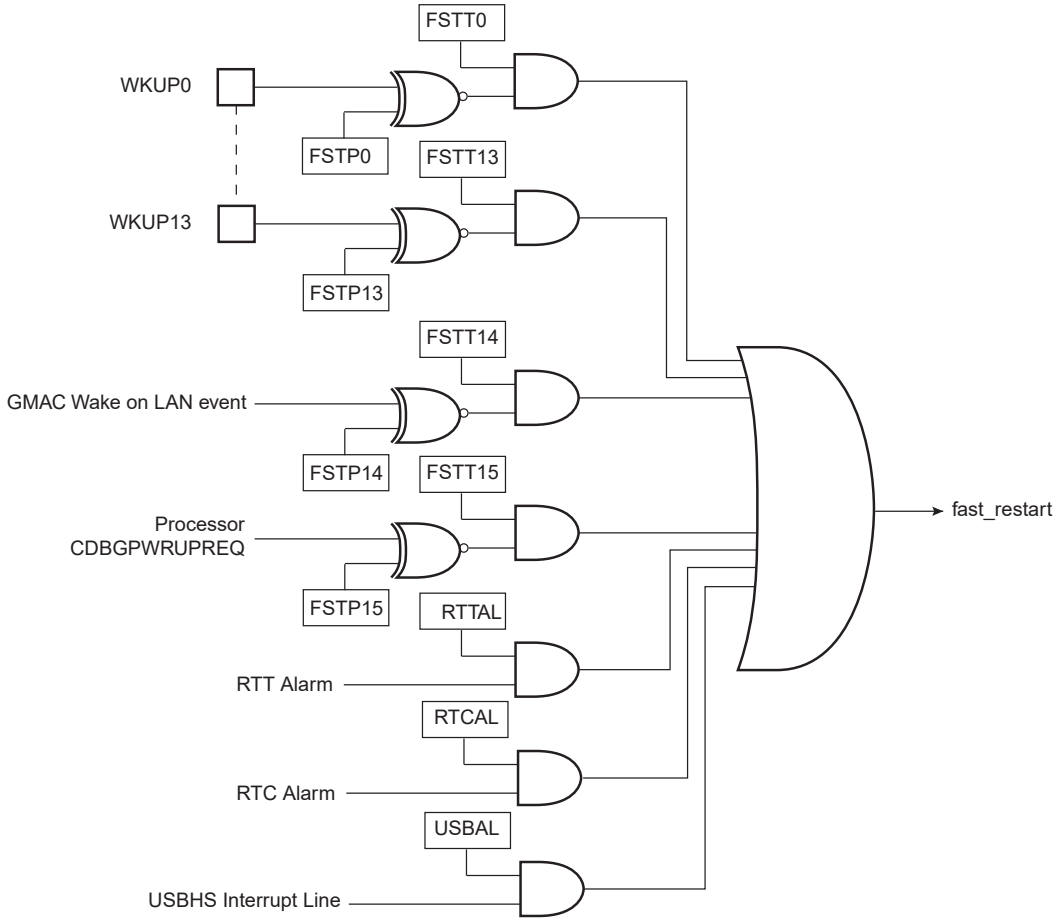
Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								WDUNF
Access								
Reset								0

Bit 0 – WDUNF Watchdog Underflow

Value	Description
0	No watchdog underflow occurred since the last read of RSWDT_SR.
1	At least one watchdog underflow occurred since the last read of RSWDT_SR.

Figure 31-4. Fast Startup Circuitry



Each wakeup input pin and alarm can be enabled to generate a fast startup event by setting the corresponding bit in PMC_FSMR.

The user interface does not provide any status for fast startup. The status can be read in the PIO Controller and the status registers of the RTC, RTTand USB Controller.

Related Links

7. Power Considerations

31.14 Startup from Embedded Flash

The inherent startup time of the embedded Flash cannot provide a fast startup of the system.

If system fast startup time is not required, the first instruction after a Wait mode exit can be located in the embedded Flash. Under these conditions, prior to entering Wait mode, the Flash controller must be programmed to perform access in 0 wait-state (refer to the embedded Flash controller section).

The procedure and conditions to enter Wait mode and the circuitry to exit Wait mode are strictly the same as fast startup (see "Fast Startup").

Related Links

22. Enhanced Embedded Flash Controller (EEFC)

38.8.63 GMAC Pause Frames Received Register

Name: GMAC_PFR
Offset: 0x164
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PFRX[15:0] Pause Frames Received Register
This register counts the number of pause frames received without error.

39. USB High-Speed Interface (USBHS)

39.1 Description

The USB High-Speed Interface (USBHS) complies with the Universal Serial Bus (USB) 2.0 specification in all speeds.

Each pipe/endpoint can be configured in one of several USB transfer types. It can be associated with one, two or three banks of a DPRAM used to store the current data payload. If two or three banks are used, then one DPRAM bank is read or written by the CPU or the DMA, while the other is read or written by the USBHS core. This feature is mandatory for isochronous pipes/endpoints.

The following table describes the hardware configuration of the USB MCU device.

Table 39-1. Description of USB Pipes/Endpoints

Pipe/ Endpoint	Mnemonic	Max. Number Banks	DMA	High Band Width	Max. Pipe/ Endpoint Size	Type
0	PEP_0	1	N	N	64	Control
1	PEP_1	3	Y	Y	1024	Isochronous/Bulk/ Interrupt/Control
2	PEP_2	3	Y	Y	1024	Isochronous/Bulk/ Interrupt/Control
3	PEP_3	2	Y	Y	1024	Isochronous/Bulk/ Interrupt/Control
4	PEP_4	2	Y	Y	1024	Isochronous/Bulk/ Interrupt/Control
5	PEP_5	2	Y	Y	1024	Isochronous/Bulk/ Interrupt/Control
6	PEP_6	2	Y	Y	1024	Isochronous/Bulk/ Interrupt/Control
7	PEP_7	2	Y	Y	1024	Isochronous/Bulk/ Interrupt/Control
8	PEP_8	2	N	Y	1024	Isochronous/Bulk/ Interrupt/Control
9	PEP_9	2	N	Y	1024	Isochronous/Bulk/ Interrupt/Control

39.2 Embedded Characteristics

- Compatible with the USB 2.0 Specification
- Supports High-Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed (1.5 Mbps) Communication

Bit 6 – STALLEDEC STALLed Interrupt Clear

Bit 5 – OVERFEC Overflow Interrupt Clear

Bit 4 – NAKINEC NAKed IN Interrupt Clear

Bit 3 – NAKOUTEC NAKed OUT Interrupt Clear

Bit 2 – RXSTPEC Received SETUP Interrupt Clear

Bit 1 – RXOUTEC Received OUT Data Interrupt Clear

Bit 0 – TXINEC Transmitted IN Interrupt Clear

40.14.15 HSMCI Interrupt Mask Register

Name: HSMCI_IMR
Offset: 0x4C
Reset: 0x0
Property: Read-only

The following configuration values are valid for all listed bit names of this register:

0: The corresponding interrupt is not enabled.

1: The corresponding interrupt is enabled.

Bit	31	30	29	28	27	26	25	24
	UNRE	OVRE	ACKRCVE	ACKRCV	XFRDONE	FIFOEMPTY		BLKOVRE
Access								
Reset	0	0	0	0	0	0		0

Bit	23	22	21	20	19	18	17	16
	CSTOE	DTOE	DCRCE	RTOE	RENDE	RCRCE	RDIRE	RINDE
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
			CSRCV	SDIOWAIT				SDIOIRQA
Access								
Reset			0	0				0

Bit	7	6	5	4	3	2	1	0
			NOTBUSY	DTIP	BLKE	TXRDY	RXRDY	CMDRDY
Access								
Reset			0	0	0	0	0	0

Bit 31 – UNRE Underrun Interrupt Mask

Bit 30 – OVRE Overrun Interrupt Mask

Bit 29 – ACKRCVE Boot Operation Acknowledge Error Interrupt Mask

Bit 28 – ACKRCV Boot Operation Acknowledge Received Interrupt Mask

Bit 27 – XFRDONE Transfer Done Interrupt Mask

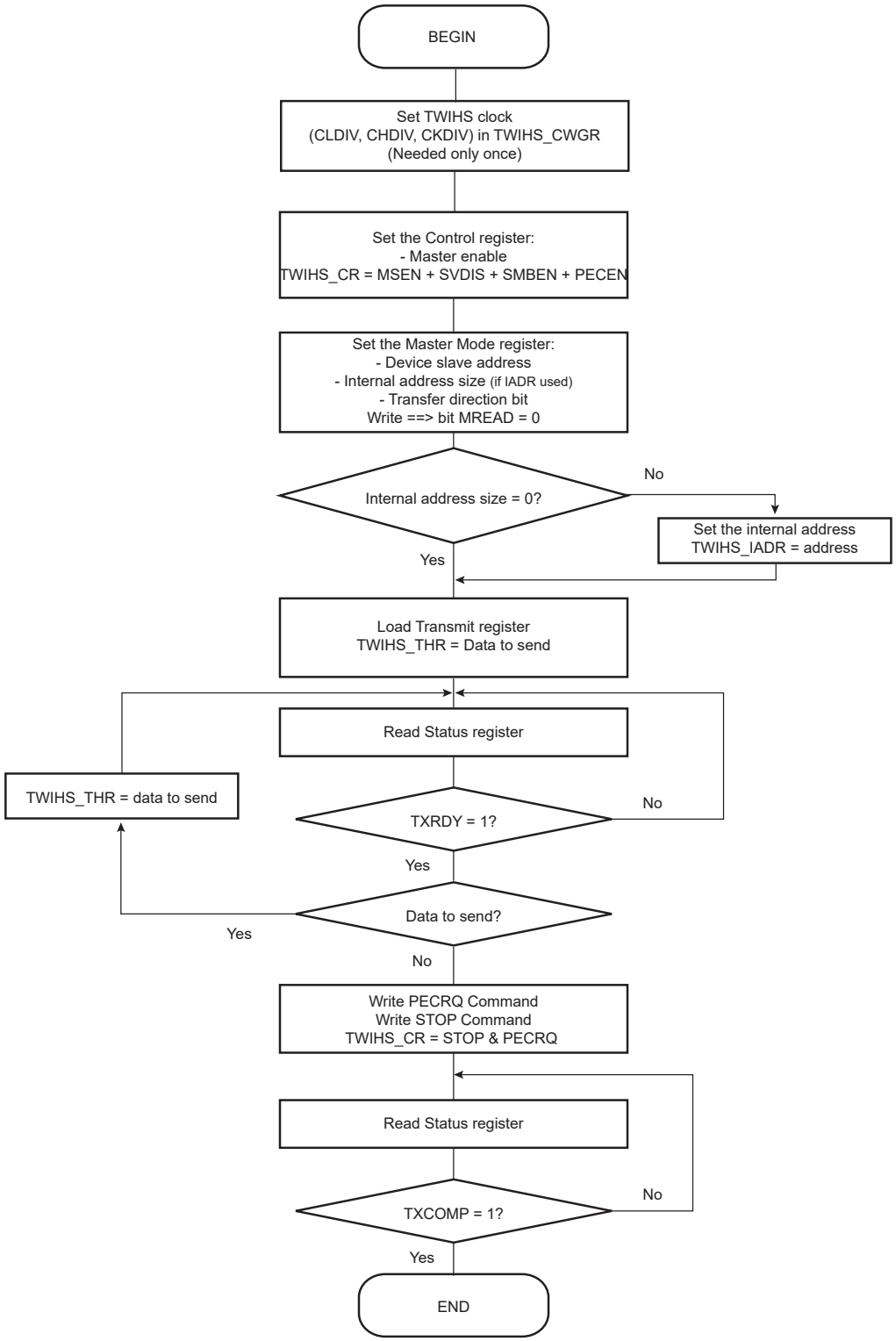
Bit 26 – FIFOEMPTY FIFO Empty Interrupt Mask

Bit 24 – BLKOVRE DMA Block Overrun Error Interrupt Mask

Bit 23 – CSTOE Completion Signal Time-out Error Interrupt Mask

Bit 22 – DTOE Data Time-out Error Interrupt Mask

Figure 43-17. SMBus Write Operation with Multiple Data Bytes with or without Internal Address and PEC Sending



46.7.18 USART Channel Status Register (SPI_MODE)

Name: US_CSR (SPI_MODE)
Offset: 0x0014
Reset: 0x0
Property: Read-only

This configuration is relevant only if USART_MODE = 0xE or 0xF in the USART Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	NSS				NSSE			
Access								
Reset	0				0			

Bit	15	14	13	12	11	10	9	8
						UNRE	TXEMPTY	
Access								
Reset						0	0	

Bit	7	6	5	4	3	2	1	0
			OVRE				TXRDY	RXRDY
Access								
Reset			0				0	0

Bit 23 – NSS Image of NSS Line

Value	Description
0	NSS line is driven low (if NSSE = 1, falling edge occurred on NSS line).
1	NSS line is driven high (if NSSE = 1, rising edge occurred on NSS line).

Bit 19 – NSSE NSS Line (Driving CTS Pin) Rising or Falling Edge Event (cleared on read)

Value	Description
0	No NSS line event has been detected since the last read of US_CSR.
1	A rising or falling edge event has been detected on NSS line since the last read of US_CSR.

Bit 10 – UNRE Underrun Error (cleared by writing a one to bit US_CR.RSTSTA)

Value	Description
0	No SPI underrun error has occurred since the last RSTSTA.
1	At least one SPI underrun error has occurred since the last RSTSTA.

Bit 9 – TXEMPTY Transmitter Empty (cleared by writing US_THR)

46.7.24 USART Receiver Timeout Register

Name: US_RTOR
Offset: 0x0024
Reset: 0x0
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
								TO[16:16]
Access								R/W
Reset								0

Bit	15	14	13	12	11	10	9	8
	TO[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TO[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 16:0 – TO[16:0] Timeout Value

Value	Description
0	The receiver timeout is disabled.
1-65535	The receiver timeout is enabled and TO is Timeout Delay / Bit Period.
1-131071	The receiver timeout is enabled and TO is Timeout Delay / Bit Period.

Value	Description
0	Setting the bit LINWKUP in US_CR sends a LIN 2.0 wakeup signal.
1	Setting the bit LINWKUP in US_CR sends a LIN 1.3 wakeup signal.

Bit 6 – FSDIS Frame Slot Mode Disable

Value	Description
0	The Frame Slot mode is enabled.
1	The Frame Slot mode is disabled.

Bit 5 – DLM Data Length Mode

Value	Description
0	The response data length is defined by field DLC of this register.
1	The response data length is defined by bits 5 and 6 of the identifier (IDCHR in US_LINIR).

Bit 4 – CHKTYP Checksum Type

Value	Description
0	LIN 2.0 “enhanced” checksum
1	LIN 1.3 “classic” checksum

Bit 3 – CHKDIS Checksum Disable

Value	Description
0	In master node configuration, the checksum is computed and sent automatically. In slave node configuration, the checksum is checked automatically.
1	Whatever the node configuration is, the checksum is not computed/sent and it is not checked.

Bit 2 – PARDIS Parity Disable

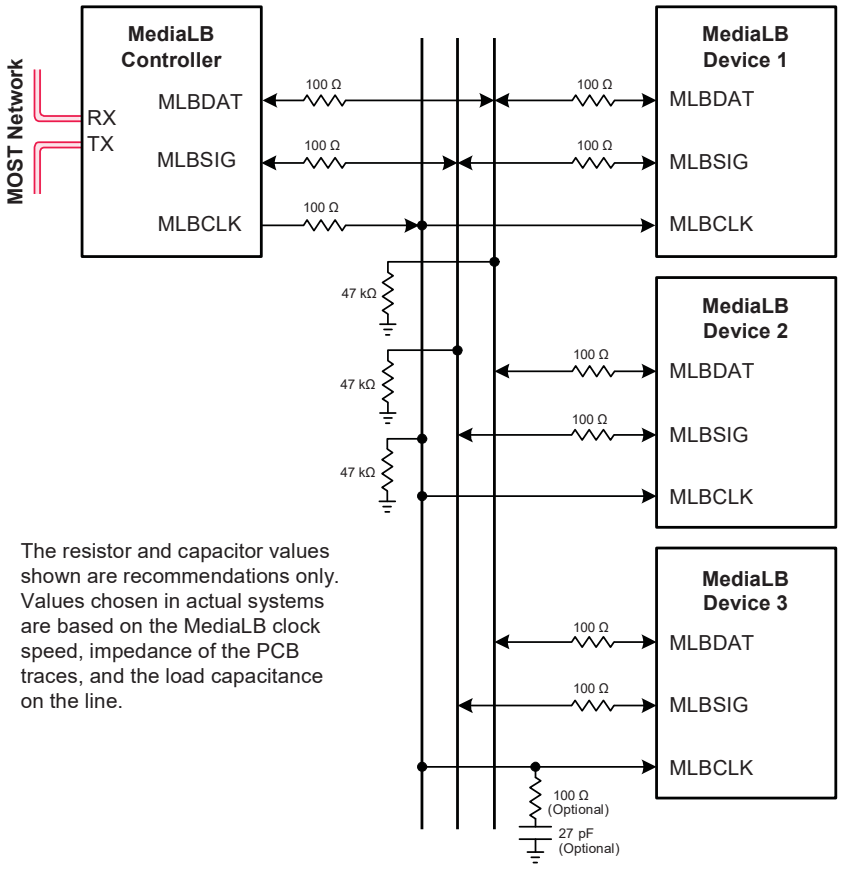
Value	Description
0	In master node configuration, the identifier parity is computed and sent automatically. In master node and slave node configuration, the parity is checked automatically.
1	Whatever the node configuration is, the Identifier parity is not computed/sent and it is not checked.

Bits 1:0 – NACT[1:0] LIN Node Action
Values which are not listed in the table must be considered as “reserved”.

Value	Name	Description
00	PUBLISH	The USART transmits the response.
01	SUBSCRIBE	The USART receives the response.
10	IGNORE	The USART does not transmit and does not receive the response.

optionally have AC-parallel termination near the farthest Device from the Controller to ensure a clean clock by minimizing reflections.

Figure 48-2. 3-pin MediaLB Connection Diagram



48.6 Functional Description

48.6.1 Link Layer

The MediaLB link layer uses the concept of ChannelAddress, Command, RxStatus, and Data to transport all MOST Network data types and manage MediaLB.

These terms are defined as follows:

- ChannelAddress:

A 16-bit token, which is sent on the MLBS line by the MediaLB Controller at the end of a physical channel. A unique ChannelAddress defines a logical channel and grants a particular physical channel to a transmitting (Tx) and a receiving (Rx) MediaLB Device.

- Command:

A byte-wide value sent by the transmitting (Tx) MediaLB Device on the MLBS line at the start of a physical channel. This command byte indicates the data type and additional control information to the Rx MediaLB Device. The Tx Device also outputs data on the MLBD signal during the same physical channel that Command is sent.

- RxStatus:

50.6 Functional Description

50.6.1 Description

All channels of the Timer Counter are independent and identical in operation except when the QDEC is enabled. The registers for channel programming are listed in 50.7 Register Summary.

50.6.2 16-bit Counter

Each 16-bit channel is organized around a 16-bit counter. The value of the counter is incremented at each positive edge of the selected clock. When the counter has reached the value 2^{16}-1 and passes to zero, an overflow occurs and the COVFS bit in the Interrupt Status register (TC_SR) is set.

The current value of the counter is accessible in real time by reading the Counter Value register (TC_CV). The counter can be reset by a trigger. In this case, the counter value passes to zero on the next valid edge of the selected clock.

50.6.3 Clock Selection

At block level, input clock signals of each channel can be connected either to the external inputs TCLKx, or to the internal I/O signals TIOAx for chaining(1) by programming the Block Mode register (TC_BMR). See Clock Chaining Selection.

Each channel can independently select an internal or external clock source for its counter(2):

- External clock signals: XC0, XC1 or XC2
- Internal clock signals: PCK6 or PCK7 (TC0 only), MCK/8, MCK/32, MCK/128, SLCK

This selection is made by the TCCLKS bits in the Channel Mode register (TC_CMRx).

The selected clock can be inverted with TC_CMRx.CLKI. This allows counting on the opposite edges of the clock.

The burst function allows the clock to be validated when an external signal is high. The BURST parameter in the TC_CMRx defines this signal (none, XC0, XC1, XC2). See Clock Selection.

Note:

1. In Waveform mode, to chain two timers, it is mandatory to initialize some parameters:
   – Configure TIOx outputs to 1 or 0 by writing the required value to TC_CMRx.ASWTRG.
   – Bit TC_BCR.SYNC must be written to 1 to start the channels at the same time.
2. In all cases, if an external clock or asynchronous internal clock PCK6 or PCK7 (TC0 only) is used, the duration of each of its levels must be longer than the peripheral clock period, so the clock frequency will be at least 2.5 times lower than the peripheral clock.

54.7.3 ACC Interrupt Enable Register

Name: ACC_IER
Offset: 0x24
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								CE
Access								W
Reset								–

Bit 0 – CE Comparison Edge

Value	Description
0	No effect.
1	Enables the interrupt when the selected edge (defined by EDGETYP) occurs.

54.7.7 ACC Analog Control Register

Name: ACC_ACR
Offset: 0x94
Reset: 0
Property: Read/Write

This register can only be written if the WPEN bit is cleared in ACC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						HYST[1:0]		ISEL
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:1 – HYST[1:0] Hysteresis Selection
Refer to the ACC characteristics in the section “Electrical Characteristics”.

Value	Name	Description
0	NONE	No hysteresis
1	MEDIUM	Medium hysteresis
2	MEDIUM	Medium hysteresis
3	HIGH	High hysteresis

Bit 0 – ISEL Current Selection
Refer to the ACC characteristics in the section “Electrical Characteristics”.

0 (LOPW): Low-power option.

1 (HISP): High-speed option.

Related Links

58. Electrical Characteristics for SAM V70/V71

Symbol	Parameter	Digital Code	Min	Typ	Max	Unit
		1110	–	3.28	–	
		1111	–	3.4	–	

Figure 59-3. VDDIO Supply Monitor

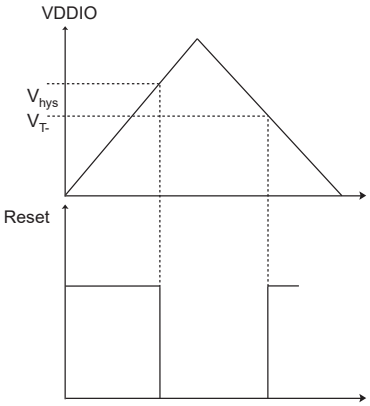
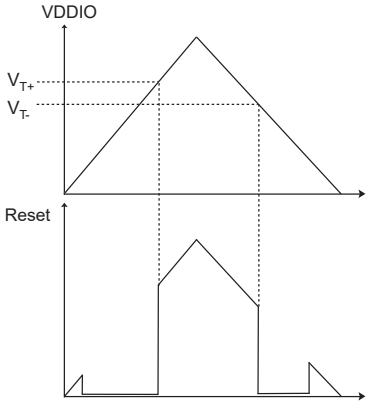


Table 59-10. VDDIO Power-On Reset Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{T+}	Threshold Voltage Rising	–	1.45	1.53	1.61	V
V_{T-}	Threshold Voltage Falling	–	1.37	1.46	–	V
V_{hys}	Hysteresis	–	40	80	130	mV
t_{RES}	Reset Time-out Period	–	240	320	800	µs

Figure 59-4. VDDIO Power-On Reset Characteristics



59.3 Power Consumption

- Power consumption of the device depending on the different Low-Power modes (Backup, Wait, Sleep) and Active mode
- Power consumption on power supply in different modes: Backup, Wait, Sleep and Active
- Power consumption by peripheral:

Note: Restrictions
With main supply < 2.5V, USB and DACC are not usable.
With main supply > 2.5V and < 3V, USB is not usable.
With main supply > 3.0 V, all peripherals are usable.

Check	Signal Name	Recommended Pin Connection	Description
	VDDIN	Decoupling/filtering capacitors (100 nF and 4.7 µF)(1)(2)	Powers the voltage regulator, AFE, DAC, and Analog comparator power supply Supply ripple must not exceed 20 mVrms for 10 kHz to 20 MHz range. **WARNING** VDDIN and VDDIO must have the same level and must be higher than VDDCORE. **WARNING** Powerup and powerdown sequences given in the "Power Considerations" chapter must be respected.
	VDDIO	Decoupling/filtering capacitors (100 nF)(1)(2)	Powers the Peripheral I/O lines (Input/Output Buffers), backup part, 1 Kbyte of Backup SRAM, 32 kHz crystal oscillator, oscillator pads Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop. Supply ripple must not exceed 30 mVrms for 10 kHz to 10 MHz range. **WARNING** VDDIN and VDDIO must have the same level and must be higher than VDDCORE. **WARNING** Powerup and powerdown sequences given in the "Power Considerations" chapter must be respected.
	VDDUTMII	Decoupling capacitor (100 nF)(1)(2)	Powers the USB transceiver interface. Must be connected to VDDIO. For USB operations, VDDUTMII and VDDIO voltage ranges must be from 3.0V to 3.6V. Must always be connected even when the USB is not used.

Date	Comments
	Table 50.6.3 “Clock Selection”: updated notes (1) and (2). Updated Section 50.6.16.4 “Position and Rotation Measurement”. Added Section 50.6.17 “Detecting a Missing Index Pulse”.
cont’d	
01-June-16	Section 52. “Analog Front-End Controller (AFEC)” Section 52.2 “Embedded Characteristics”: deleted bullet on conversion rate (redundant with Electrical Characteristics) Section 52.6.1 “Analog Front-End Conversion”: updated and changed clock frequency range. Updated formula to calculate AFE conversion time. Section 52.6.3 “Conversion Resolution”: added Note. Section 52.6.6 “Conversion Triggers”: added detail on effects of delay variation. Section 52.6.11 “Input Gain and Offset”: updated information on AOFF field. Section 52.6.12 “AFE Timings”: updated Warning and deleted paragraph on settling time. Section 52.6.15 “Automatic Error Correction”: - modified the description of Gs and value (now 15, was 11). - modified the formula given to obtain the final conversion result after error correction. - added details on OFFSETCORR and GAINCORR fields. - deleted definitions of unused terms ‘ConvValue’ and ‘Resolution’ - added Figure 7-14 “AFE Digital Signal Processing”. Section 52.7.2 “AFEC Mode Register”: updated descriptions of fieldsTRACKTIM and TRANSFER. Section 52.7.18 “AFEC Channel Selection Register”: updated CSEL bit description. Section 52.7.20 “AFEC Channel Offset Compensation Register”: added note on configuration of AOFF.
	Section 58. “Electrical Characteristics” Added Table 58-2 “Recommended Thermal Operating Conditions”. Updated Table 58-3 “DC Characteristics”. Updated Table 58-31 “AFE Timing Characteristics”. Modified AFEC_ACR.IBCTL value in Note (1) of Table 58-31 “AFE Timing Characteristics” and in Section 58.8.1.2 “ADC Bias Current”. Table 58-38 “Number of Tau:n”: deleted bullets on calculated tracking time. Updated Table 58-41 “Temperature Sensor Characteristics”. Table 58-52 “I/O Characteristics”: updated VDDIO for FreqMax1. Section 58.13.1.5 “QSPI Characteristics”: updated comments in “Master Read Mode”