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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70n19a-ant

LQFP Pin	LFBGA/ TFBGA Ball	UFBGA Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		PIO Peripheral D		Reset State
					Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
129	A6	A7	VDDIO	GPIO	PA29	I/O	–	–	RI1	I	TCLK2	I	–	–	–	–	PIO, I, PU, ST
116	A10	A11	VDDIO	GPIO	PA30	I/O	WKUP11 (1)	I	PWMC0_ PWML2	O	PWMC1_ PWMEX TRG0	I	MCDA0	I/O	I2SC0_D O	O	PIO, I, PU, ST
118	C8	C10	VDDIO	GPIO_A D	PA31	I/O	–	–	SPI0_NP CS1	I/O	PCK2	O	MCDA1	I/O	PWMC1_ PWMH2	O	PIO, I, PU, ST
21	H4	H2	VDDIO	GPIO	PB0	I/O	AFE0_A D10/ RTCOUT 0(7)	I	PWMC0_ PWMH0	O	–	–	RXD0	I	TF	I/O	PIO, I, PU, ST
20	G3	H1	VDDIO	GPIO	PB1	I/O	AFE1_A D0/ RTCOUT 1(7)	I	PWMC0_ PWMH1	O	GTSUCO MP	O	TXD0	I/O	TK	I/O	PIO, I, PU, ST
26	J2	K1	VDDIO	GPIO	PB2	I/O	AFE0_A D5(5)	I	CANTX0	O	–	–	CTS0	I	SPI0_NP CS0	I/O	PIO, I, PU, ST
31	J3	L1	VDDIO	GPIO_A D	PB3	I/O	AFE0_A D2/ WKUP12 (6)	I	CANRX0	I	PCK2	O	RTS0	O	ISI_D2	I	PIO, I, PU, ST
105	A12	C13	VDDIO	GPIO_M L B	PB4	I/O	TDI(9)	I	TWD1	I/O	PWMC0_ PWMH2	O	MLBCLK	I	TXD1	I/O	PIO, I, PU, ST
109	C10	C12	VDDIO	GPIO_M L B	PB5	I/O	TDO/TR A CESWO/ WKUP13 (9)	O	TWCK1	O	PWMC0_ PWML0	O	MLBDAT	I/O	TD	O	O, PU
79	J11	K11	VDDIO	GPIO	PB6	I/O	SWDIO/T MS(9)	I	–	–	–	–	–	–	–	–	PIO,I,ST
89	F9	H13	VDDIO	GPIO	PB7	I/O	SWCLK/ TCK(9)	I	–	–	–	–	–	–	–	–	PIO,I,ST
141	A3	B2	VDDIO	CLOCK	PB8	I/O	XOUT(10)	O	–	–	–	–	–	–	–	–	PIO, HiZ
142	A2	A2	VDDIO	CLOCK	PB9	I/O	XIN(10)	I	–	–	–	–	–	–	–	–	PIO, HiZ
87	G12	J10	VDDIO	GPIO	PB12	I/O	ERASE(9)	I	PWMC0_ PWML1	O	GTSUCO MP	O	–	–	PCK0	O	PIO, I, PD, ST
144	B2	A1	VDDIO	GPIO_A D	PB13	I/O	DAC0(11)	O	PWMC0_ PWML2	O	PCK0	O	SCK0	I/O	–	–	PIO, I, PU, ST
11	E4	F2	VDDIO	GPIO_A D	PC0	I/O	AFE1_A D9(5)	I	D0	I/O	PWMC0_ PWML0	O	–	–	–	–	PIO, I, PU, ST
38	J4	M3	VDDIO	GPIO_A D	PC1	I/O	–	–	D1	I/O	PWMC0_ PWML1	O	–	–	–	–	PIO, I, PU, ST
39	K4	N3	VDDIO	GPIO_A D	PC2	I/O	–	–	D2	I/O	PWMC0_ PWML2	O	–	–	–	–	PIO, I, PU, ST
40	L3	N4	VDDIO	GPIO_A D	PC3	I/O	–	–	D3	I/O	PWMC0_ PWML3	O	–	–	–	–	PIO, I, PU, ST
41	J5	L3	VDDIO	GPIO_A D	PC4	I/O	–	–	D4	I/O	–	–	–	–	–	–	PIO, I, PU, ST
58	L8	M8	VDDIO	GPIO_A D	PC5	I/O	–	–	D5	I/O	TIOA6	I/O	–	–	–	–	PIO, I, PU, ST
54	K7	L7	VDDIO	GPIO_A D	PC6	I/O	–	–	D6	I/O	TIOB6	I/O	–	–	–	–	PIO, I, PU, ST
48	M4	L5	VDDIO	GPIO_A D	PC7	I/O	–	–	D7	I/O	TCLK6	I	–	–	–	–	PIO, I, PU, ST
82	J12	K13	VDDIO	GPIO_A D	PC8	I/O	–	–	NWR0/N WE	O	TIOA7	I/O	–	–	–	–	PIO, I, PU, ST
86	G11	J11	VDDIO	GPIO_A D	PC9	I/O	–	–	NANDOE	O	TIOB7	I/O	–	–	–	–	PIO, I, PU, ST
90	F10	H12	VDDIO	GPIO_A D	PC10	I/O	–	–	NANDW E	O	TCLK7	I	–	–	–	–	PIO, I, PU, ST
94	F11	F13	VDDIO	GPIO_A D	PC11	I/O	–	–	NRD	O	TIOA8	I/O	–	–	–	–	PIO, I, PU, ST

19.4.4 Bus Matrix Priority Registers B For Slaves

Name: MATRIX_PRBSx
Offset: 0x84 + x*0x08 [x=0..8]
Reset: 0x00000222
Property: Read/Write

This register can only be written if the WPE bit is cleared in the Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							M12PR[1:0]	
Access							R/W	R/W
Reset							0	0

Bit	15	14	13	12	11	10	9	8
			M11PR[1:0]				M10PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			1	0

Bit	7	6	5	4	3	2	1	0
			M9PR[1:0]				M8PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			1	0			1	0

Bits 0:1, 4:5, 8:9, 12:13, 16:17 – MxPR Master 8 Priority
Fixed priority of Master x for accessing the selected slave. The higher the number, the higher the priority.

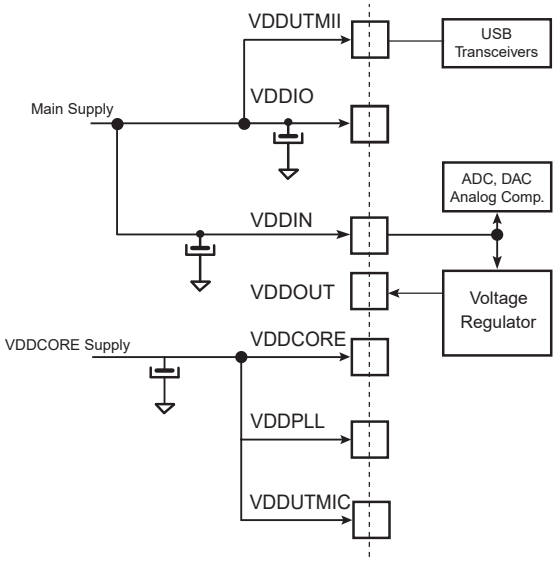
All the masters programmed with the same MxPR value for the slave make up a priority pool.

Round-robin arbitration is used in the lowest (MxPR = 0) and highest (MxPR = 3) priority pools.

Fixed priority is used in intermediate priority pools (MxPR = 1) and (MxPR = 2).

See “Arbitration Priority Scheme” for details.

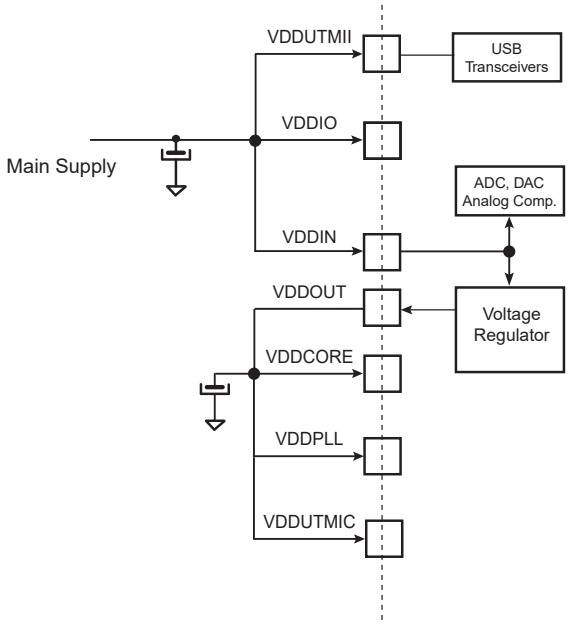
Figure 23-2. Separate Backup Supply Powering Scheme



Note: Restrictions
With main supply < 3.0V, USB is not usable.
With main supply < 2.7V, MediaLB is not usable.
With main supply < 2.0V, ADC, DAC and Analog comparator are not usable.
With main supply and VDDIN > 3V, all peripherals are usable.

When no separate backup supply for VDDIO is used, since the external voltage applied on VDDIO is kept, all of the I/O configurations (i.e., WKUP pin configuration) are maintained in Backup mode. When not using backup batteries, VDDIORDY is set so the user does not need to program it.

Figure 23-3. No Separate Backup Supply Powering Scheme



Note: Restrictions
with main supply < 2.0 V, USB and ADC/DAC and analog comparator are not usable.
With main supply > 2.0V and < 3V, USB is not usable.

This wait cycle is referred to as a read to write wait state in this document.

This wait cycle is applied in addition to chip select and reload user configuration wait states when they are to be inserted. See Figure 12-1.

35.12 Data Float Wait States

Some memory devices are slow to release the external bus. For such devices, it is necessary to add wait states (data float wait states) after a read access:

- before starting a read access to a different external memory
- before starting a write access to the same device or to a different external one.

The data float output time (t_{DF}) for each external memory device is programmed in the SMC_MODE.TDF_CYCLES field for the corresponding chip select. The value of SMC_MODE.TDF_CYCLES indicates the number of data float wait cycles (between 0 and 15) before the external device releases the bus, and represents the time allowed for the data output to go to high impedance after the memory is disabled.

Data float wait states do not delay internal memory accesses. Hence, a single access to an external memory with long t_{DF} will not slow down the execution of a program from internal memory.

The data float wait states management depends on SMC_MODE.READ_MODE and the SMC_MODE.TDF_MODE fields for the corresponding chip select.

35.12.1 SMC_MODE.READ_MODE

Setting SMC_MODE.READ_MODE to 1 indicates to the SMC that the NRD signal is responsible for turning off the tri-state buffers of the external memory device. The Data Float Period then begins after the rising edge of the NRD signal and lasts SMC_MODE.TDF_CYCLES MCK cycles.

When the read operation is controlled by the NCS signal (SMC_MODE.READ_MODE = 0), the TDF field gives the number of MCK cycles during which the data bus remains busy after the rising edge of NCS.

Figure 35-21 illustrates the Data Float Period in NRD-controlled mode (SMC_MODE.READ_MODE =1), assuming a data float period of 2 cycles (SMC_MODE.TDF_CYCLES = 2). Figure 35-22 shows the read operation when controlled by NCS (SMC_MODE.READ_MODE = 0) and SMC_MODE.TDF_CYCLES = 3.

Offset	Name	Bit Pos.								
		23:16								
		31:24								
0x58	ISI_DMA_C_DSCR	7:0	C_DSCR[5:0]							
		15:8	C_DSCR[13:6]							
		23:16	C_DSCR[21:14]							
		31:24	C_DSCR[29:22]							
0x5C ... 0xE3	Reserved									
0xE4	ISI_WPMR	7:0								WPEN
		15:8	WPKEY[7:0]							
		23:16	WPKEY[15:8]							
		31:24	WPKEY[23:16]							
0xE8	ISI_WPSR	7:0								WPVS
		15:8	WPVSRC[7:0]							
		23:16	WPVSRC[15:8]							
		31:24								

Bit 24 – P_OVR Preview Datapath Overflow (cleared on read)

Value	Description
0	No overflow
1	An overrun condition has occurred in input FIFO on the preview path. The overrun happens when the FIFO is full and an attempt is made to write a new sample to the FIFO since the last read of ISI_SR.

Bit 19 – SIP Synchronization in Progress
When the status of the preview or codec DMA channel is modified, a minimum amount of time is required to perform the clock domain synchronization.

Value	Description
0	The clock domain synchronization process is terminated.
1	This bit is set when the clock domain synchronization operation occurs. No modification of the channel status is allowed when this bit is set, to guarantee data integrity.

Bit 17 – CXFR_DONE Codec DMA Transfer has Terminated (cleared on read)

Value	Description
0	Codec transfer done not detected.
1	Codec transfer done detected. When set, this bit indicates that the data transfer on the codec channel has completed since the last read of ISI_SR.

Bit 16 – PXFR_DONE Preview DMA Transfer has Terminated (cleared on read)

Value	Description
0	Preview transfer done not detected.
1	Preview transfer done detected. When set, this bit indicates that the data transfer on the preview channel has completed since the last read of ISI_SR.

Bit 10 – VSYNC Vertical Synchronization (cleared on read)

Value	Description
0	Indicates that the vertical synchronization has not been detected since the last read of the ISI_SR.
1	Indicates that a vertical synchronization has been detected since the last read of the ISI_SR.

Bit 8 – CDC_PND Pending Codec Request

Value	Description
0	Indicates that no codec request is pending
1	Indicates that the request has been taken into account but cannot be serviced within the current frame. The operation is postponed to the next frame.

Bit 2 – SRST Module Software Reset Request has Terminated (cleared on read)

Value	Description
0	Indicates that the request is not completed (if a request was issued).
1	Software reset request has completed. This flag is reset after a read operation.

Bit 1 – DIS_DONE Module Disable Request has Terminated (cleared on read)

39.6.36 Host Global Interrupt Disable Register

Name: USBHS_HSTIDR
Offset: 0x0414
Property: Write-only

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Clears the corresponding bit in USBHS_HSTIMR.

Bit	31	30	29	28	27	26	25	24
	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	DMA_0	
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							PEP_9	PEP_8
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PEP_7	PEP_6	PEP_5	PEP_4	PEP_3	PEP_2	PEP_1	PEP_0
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		HWUPIEC	HSOFIEC	RXRSMIEC	RSMEDIEC	RSTIEC	DDISCIEC	DCONNIEC
Access								
Reset								

Bits 25, 26, 27, 28, 29, 30, 31 – DMA_ DMA Channel x Interrupt Disable

Bits 8, 9, 10, 11, 12, 13, 14, 15, 16, 17 – PEP_ Pipe x Interrupt Disable

Bit 6 – HWUPIEC Host Wakeup Interrupt Disable

Bit 5 – HSOFIEC Host Start of Frame Interrupt Disable

Bit 4 – RXRSMIEC Upstream Resume Received Interrupt Disable

Bit 3 – RSMEDIEC Downstream Resume Sent Interrupt Disable

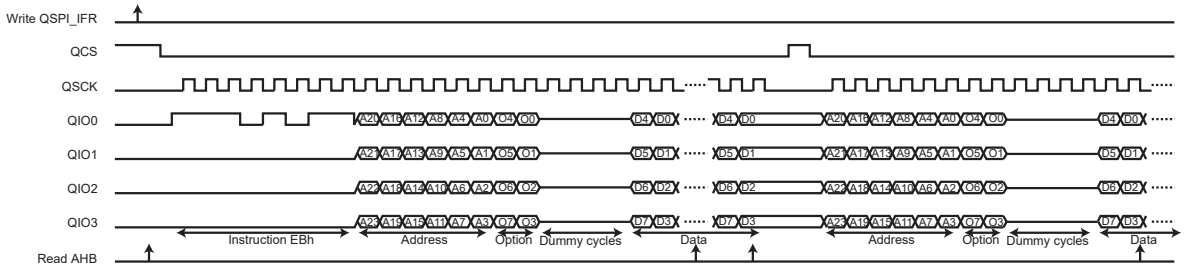
Bit 2 – RSTIEC USB Reset Sent Interrupt Disable

Bit 1 – DDISCIEC Device Disconnection Interrupt Disable

Bit 0 – DCONNIEC Device Connection Interrupt Disable

- Write a ‘1’ to QSPI_CR.LASTXFR.
- Wait for QSPI_SR.INSTRE to rise.

Figure 42-17. Instruction Transmission Waveform 7



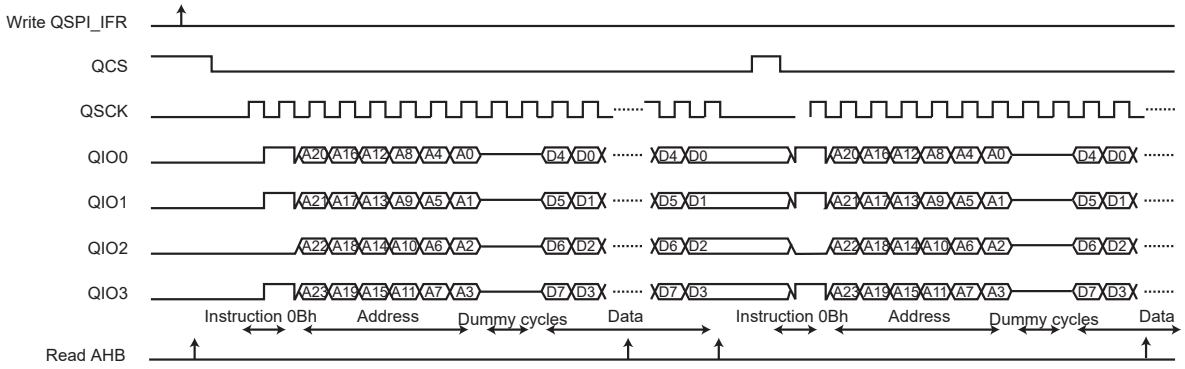
Example 8:

Instruction in Quad SPI, with address in Quad SPI, without option, with data read in Quad SPI, with two dummy cycles, with fetch.

Command: HIGH-SPEED READ (0Bh)

- Write 0x0000_000B in QSPI_ICR.
- Write 0x0002_20B6 in QSPI_IFR.
- Read QSPI_IFR (dummy read) to synchronize system bus accesses.
- Read data in the QSPI system bus memory space (0x80000000).
  Fetch is enabled, the address of the system bus read accesses is always used.
- Write a ‘1’ to QSPI_CR.LASTXFR.
- Wait for QSPI_SR.INSTRE to rise.

Figure 42-18. Instruction Transmission Waveform 8



Example 9:

Instruction in Quad SPI, without address, without option, with data read in Quad SPI, without dummy cycles, without fetch.

Command: HIGH-SPEED READ (05h)

- Write 0x0000_0005 in QSPI_ICR.
- Write 0x0000_0096 in QSPI_IFR.
- Read QSPI_IFR (dummy read) to synchronize system bus accesses.
- Read data in the QSPI system bus memory space (0x80000000).
  Fetch is disabled.
- Write a ‘1’ to QSPI_CR.LASTXFR.

43.6.5.8 Asynchronous Partial Wakeup (SleepWalking)

The TWIHS includes an asynchronous start condition detector. It is capable of waking the device up from a Sleep mode upon an address match (and optionally an additional data match), including Sleep modes where the TWIHS peripheral clock is stopped.

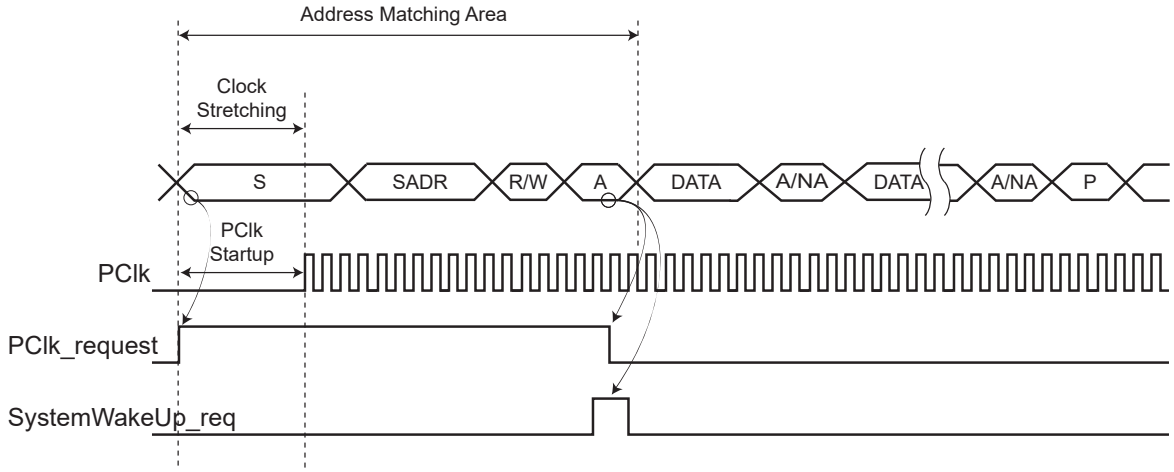
After detecting the START condition on the bus, the TWIHS stretches TWCK until the TWIHS peripheral clock has started. The time required for starting the TWIHS depends on which Sleep mode the device is in. After the TWIHS peripheral clock has started, the TWIHS releases its TWCK stretching and receives one byte of data (slave address) on the bus. At this time, only a limited part of the device, including the TWIHS module, receives a clock, thus saving power. If the address phase causes a TWIHS address match (and, optionally, if the first data byte causes data match as well), the entire device is woken up and normal TWIHS address matching actions are performed. Normal TWIHS transfer then follows. If the TWIHS is not addressed (or if the optional data match fails), the TWIHS peripheral clock is automatically stopped and the device returns to its original Sleep mode.

The TWIHS has the capability to match on more than one address. The SADR1EN, SADR2EN and SADR3EN bits in TWIHS_SMR enable address matching on additional addresses which can be configured through SADR1, SADR2 and SADR3 fields in the TWIHS_SWMR. The SleepWalking matching process can be extended to the first received data byte if TWIHS_SMR.DATAMEN is set and, in this case, a complete matching includes address matching and first received data matching. TWIHS_SWMR.DATAM configures the data to match on the first received byte.

When the system is in Active mode and the TWIHS enters Asynchronous Partial Wakeup mode, the flag SVACC must be programmed as the unique source of the TWIHS interrupt and the data match comparison must be disabled.

When the system exits Wait mode as the result of a matching condition, the SVACC flag is used to determine if the TWIHS is the source of exit.

Figure 43-39. Address Match Only (Data Matching Disabled)



Bit 9 – RXDMA Single or Multiple DMA Controller Channels for Receiver

Value	Description
0	The receiver uses only one DMA Controller channel for all audio channels.
1	The receiver uses one DMA Controller channel per audio channel.

Bit 8 – RXMONO Receive Mono

Value	Description
0	Stereo
1	Mono, with left audio samples duplicated to right audio channel by the I2SC.

Bits 7:6 – FORMAT[1:0] Data Format

Value	Name	Description
0	I2S	I^2S format, stereo with I2SC_WS low for left channel, and MSB of sample starting one I2SC_CK period after I2SC_WS edge
1	LJ	Left-justified format, stereo with I2SC_WS high for left channel, and MSB of sample starting on I2SC_WS edge
2	–	Reserved
3	–	Reserved

Bits 4:2 – DATALENGTH[2:0] Data Word Length

Value	Name	Description
0	32_BITS	Data length is set to 32 bits.
1	24_BITS	Data length is set to 24 bits.
2	20_BITS	Data length is set to 20 bits.
3	18_BITS	Data length is set to 18 bits.
4	16_BITS	Data length is set to 16 bits.
5	16_BITS_COMPACT	Data length is set to 16-bit compact stereo. Left sample in bits 15:0 and right sample in bits 31:16 of same word.
6	8_BITS	Data length is set to 8 bits.
7	8_BITS_COMPACT	Data length is set to 8-bit compact stereo. Left sample in bits 7:0 and right sample in bits 15:8 of the same word.

Bit 0 – MODE Inter-IC Sound Controller Mode

Value	Name	Description
0	SLAVE	I2SC_CK and I2SC_WS pin inputs used as bit clock and word select/frame synchronization.
1	MASTER	Bit clock and word select/frame synchronization generated by I2SC from MCK and output to I2SC_CK and I2SC_WS pins. Peripheral clock or GCLK is output as master clock on I2SC_MCK if I2SC_MR.IMCKMODE is set.

The DMAC uses the trigger flags, TXRDY and RXRDY, to write or read into the USART. The DMAC always writes in the Transmit Holding register (US_THR) and it always reads in the Receive Holding register (US_RHR). The size of the data written or read by the DMAC in the USART is always a byte.

46.6.9.16.1 Master Node Configuration

The user can choose between two DMAC modes by the PDCM bit in the US_LINMR:

- PDCM = 1: the LIN configuration is stored in the WRITE buffer and it is written by the DMAC in the Transmit Holding register US_THR (instead of the LIN Mode register US_LINMR). Because the DMAC transfer size is limited to a byte, the transfer is split into two accesses. During the first access the bits, NACT, PARDIS, CHKDIS, CHKTYP, DLM and FSDIS are written. During the second access the 8-bit DLC field is written.
- PDCM = 0: the LIN configuration is not stored in the WRITE buffer and it must be written by the user in US_LINMR.

The WRITE buffer also contains the Identifier and the DATA, if the USART sends the response (NACT = PUBLISH).

The READ buffer contains the DATA if the USART receives the response (NACT = SUBSCRIBE).

Figure 46-51. Master Node with DMAC (PDCM = 1)

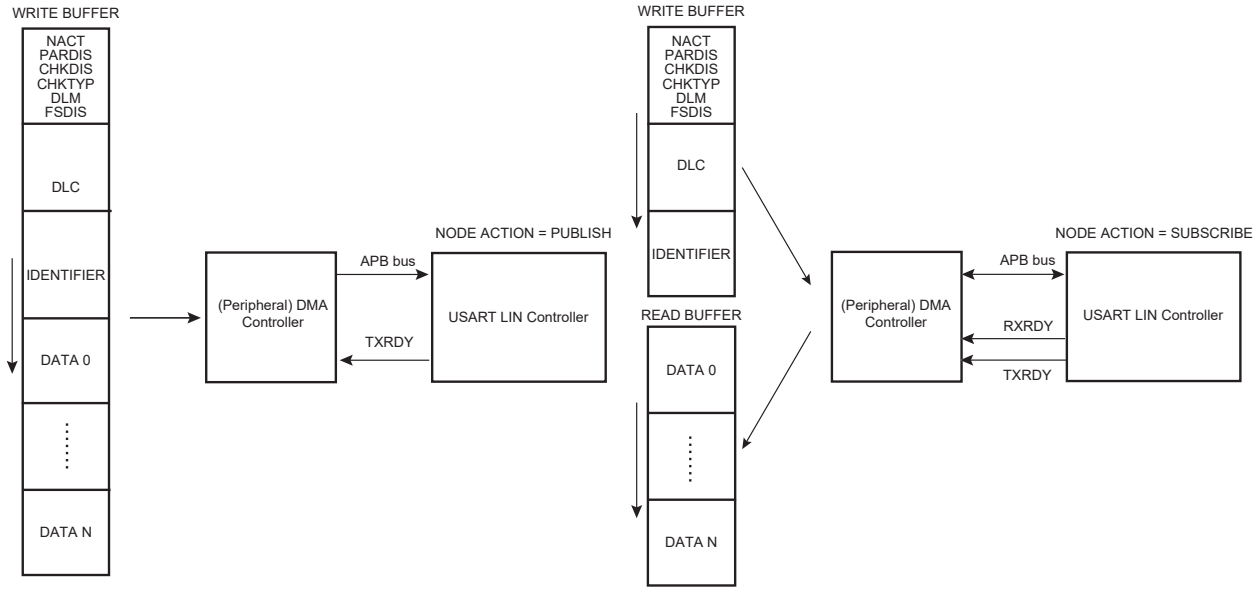


Figure 46-52. Master Node with DMAC (PDCM = 0)

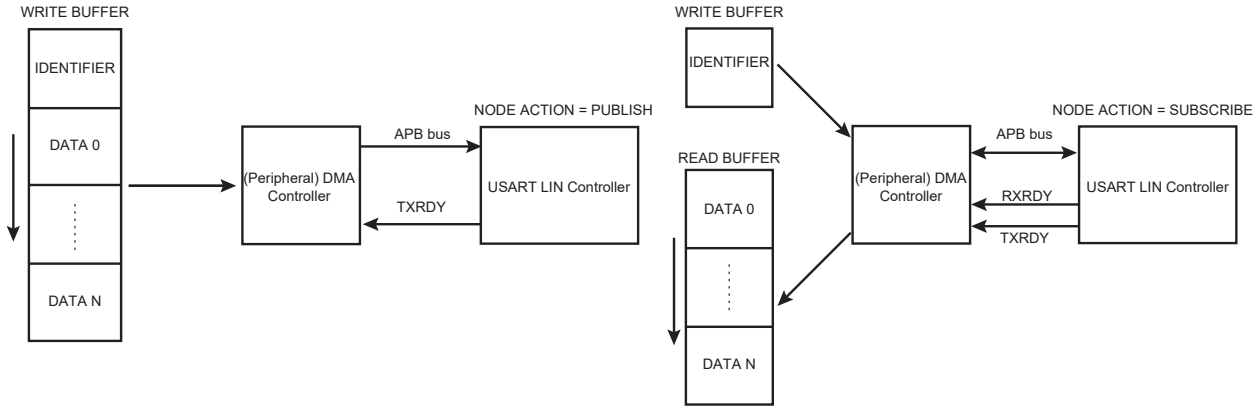
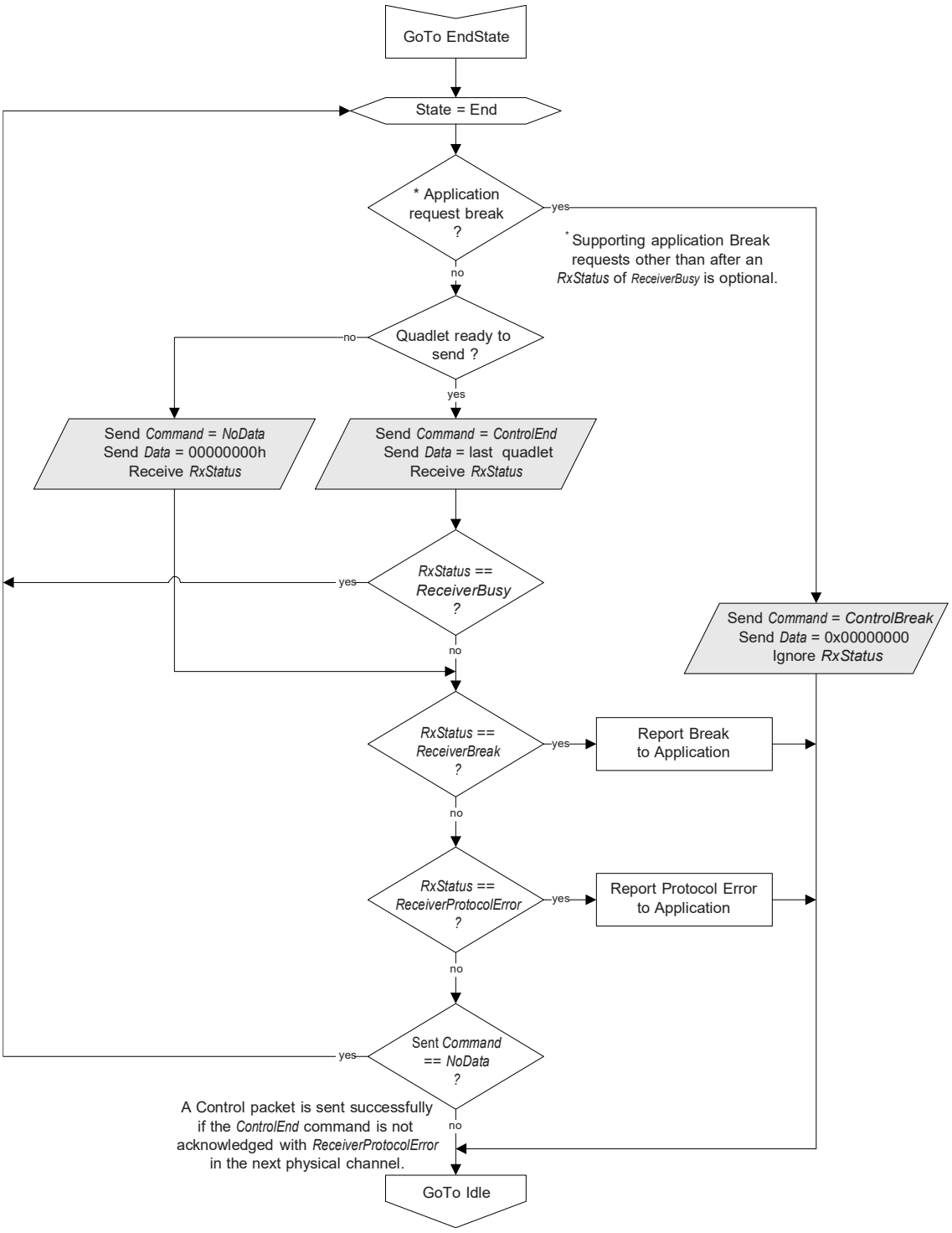


Figure 48-8. Control Packet Tx Device Protocol: End



48.7.4 MediaLB System Status Register

Name: MLB_MSS
Offset: 0x020
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			SERVREQ	SWSYSCMD	CSSYSCMD	ULKSYSCMD	LKSYSCMD	RSTSYSCMD
Access								
Reset			0	0	0	0	0	0

Bit 5 – SERVREQ Service Request Enabled

Value	Description
0	The MediaLB block responds with a “device present” system response.
1	The MediaLB block responds with a “device present, request service” system response if a matching channel scan system command is detected.

Bit 4 – SWSYSCMD Software System Command Detected in the System Quadlet (cleared by writing a 0)
Set by hardware, cleared by software. Data is stored in the MLB_MSD register for this command.

Bit 3 – CSSYSCMD Channel Scan System Command Detected in the System Quadlet (cleared by writing a 0)
Set by hardware, cleared by software. If the node address specified in Data quadlet matches the value in MLB_MLBC1.NDA, the device responds either “device present” or “device present, request service” system response in the next system quadlet.

Bit 2 – ULKSYSCMD Network Unlock System Command Detected in the System Quadlet (cleared by writing a 0)
Set by hardware, cleared by software.

48.7.21 MIF Data Write Enable 2 Register

Name: MLB_MDWE2
Offset: 0x0D8
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	MASK: Bitwise Write Enable for CTR Data - bits[95:64]							
Access								
Reset	0	0	0	0	0	0	0	0

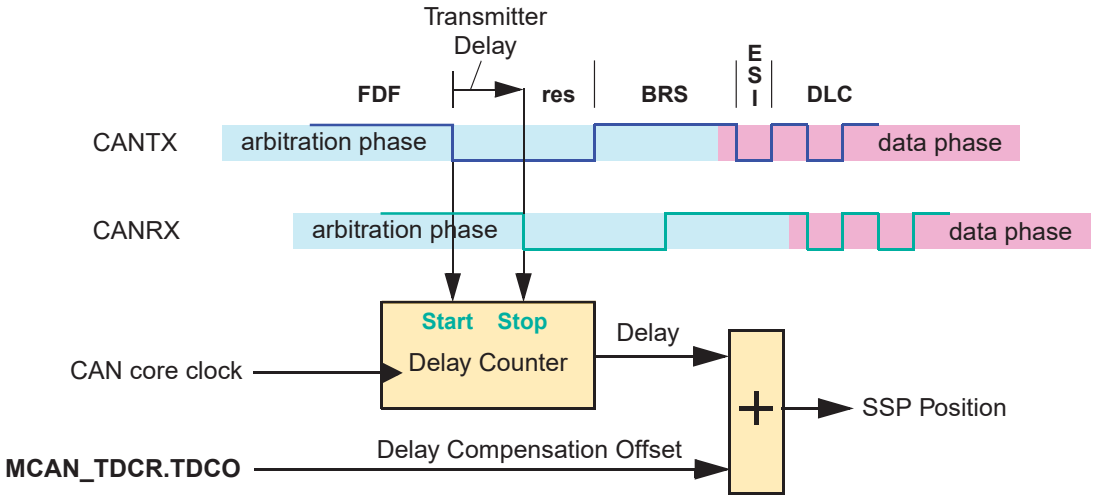
Bit	23	22	21	20	19	18	17	16
	MASK: Bitwise Write Enable for CTR Data - bits[95:64]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	MASK: Bitwise Write Enable for CTR Data - bits[95:64]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MASK: Bitwise Write Enable for CTR Data - bits[95:64]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MASK: Bitwise Write Enable for CTR Data - bits[95:64]
MASK[n] = 1 indicates that CTR data [n] is enabled.

Figure 49-2. Transmitter Delay Measurement



To avoid that a dominant glitch inside the received FDF bit ends the delay compensation measurement before the falling edge of the received res bit, resulting in a to early SSP position, the use of a transmitter delay compensation filter window can be enabled by programming MCAN_TDCR.TDCF.

This defines a minimum value for the SSP position. Dominant edges on CANRX, that would result in an earlier SSP position are ignored for transmitter delay measurement. The measurement is stopped when the SSP position is at least MCAN_TDCR.TDCF AND CANRX is low.

49.5.1.5 Restricted Operation Mode

In Restricted Operation mode, the node is able to receive data and remote frames and to give acknowledge to valid frames, but it does not send data frames, remote frames, active error frames, or overload frames. In case of an error condition or overload condition, it does not send dominant bits, instead it waits for the occurrence of bus idle condition to resynchronize itself to the CAN communication. The error counters are not incremented. The processor can set the MCAN into Restricted Operation mode by setting bit MCAN_CCCR.ASM. The bit can only be set by the processor when both MCAN_CCCR.CCE and MCAN_CCCR.INIT are set to '1'. The bit can be reset by the processor at any time.

Restricted Operation mode is automatically entered when the Tx Handler was not able to read data from the Message RAM in time. To leave Restricted Operation mode, the processor has to reset MCAN_CCCR.ASM.

The Restricted Operation mode can be used in applications that adapt themselves to different CAN bit rates. In this case the application tests different bit rates and leaves the Restricted Operation mode after it has received a valid frame.

Note: The Restricted Operation Mode must not be combined with the Loop Back mode (internal or external).

49.5.1.6 Bus Monitoring Mode

The MCAN is set in Bus Monitoring mode by setting MCAN_CCCR.MON. In Bus Monitoring mode (see ISO11898-1, 10.12 Bus monitoring), the MCAN is able to receive valid data frames and valid remote frames, but cannot start a transmission. In this mode, it sends only recessive bits on the CAN bus. If the MCAN is required to send a dominant bit (ACK bit, overload flag, active error flag), the bit is rerouted internally so that the MCAN monitors this dominant bit, although the CAN bus may remain in recessive state. In Bus Monitoring mode, the Tx Buffer Request Pending register (MCAN_TXBRP) is held in reset state.

49.6.44 MCAN Transmit Buffer Cancellation Finished Interrupt Enable

Name: MCAN_TXBCIE
Offset: 0xE4
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – CFIEx Cancellation Finished Interrupt Enable for Transmit Buffer x
Each Transmit Buffer has its own Cancellation Finished Interrupt Enable bit.

Value	Description
0	Cancellation finished interrupt disabled.
1	Cancellation finished interrupt enabled.

51.7.7 PWM Interrupt Mask Register 1

Name: PWM_IMR1
Offset: 0x18
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					FCHID3	FCHID2	FCHID1	FCHID0
Access					R	R	R	R
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					CHID3	CHID2	CHID1	CHID0
Access					R	R	R	R
Reset					0	0	0	0

Bits 16, 17, 18, 19 – FCHIDx Fault Protection Trigger on Channel x Interrupt Mask

Bits 0, 1, 2, 3 – CHIDx Counter Event on Channel x Interrupt Mask

Symbol		VDDIO Supply		Unit
	Parameter	Min	Max	
SMC_5	A0–A22 Valid before NRD High	(NRD_SETUP + NRD_PULSE) × t_{CPMCK} - 4.3	–	ns
SMC_6	NCS low before NRD High	(NRD_SETUP + NRD_PULSE - NCS_RD_SETUP) × t_{CPMCK} - 2.4	–	ns
SMC_7	NRD Pulse Width	NRD_PULSE × t_{CPMCK} - 0.3	–	ns

Table 58-61. SMC Read Signals - NCS Controlled (READ_MODE = 0)

Symbol		VDDIO Supply		Unit
	Parameter	Min	Max	
NO HOLD Settings (NCS_RD_HOLD = 0)				
SMC_8	Data Setup before NCS High	21.4	–	ns
SMC_9	Data Hold after NCS High	0	–	ns
HOLD Settings (NCS_RD_HOLD ≠ 0)				
SMC_{10}	Data Setup before NCS High	11.7	–	ns
SMC_{11}	Data Hold after NCS High	0	–	ns
HOLD or NO HOLD Settings (NCS_RD_HOLD ≠ 0, NCS_RD_HOLD = 0)				
SMC_{12}	A0–A22 valid before NCS High	(NCS_RD_SETUP + NCS_RD_PULSE) × t_{CPMCK} - 3.9	–	ns
SMC_{13}	NRD low before NCS High	(NCS_RD_SETUP + NCS_RD_PULSE - NRD_SETUP) × t_{CPMCK} - 4.2	–	ns
SMC_{14}	NCS Pulse Width	NCS_RD_PULSE length × t_{CPMCK} - 0.2	–	ns

58.13.1.9.3 Write Timings

Table 58-62. SMC Write Signals - NWE Controlled (WRITE_MODE = 1)

Symbol	VDDIO Supply	1.8V Domain	3.3V Domain	1.8V Domain	3.3V Domain	Unit
	Parameter	Min		Max		
HOLD or NO HOLD Settings (NWE_HOLD ≠ 0, NWE_HOLD = 0)						
SMC_{15}	Data Out Valid before NWE High	NWE_PULSE × t_{CPMCK} - 5.4	NWE_PULSE × t_{CPMCK} - 4.6	–	–	ns
SMC_{16}	NWE Pulse Width	NWE_PULSE × t_{CPMCK} - 0.7	NWE_PULSE × t_{CPMCK} - 0.3	–	–	ns
SMC_{17}	A0–A22 valid before NWE low	NWE_SETUP × t_{CPMCK} - 4.9	NWE_SETUP × t_{CPMCK} - 4.2	–	–	ns

Signal Name	Recommended Pin Connection	Description
		Decoupling/filtering capacitors must be added to improve startup stability and reduce source voltage drop. Supply ripple must not exceed 20 mVrms for 10 kHz to 20 MHz range. **WARNING** Powerup and powerdown sequences given in the "Power Considerations" chapter must be respected.
VDDPLL	Decoupling/filtering capacitors ferrite beads (100 nF and 470 Ohm @ 100 MHz) (1) (2)	Powers the PLLA and the fast RC oscillator. The VDDPLL power supply pin draws small current, but it is noise sensitive. Care must be taken in VDDPLL power supply routing, decoupling and also on bypass capacitors. Supply ripple must not exceed 20 mVrms for 10 kHz to 10 MHz range and 10 mVrms for higher frequencies.
VDDUTMIC	Decoupling/filtering capacitors ferrite beads (100 nF and 470 Ohm @ 100 MHz) (1) (2)	Powers the USB transceiver core. Must always be connected even if the USB is not used. Decoupling/filtering capacitors/ferrite beads must be added to improve startup stability and reduce source voltage drop. Supply ripple must not exceed 10 mVrms for 10 kHz to 10 MHz range.
GND	Voltage Regulator, Core Chip and Peripheral I/O lines ground	GND pins are common to VDDIN, VDDCORE and VDDIO pins. GND pins should be connected as shortly as possible to the system ground plane.
GNDUTMI	UDPHS and UHPHS UTMI+ Core and interface ground	GNDUTMI pins are common to VDDUTMII and VDDUTMIC pins. GNDUTMI pins should be connected as shortly as possible to the system ground plane.
GNDPLL	PLLA cell and Main Oscillator ground	GNDPLL pin is provided for VDDPLL pin. GNDPLL pin should be connected as shortly as possible to the system ground plane.
GNDANA	Analog ground	GNDANA pins are common to AFE, DAC and ACC supplied by VDDIN pin. GNDANA pins should be connected as shortly as possible to the system ground plane.
GNDPLLUSB	USB PLL ground	GNDPLLUSB pin is provided for VDDPLLUSB pin. GNDPLLUSB pin should be connected as shortly as possible to the system ground plane.

Date	Changes
	Section 10.1.5.9 “Fast Flash Programming Interface”: removed ‘serial JTAG interface’.
	Section 11. “Event System” Table 11-1 “ Event Mapping List“: in row “Audio clock recovery from Ethernet’ changed the text in Description column.
	Section 13. “Peripherals” Table 13-1 “Peripheral Identifiers“: modfied content of column ‘Description’ for clarity. Section 13.2 “Peripheral Signal Multiplexing on I/O Lines”: corrected PIOC to PIOD for 100-pin version. Moved Section 13.3 “Peripheral Mapping to DMA” to Section 35.3 “DMA Controller Peripheral Connections”.
24-Feb-15	Section 15. “Debug and Test Features” Section 15.1 “Description”: removed references to JTAG Debug Port and JTAG-DP. Updated Figure 15-1 “Debug and Test Block Diagram”: added Cortex-M7, ETM and PCK3 blocks and trace pins. Renamed block ‘SWJ-DP’ to ‘SW-DP’. Table 15-1 “Debug and Test Signal List”: removed TRACECTL. Updated Figure 15-4 “Debug Architecture”. added ETM and Trace Port blocks. Removed TPIU. Section 15.6.5 “Serial Wire Debug Port (SW-DP) Pins”: removed all references to JTAG Debug Port and JTAG-DP. Section 15.6.6 “Embedded Trace Module (ETM) Pins”: removed TRACECTL from bullet points. Updated Section 15.6.7 “Flash Patch Breakpoint (FPB)” . Section 15.6.9.2 “Asynchronous Mode”: removed reference to JTAG Debug Port and JTAG debug mode.
	Section 16. “SAM-BA Boot Program” Section 16.6.4 “In Application Programming (IAP) Feature”: replaced software code example.
	Section 18. “Bus Matrix (MATRIX)” Table 18-3 “Master to Slave Access”: changed Master 4/Slave 4 access from possible (“x”) to not possble (‘-”) Table 18-4 “Register Mapping”: changed reset value for CCFG_SYSIO register. Section 18.12.7 “System I/O and CAN1 Configuration Register”: corrected typo in CAN1DMABA bit name. Section 18.11 “Register Write Protection”: replaced “The WPVS bit is automatically cleared after reading the MATRIX_WPSR” with “The WPVS flag is reset by writing the MATRIX_WPMR with the appropriate access key WPKEY”