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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70n20a-an

Table 18-1. Signal Description List

Signal Name	Function	Type	Active Level	Comments
Power				
VDDIO	I/O Lines Power Supply	Power	–	–
VDDCORE	Core Power Supply	Power	–	–
VDDPLL	PLL Power Supply	Power	–	–
GND	Ground	Ground	–	–
Clocks				
XIN	Main Clock Input	Input	–	–
Test				
TST	Test Mode Select	Input	High	Must be connected to VDDIO
PGMEN0	Test Mode Select	Input	Low	Must be connected to GND
PGMEN1	Test Mode Select	Input	High	Must be connected to VDDIO
PIO				
PGMNCMD	Valid command available	Input	Low	Pulled-up input at reset
PGMRDY	0: Device is busy 1: Device is ready for a new command	Output	High	Pulled-up input at reset
PGMNOE	Output Enable (active high)	Input	Low	Pulled-up input at reset
PGMNVALID	0: DATA[15:0] is in input mode 1: DATA[15:0] is in output mode	Output	Low	Pulled-up input at reset
PGMM[3:0]	Specifies DATA type (see Table 18-2)	Input	–	Pulled-up input at reset
PGMD[15:0]	Bidirectional data bus	Input/Output	–	Pulled-up input at reset

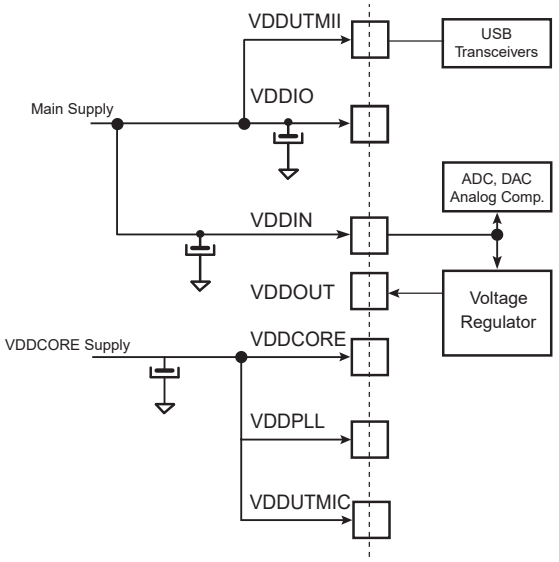
18.3.2 Signal Names

Depending on the MODE settings, DATA is latched in different internal registers.

Table 18-2. Mode Coding

MODE[3:0]	Symbol	Data
0000	CMDE	Command Register
0001	ADDR0	Address Register LSBs
0010	ADDR1	–
0011	ADDR2	–

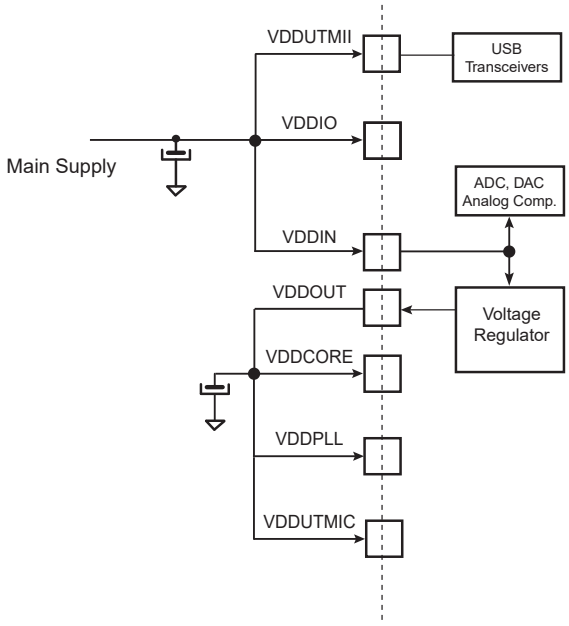
Figure 23-2. Separate Backup Supply Powering Scheme



Note: Restrictions
With main supply < 3.0V, USB is not usable.
With main supply < 2.7V, MediaLB is not usable.
With main supply < 2.0V, ADC, DAC and Analog comparator are not usable.
With main supply and VDDIN > 3V, all peripherals are usable.

When no separate backup supply for VDDIO is used, since the external voltage applied on VDDIO is kept, all of the I/O configurations (i.e., WKUP pin configuration) are maintained in Backup mode. When not using backup batteries, VDDIORDY is set so the user does not need to program it.

Figure 23-3. No Separate Backup Supply Powering Scheme



Note: Restrictions
with main supply < 2.0 V, USB and ADC/DAC and analog comparator are not usable.
With main supply > 2.0V and < 3V, USB is not usable.

31.20.21 PMC Write Protection Mode Register

Name: PMC_WPMR
Offset: 0x00E4
Reset: 0x0
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	WPKEY[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	WPKEY[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	WPKEY[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
								WPEN
Access								
Reset								0

Bits 31:8 – WPKEY[23:0] Write Protection Key

Value	Name	Description
0x504D43	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

Bit 0 – WPEN Write Protection Enable
See "Register Write Protection" for the list of registers that can be write-protected.

Value	Description
0	Disables the write protection if WPKEY corresponds to 0x504D43 (“PMC” in ASCII).
1	Enables the write protection if WPKEY corresponds to 0x504D43 (“PMC” in ASCII).

32.6.1.7 PIO Input Filter Enable Register

Name: PIO_IFER
Offset: 0x0020
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Input Filter Enable

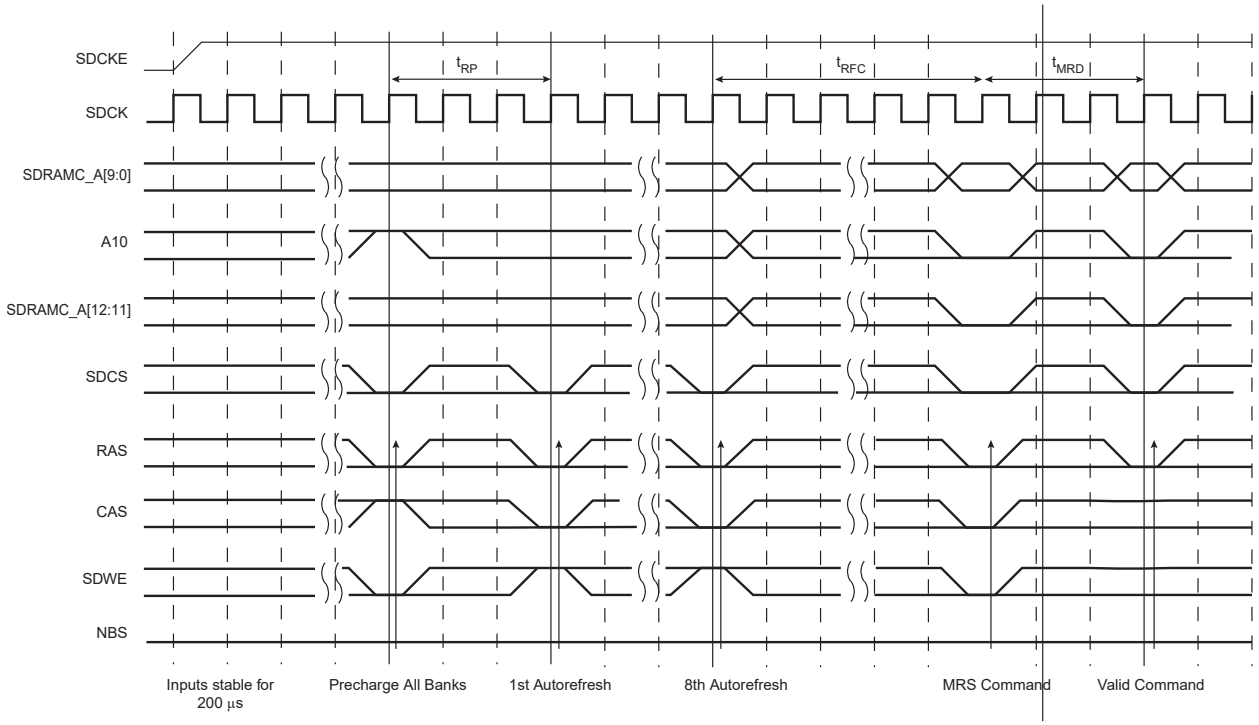
Value	Description
0	No effect.
1	Enables the input glitch filter on the I/O line.

8. A Mode Register set (MRS) cycle is issued to program the parameters of the SDRAM, in particular CAS latency and burst length. The application must write a 3 to the MODE field in the SDRAMC_MR. Read the SDRAMC_MR and add a memory barrier assembler instruction just after the read. Perform a write access to the SDRAM. The write address must be chosen so that BA[1:0] are set to 0. For example, with a 16-bit 128 MB SDRAM (12 rows, 9 columns, 4 banks) bank address, the SDRAM write access should be done at the address 0x70000000.
9. For mobile SDRAM initialization, an Extended Mode Register set (EMRS) cycle is issued to program the SDRAM parameters (TCSR, PASR, DS). The application must set the MODE field to 5 in the SDRAMC_MR. Read the SDRAMC_MR and add a memory barrier assembler instruction just after the read. Perform a write access to the SDRAM. The write address must be chosen so that BA[1] or BA[0] are set to 1. For example, with a 16-bit 128 MB SDRAM (12 rows, 9 columns, 4 banks) bank address, the SDRAM write access should be done at address 0x70800000 or 0x70400000.
10. The application must go into Normal mode. Configure MODE to 0 in the SDRAMC_MR. Read the SDRAMC_MR and add a memory barrier assembler instruction just after the read. Perform a write access at any location in the SDRAM.
11. Write the refresh rate into the COUNT field in the Refresh Timer register (SDRAMC_TR). (Refresh rate = delay between refresh cycles). The SDRAM device requires a refresh every 15.625 µs or 7.81 µs. With a 100 MHz frequency, the Refresh Timer register must be set with the value 1562 (15.625 µs x 100 MHz) or 781 (7.81 µs x 100 MHz).

After initialization, the SDRAM devices are fully functional.

Note: The instructions stated in Step 5 of the initialization process must be respected to make sure the subsequent commands issued by the SDRAMC are taken into account.

Figure 34-1. SDRAM Device Initialization Sequence



Frame Segment	Value
Control (Octet 74)	00
Other stuff (Octets 75–168)	—

Table 38-7. Example of Delay Request Frame in 1588 Version 1 Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	—
SA (Octets 6–11)	—
Type (Octets 12–13)	0800
IP stuff (Octets 14–22)	—
UDP (Octet 23)	11
IP stuff (Octets 24–29)	—
IP DA (Octets 30–32)	E00001
IP DA (Octet 33)	81 or 82 or 83 or 84
Source IP port (Octets 34–35)	—
Dest IP port (Octets 36–37)	013F
Other stuff (Octets 38–42)	—
Version PTP (Octet 43)	01
Other stuff (Octets 44–73)	—
Control (Octet 74)	01
Other stuff (Octets 75–168)	—

For 1588 version 1 messages, sync and delay request frames are indicated by the GMAC if the frame type field indicates TCP/IP, UDP protocol is indicated, the destination IP address is 224.0.1.129/130/131 or 132, the destination UDP port is 319 and the control field is correct.

The control field is 0x00 for sync frames and 0x01 for delay request frames.

For 1588 version 2 messages, the type of frame is determined by looking at the message type field in the first byte of the PTP frame. Whether a frame is version 1 or version 2 can be determined by looking at the version PTP field in the second byte of both version 1 and version 2 PTP frames.

In version 2 messages sync frames have a message type value of 0x0, delay_req have 0x1, Pdelay_Req have 0x2 and Pdelay_Resp have 0x3.

Table 38-8. Example of Sync Frame in 1588 Version 2 (UDP/IPv4) Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	—

Writing a '0' to this bit disables the Management Port, and forces MDIO to high impedance state and MDC to low impedance.

Value	Description
0	Management Port is disabled.
1	Management Port is enabled.

Bit 3 – TXEN Transmit Enable
Writing a '1' to this bit enables the GMAC transmitter to send data.

Writing a '0' to this bit stops transmission immediately, the transmit pipeline and control registers is cleared, and the Transmit Queue Pointer Register will be set to point to the start of the transmit descriptor list.

Value	Description
0	Transmit is disabled.
1	Transmit is enabled.

Bit 2 – RXEN Receive Enable
Writing a '1' to this bit enables the GMAC to receive data.

Writing a '0' to this bit stops frame reception immediately, and the receive pipeline is cleared. The Receive Queue Pointer Register is not affected.

Value	Description
0	Receive is disabled.
1	Receive is enabled.

Bit 1 – LBL Loop Back Local
Writing '1' to this bit connects GTX to GRX, GTXEN to GRXDV, and forces full duplex mode.

GRXCK and GTXCK may malfunction as the GMAC is switched into and out of internal loop back. It is important that receive and transmit circuits have already been disabled when making the switch into and out of internal loop back.

Value	Description
0	Loop back local is disabled.
1	Loop back local is enabled.

Bit 5 – EORSM End of Resume Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.EORSMC bit is written to one to acknowledge the interrupt.
1	Set when the USBHS detects a valid “End of Resume” signal initiated by the host. This triggers a USB interrupt if USBHS_DEVIMR.EORSME = 1.

Bit 4 – WAKEUP Wakeup Interrupt
This interrupt is generated even if the clock is frozen by the USBHS_CTRL.FRZCLK bit.

Value	Description
0	Cleared when the USBHS_DEVICR.WAKEUPC bit is written to one to acknowledge the interrupt (USB clock inputs must be enabled before), or when the Suspend (SUSP) interrupt bit is set.
1	Set when the USBHS is reactivated by a filtered non-idle signal from the lines (not by an upstream resume). This triggers an interrupt if USBHS_DEVIMR.WAKEUPE = 1.

Bit 3 – EORST End of Reset Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.EORSTC bit is written to one to acknowledge the interrupt.
1	Set when a USB “End of Reset” has been detected. This triggers a USB interrupt if USBHS_DEVIMR.EORSTE = 1.

Bit 2 – SOF Start of Frame Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.SOFC bit is written to one to acknowledge the interrupt.
1	Set when a USB “Start of Frame” PID (SOF) has been detected (every 1 ms). This triggers a USB interrupt if SOFE = 1. The FNUM field is updated. In High-speed mode, the MFNUM field is cleared.

Bit 1 – MSOF Micro Start of Frame Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.MSOFC bit is written to one to acknowledge the interrupt.
1	Set in High-speed mode when a USB “Micro Start of Frame” PID (SOF) has been detected (every 125 µs). This triggers a USB interrupt if MSOFE = 1. The MFNUM field is updated. The FNUM field is unchanged.

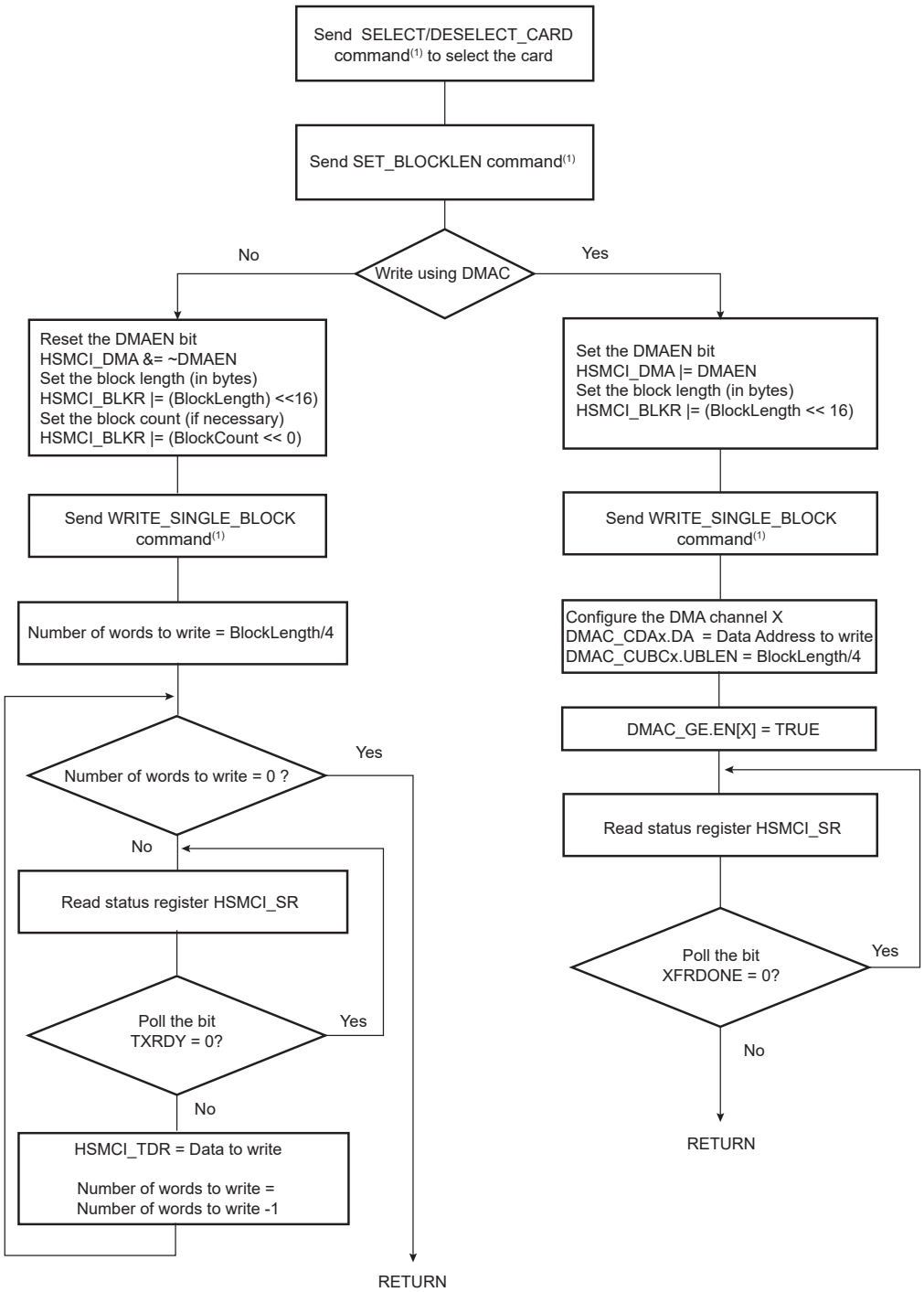
Bit 0 – SUSP Suspend Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.SUSPC bit is written to one to acknowledge the interrupt, or when the Wakeup (WAKEUP) interrupt bit is set.
1	Set when a USB “Suspend” idle bus state has been detected for 3 frame periods (J state for 3 ms). This triggers a USB interrupt if USBHS_DEVIMR.SUSPE = 1.

If set, the bit DMAEN in the HSMCI DMA Condiguration Register (HSMCI_DMA) enables DMA transfer.

The flowchart, Write Functional Flow Diagram, shows how to write a single block with or without use of DMA facilities. Polling or interrupt method can be used to wait for the end of write according to the contents of the HSMCI Interrupt Mask Register (HSMCI_IMR).

Figure 40-9. Write Functional Flow Diagram



Note: 1. It is assumed that this command has been correctly sent (see Command/Response Functional Flow Diagram).

40.14.4 HSMCI SDCard/SDIO Register

Name: HSMCI_SDCR
Offset: 0x0C
Reset: 0x0
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the HSMCI Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	SDCBUS[1:0]						SDCSEL[1:0]	
Access								
Reset	0	0					0	0

Bits 7:6 – SDCBUS[1:0] SDCard/SDIO Bus Width

Value	Name	Description
0	1	1 bit
1	Reserved	
2	4	4 bits
3	8	8 bits

Bits 1:0 – SDCSEL[1:0] SDCard/SDIO Slot

Value	Name	Description
0	SLOTA	Slot A is selected.
1	SLOTB	Reserved
2	SLOTC	Reserved
3	SLOTD	Reserved

43.7.12 TWIHS Receive Holding Register

Name: TWIHS_RHR
Offset: 0x30
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	RXDATA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – RXDATA[7:0] Master or Slave Receive Holding Data

45.8.8 I2SC Interrupt Mask Register

Name: I2SC_IMR
Offset: 0x1C
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		TXUR	TXRDY			RXOR	RXRDY	
Access		R	R			R	R	
Reset		0	0			0	0	

Bit 6 – TXUR Transmit Underflow Interrupt Disable

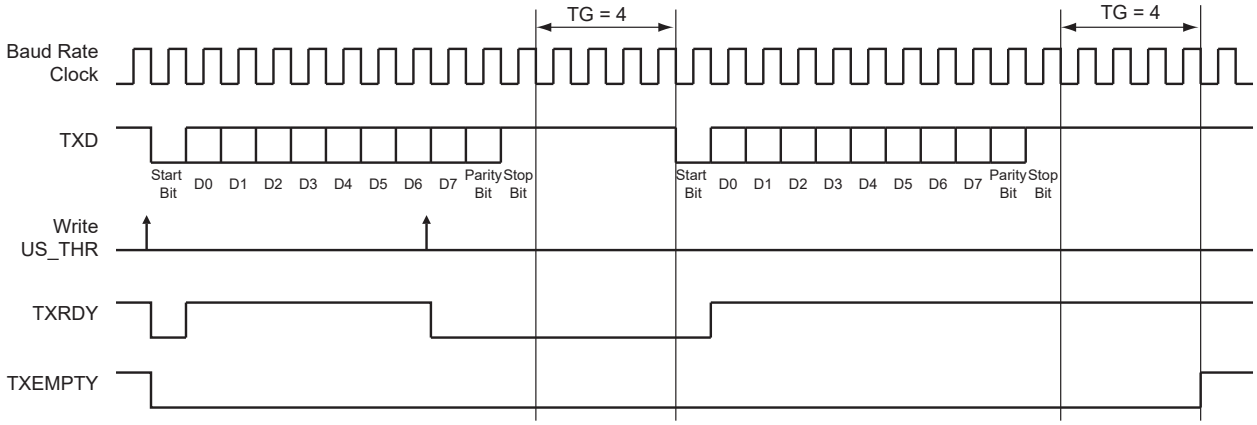
Value	Description
0	The corresponding interrupt is disabled. This bit is cleared when the corresponding bit in I2SC_IDR is written to ’1’.
1	The corresponding interrupt is enabled. This bit is set when the corresponding bit in I2SC_IER is written to ’1’.

Bit 5 – TXRDY Transmit Ready Interrupt Disable

Value	Description
0	The corresponding interrupt is disabled. This bit is cleared when the corresponding bit in I2SC_IDR is written to ’1’.
1	The corresponding interrupt is enabled. This bit is set when the corresponding bit in I2SC_IER is written to ’1’.

Bit 2 – RXOR Receiver Overrun Interrupt Disable

Figure 46-22. Timeguard Operations



The following table indicates the maximum length of a timeguard period that the transmitter can handle depending on the baud rate.

Table 46-7. Maximum Timeguard Length Depending on Baud Rate

Baud Rate (bit/s)	Bit Time (µs)	Timeguard (ms)
1,200	833	212.50
9,600	104	26.56
14,400	69.4	17.71
19,200	52.1	13.28
28,800	34.7	8.85
38,400	26	6.63
56,000	17.9	4.55
57,600	17.4	4.43
115,200	8.7	2.21

46.6.3.11 Receiver Timeout

The Receiver Timeout provides support in handling variable-length frames. This feature detects an idle condition on the RXD line. When a timeout is detected, US_CSR.TIMEOUT rises and can generate an interrupt, thus indicating to the driver an end of frame.

The timeout delay period (during which the receiver waits for a new character) is programmed in the TO field of the Receiver Timeout register (US_RTOR). If TO is written to ‘0’, the Receiver Timeout is disabled and no timeout is detected. US_CSR.TIMEOUT remains at ‘0’. Otherwise, the receiver loads a 16-bit counter with the value programmed in US_RTOR.TO. This counter is decremented at each bit period and reloaded each time a new character is received. If the counter reaches 0, TIMEOUT rises. Then, the user can either:

- Stop the counter clock until a new character is received. This is performed by writing a ‘1’ to US_CR.STTTO. In this case, the idle state on RXD before a new character is received will not provide a timeout. This prevents having to handle an interrupt before a character is received and allows waiting for the next idle state on RXD after a frame is received.

Value	Description
0-255	The received character must be higher or equal to the value of VAL1 and lower or equal to VAL2 to set CMP flag in UART_SR. If asynchronous partial wake-up (SleepWalking) is enabled in PMC_SLPWK_ER, the UART requests a system wake-up if the condition is met.

Bit 25 – CRX_PE Control Rx Protocol Error Enable

Value	Description
1	A ProtocolError detected on a control Rx channel causes the appropriate channel bit in the MLB_MS0 or MLB_MS1 registers to be set.

Bit 24 – CRX_DONE Control Rx Packet Done Enable

Value	Description
1	A packet received with no errors on a control Rx channel causes the appropriate channel bit in the MLB_MS0 or MLB_MS1 registers to be set.

Bit 22 – ATX_BREAK Asynchronous Tx Break Enable

Value	Description
1	A ReceiverBreak response received from the receiver on an asynchronous Tx channel causes the appropriate channel bit in the MLB_MS0 or MLB_MS1 registers to be set.

Bit 21 – ATX_PE Asynchronous Tx Protocol Error Enable

Value	Description
1	A ProtocolError generated by the receiver on an asynchronous Tx channel causes the appropriate channel bit in the MLB_MS0 or MLB_MS1 registers to be set.

Bit 20 – ATX_DONE Asynchronous Tx Packet Done Enable
Tx channel causes the appropriate channel bit in the MLB_MS0 or MLB_MS1 registers to be set.

Value	Description
1	A packet transmitted with no errors on an asynchronous

Bit 19 – ARX_BREAK Asynchronous Rx Break Enable

Value	Description
1	A AsyncBreak command received from the transmitter on an asynchronous Rx channel causes the appropriate channel bit in the MLB_MS0 or MLB_MS1 registers to be set.

Bit 18 – ARX_PE Asynchronous Rx Protocol Error Enable

Value	Description
1	A ProtocolError detected on an asynchronous Rx channel causes the appropriate channel bit in the MLB_MS0 or MLB_MS1 registers to be set.

Bit 17 – ARX_DONE Asynchronous Rx Done Enable

Value	Description
1	A packet received with no errors on an asynchronous Rx channel causes the appropriate channel bit in the MLB_MS0 or MLB_MS1 registers to be set.

Bit 16 – SYNC_PE Synchronous Protocol Error Enable

Value	Description
1	A ProtocolError detected on a synchronous Rx channel causes the appropriate channel bit in the MLB_MS0 or MLB_MS1 registers to be set.

51. Pulse Width Modulation Controller (PWM)

51.1 Description

The Pulse Width Modulation Controller (PWM) generates output pulses on 4 channels independently according to parameters defined per channel. Each channel controls two complementary square output waveforms. Characteristics of the output waveforms such as period, duty-cycle, polarity and dead-times (also called dead-bands or non-overlapping times) are configured through the user interface. Each channel selects and uses one of the clocks provided by the clock generator. The clock generator provides several clocks resulting from the division of the PWM peripheral clock. External triggers can be managed to allow output pulses to be modified in real time.

All accesses to the PWM are made through registers mapped on the peripheral bus. All channels integrate a double buffering system in order to prevent an unexpected output waveform while modifying the period, the spread spectrum, the duty-cycle or the dead-times.

Channels can be linked together as synchronous channels to be able to update their duty-cycle or dead-times at the same time.

The update of duty-cycles of synchronous channels can be performed by the DMA Controller channel which offers buffer transfer without processor Intervention.

The PWM includes a spread-spectrum counter to allow a constantly varying period (only for Channel 0). This counter may be useful to minimize electromagnetic interference or to reduce the acoustic noise of a PWM driven motor.

The PWM provides 8 independent comparison units capable of comparing a programmed value to the counter of the synchronous channels (counter of channel 0). These comparisons are intended to generate software interrupts, to trigger pulses on the 2 independent event lines (in order to synchronize ADC conversions with a lot of flexibility independently of the PWM outputs) and to trigger DMA Controller transfer requests.

PWM outputs can be overridden synchronously or asynchronously to their channel counter.

The PWM provides a fault protection mechanism with 8 fault inputs, capable to detect a fault condition and to override the PWM outputs asynchronously (outputs forced to ‘0’, ‘1’ or Hi-Z).

For safety usage, some configuration registers are write-protected.

51.2 Embedded Characteristics

- 4 Channels
- Common Clock Generator Providing Thirteen Different Clocks
  - A Modulo n Counter Providing Eleven Clocks
  - Two Independent Linear Dividers Working on Modulo n Counter Outputs
- Independent Channels
  - Independent 16-bit Counter for Each Channel
  - Independent Complementary Outputs with 12-bit Dead-Time Generator (Also Called Dead-Band or Non-Overlapping Time) for Each Channel
  - Independent Push-Pull Mode for Each Channel
  - Independent Enable Disable Command for Each Channel

56. True Random Number Generator (TRNG)

56.1 Description

The True Random Number Generator (TRNG) passes the American *NIST Special Publication 800-22 (A Statistical Test Suite for Random and Pseudorandom Number Generators for Cryptographic Applications) and the Diehard Suite of Tests.*

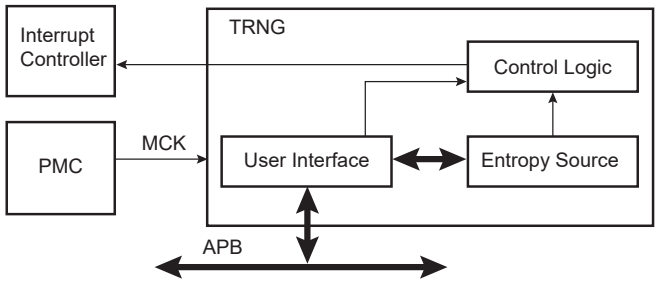
The TRNG may be used as an entropy source for seeding an NIST approved DRNG (Deterministic RNG) as required by FIPS PUB 140-2 and 140-3.

56.2 Embedded Characteristics

- Passes *NIST Special Publication 800-22 Test Suite*
- Passes *Diehard Suite of Tests*
- May be Used as Entropy Source for seeding a NIST-approved DRNG (Deterministic RNG) as required by FIPS PUB 140-2 and 140-3
- Provides a 32-bit Random Number Every 84 Clock Cycles

56.3 Block Diagram

Figure 56-1. TRNG Block Diagram



56.4 Product Dependencies

56.4.1 Power Management

The TRNG interface may be clocked through the Power Management Controller (PMC), thus the programmer must first configure the PMC to enable the TRNG user interface clock. The user interface clock is independent from any clock that may be used in the entropy source logic circuitry. The source of entropy can be enabled before enabling the user interface clock.

56.4.2 Interrupt Sources

The TRNG interface has an interrupt line connected to the Interrupt Controller. In order to handle interrupts, the Interrupt Controller must be programmed before configuring the TRNG.

Symbol	Parameter	Conditions			Min	Max	Unit
		Load	V_{DDIO}	Drive Level			
				High	–	55	
$PulseminH_1$	Pin Group 1 (1) High Level Pulse Width	10 pF	3.0V	High	6.1	9.2	ns
$PulseminL_1$	Pin Group 1 (1) Low Level Pulse Width	10 pF	3.0V	High	6.1	9.2	ns
FreqMax2	Pin Group 2 (2)Maximum output frequency	10 pF	3.0V	High	–	125	MHz
				Low	–	100	
$PulseminH_2$	Pin Group 2 (2) High Level Pulse Width	10 pF	3.0V	High	3.4	4.1	ns
$PulseminL_2$	Pin Group 2 (2) Low Level Pulse Width	10 pF	3.0V	High	3.4	4.1	ns
FreqMax3	Pin Group3(3) Maximum output frequency	30 pF	3.0V	High	–	75	MHz
				Low	–	50	
$PulseminH_3$	Pin Group 3 (3) High Level Pulse Width	30 pF	3.0V	High	6.0	7.3	ns
$PulseminL_3$	Pin Group 3 (3) Low Level Pulse Width	30 pF		High	6.0	7.3	ns
FreqMax4	Pin Group 4(4) Maximum output frequency	40 pF	3.0V	–	–	51	MHz
$PulseminH_4$	Pin Group 4(4) High Level Pulse Width	40 pF	3.0V	–	7.8	11.2	ns
$PulseminL_4$	Pin Group 4(4) Low Level Pulse Width	40 pF	3.0V	–	7.8	11.2	ns

Note:

1. Pin Group 1 = GPIO, CLOCK
2. Pin Group 2 = GPIO_CLK
3. Pin Group 3 = GPIO_AD
4. Pin Group 4 = GPIO_MLB

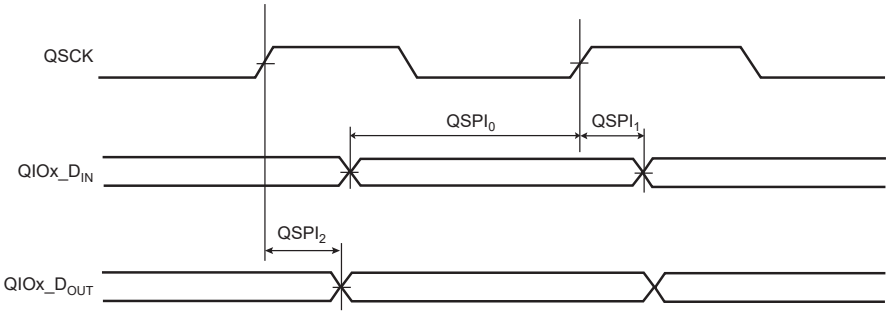
58.13.1.4 MediaLB Characteristics

The system has been constrained to achieve the timings in 256×Fs and 512×Fs in compliance with the MediaLB (MLB) specification.

Note: 1024×Fs timings are achieved under STH conditions only.

58.13.1.5 QSPI Characteristics

Figure 58-17. QSPI Master Mode with (CPOL= NCPHA = 0) or (CPOL= NCPHA= 1)



Symbol	Parameter	Condition	Min	Max	Unit
SSC_3	TF hold time after TK edge (TK output)	–	0	–	ns
SSC_4	TK edge to TF/TD (TK output, TF input)	–	-5.7[(1)]	3.1[(1)]	ns
		STTDLY = 0 START = 4, 5 or 7	-5.7 + (2 × t_{CPMCK})[(1)]	3.1 + (2 × t_{CPMCK})[(1)]	
SSC_5	TF setup time before TK edge (TK input)	–	0	–	ns
SSC_6	TF hold time after TK edge (TK input)	–	t_{CPMCK}	–	ns
SSC_7	TK edge to TF/TD (TK input, TF input)	–	3.6[(1)]	14.7[(1)]	ns
		STTDLY = 0 START = 4, 5 or 7	3.6 + (3 × t_{CPMCK})[(1)]	14.7 + (3 × t_{CPMCK})[(1)]	
Receiver					
SSC_8	RF/RD setup time before RK edge (RK input)	–	0	–	ns
SSC_9	RF/RD hold time after RK edge (RK input)	–	t_{CPMCK}	–	ns
SSC_{10}	RK edge to RF (RK input)	–	3.5[(1)]	12.1[(1)]	ns
SSC_{11}	RF/RD setup time before RK edge (RK output)	–	13.5 - t_{CPMCK}	–	ns
SSC_{12}	RF/RD hold time after RK edge (RK output)	–	t_{CPMCK} - 2.9	–	ns
SSC_{13}	RK edge to RF (RK output)	–	-2.8[(1)]	2.6[(1)]	ns

Note: Note: 1. For output signals (TF, TD, RF), min and max access times are defined. The min access time is the time between the TK (or RK) edge and the signal change. The max access timing is the time between the TK edge and the signal stabilization. The figure below illustrates min and max accesses for SSC0. The same applies for SSC1, SSC4, and SSC7, SSC10 and SSC13.

Date	Comments
	Section 46.6.3.11 “Receiver Timeout”: deleted redundant paragraphs on STTTO and RETTO. Section 46.6.4 “ISO7816 Mode”: corrected USART_MODE value for prototcol T = 1. Section 46.6.10 “LON Mode”: added information on node-to-node communication. Section 46.7.3 “USART Mode Register”: updated USART_MODE description to include LIN mode support.
cont’d	
01-June-16	Section 49. “Controller Area Network (MCAN)” Throughout: Renamed Fast Bit TIming and Prescaler Register to Data Bit TIming and Prescaler Register (MCAN_DBTP). Renamed field FBRP to DBRP and updated description. Updated descriptions of DSJW, DTSEG2 and DTSEG1. Added Section 49.4.5 “Timestamping”. Changed ‘Baud’ to ‘Bit’ in: - Section 49.5.3 “Timeout Counter”: in ‘Note’. - Section 49.6.4 “MCAN Data Bit Timing and Prescaler Register”: DBRP field description. - Section 49.6.8 “MCAN Nominal Bit Timing and Prescaler Register” NBRP field description. Updated Section 49.5.1.3 “CAN FD Operation”. Renamed section Transceiver Delay Compensation to Transmitter Delay Compensation (Section 49.5.1.4). Changed NTSEG1 to TSEG1. Updated content. Section 49.5.1.5 “Restricted Operation Mode”: added ‘Note’. Updated Figure 49-5 “Standard Message ID Filter Path” and Figure 49-6 “Extended Message ID Filter Path”. Section 49.6.7 “MCAN CC Control Register”: added bit NISO. Updated descriptions of FDOE, BRSE, PXHD and EFBI. Section 49.6.9 “MCAN Timestamp Counter Configuration Register”: updated TSS description. Section 49.6.10 “MCAN Timestamp Counter Value Register”: updated TSC description. Section 49.6.20 “MCAN Global Filter Configuration”: added some details on register description. Updated ANFE and ANFS field descriptions. Section 49.6.21 “MCAN Standard ID Filter Configuration” and Section 49.6.22 “MCAN Extended ID Filter Configuration”: added some details on register description. Section 49.6.24 “MCAN High Priority Message Status”: updated MSI description for value ‘1’.
	Section 50. “Timer Counter (TC)” Throughout: Replaced TIOA, TIOB, TCLK with TIOAx, TIOBx, TCLKx. Reformatted and renamed Table 50-2 “Channel Signal Description”.