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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M7 |
| Core Size | 32-Bit Single-Core |
| Speed | 300MHz |
| Connectivity | I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 75 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 384K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.08V ~ 3.6V |
| Data Converters | A/D 10x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsams70n20b-ant |

**Low-Power Features**

- Low-power Sleep, Wait and Backup modes, with typical power consumption down to 1.1 µA in Backup mode with RTC, RTT and wakeup logic enabled
- Ultra low-power RTC and RTT
- 1 Kbyte of backup RAM (BRAM) with dedicated regulator

**Peripherals**

- One Ethernet MAC (GMAC) 10/100 Mbps in MII mode and RMII with dedicated DMA. IEEE1588 PTP frames and 802.3az Energy-efficiency support. Ethernet AVB support with IEEE802.1AS Timestamping and IEEE802.1Qav credit-based traffic-shaping hardware support.
- USB 2.0 Device/Mini Host High-speed (USBHS) at 480 Mbps, 4-Kbyte FIFO, up to 10 bidirectional endpoints, dedicated DMA
- 12-bit ITU-R BT. 601/656 Image Sensor Interface (ISI)
- Two master Controller Area Networks (MCAN) with Flexible Data Rate (CAN-FD) with SRAM-based mailboxes, time- and event-triggered transmission
- MediaLB® device with 3-wire mode, up to 1024 x Fs speed, supporting MOST25 and MOST50 networks
- Three USARTs. USART0/1/2 support LIN mode, ISO7816, IrDA®, RS-485, SPI, Manchester and Modem modes; USART1 supports LON mode.
- Five 2-wire UARTs with SleepWalking™ support
- Three Two-Wire Interfaces (TWIHS) ($I^2C$-compatible) with SleepWalking support
- Quad I/O Serial Peripheral Interface (QSPI) interfacing up to 256 MB Flash and with eXecute-In-Place and on-the-fly scrambling
- Two Serial Peripheral Interfaces (SPI)
- One Serial Synchronous Controller (SSC) with $I^2S$ and TDM support
- Two Inter-IC Sound Controllers (I2SC)
- One High-speed Multimedia Card Interface (HSMCI) (SDIO/SD Card/e.MMC)
- Four Three-Channel 16-bit Timer/Counters (TC) with Capture, Waveform, Compare and PWM modes, constant on time. Quadrature decoder logic and 2-bit Gray Up/Down Counter for stepper motor
- Two 4-channel 16-bit PWMs with complementary outputs, Dead Time Generator and eight fault inputs per PWM for motor control, two external triggers to manage power factor correction (PFC), DC-DC and lighting control.
- Two Analog Front-End Controllers (AFEC), each supporting up to 12 channels with differential input mode and programmable gain stage, allowing dual sample-and-hold at up to 1.7 Msps. Offset and gain error correction feature.
- One 2-channel 12-bit 1 Msps-per-channel Digital-to-Analog Controller (DAC) with Differential and Over Sampling modes
- One Analog Comparator Controller (ACC) with flexible input selection, selectable input hysteresis

**Cryptography**

- True Random Number Generator (TRNG)
- AES: 256-, 192-, 128-bit Key Algorithm, Compliant with FIPS PUB-197 Specifications
- Integrity Check Monitor (ICM). Supports Secure Hash Algorithm SHA1, SHA224 and SHA256.

**I/O**

- Up to 114 I/O lines with external interrupt capability (edge- or level-sensitivity), debouncing, glitch filtering and On-die Series Resistor Termination
- Five Parallel Input/Output Controllers (PIO)

## 35.16 Register Summary

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | SMC_SETUP[0..3] | 7:0 | | | NWE_SETUP[5:0] | | | | | |
| | | 15:8 | | | NCS_WR_SETUP[5:0] | | | | | |
| | | 23:16 | | | NRD_SETUP[5:0] | | | | | |
| | | 31:24 | | | NCS_RD_SETUP[5:0] | | | | | |
| 0x00 | SMC_PULSE[0..3] | 7:0 | | NWE_PULSE[6:0] | | | | | | |
| | | 15:8 | | NCS_WR_PULSE[6:0] | | | | | | |
| | | 23:16 | | NRD_PULSE[6:0] | | | | | | |
| | | 31:24 | | NCS_RD_PULSE[6:0] | | | | | | |
| 0x00 | SMC_CYCLE[0..3] | 7:0 | NWE_CYCLE[7:0] | | | | | | | |
| | | 15:8 | | | | | | | | NWE_CYCLE[8:8] |
| | | 23:16 | NRD_CYCLE[7:0] | | | | | | | |
| | | 31:24 | | | | | | | | NRD_CYCLE[8:8] |
| 0x00 | SMC_MODE[0..3] | 7:0 | | | EXNW_MODE[1:0] | | | | WRITE_MODE | READ_MODE |
| | | 15:8 | | | | DBW | | | | BAT |
| | | 23:16 | | | | TDF_MODE | TDF_CYCLES[3:0] | | | |
| | | 31:24 | | | PS[1:0] | | | | | PMEN |
| 0x04 ... 0x7F | Reserved | | | | | | | | | |
| 0x80 | SMC_OCMS | 7:0 | | | | | | | | SMSE |
| | | 15:8 | | | | | CS3SE | CS2SE | CS1SE | CS0SE |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x84 | SMC_KEY1 | 7:0 | KEY1[7:0] | | | | | | | |
| | | 15:8 | KEY1[15:8] | | | | | | | |
| | | 23:16 | KEY1[23:16] | | | | | | | |
| | | 31:24 | KEY1[31:24] | | | | | | | |
| 0x88 | SMC_KEY2 | 7:0 | KEY2[7:0] | | | | | | | |
| | | 15:8 | KEY2[15:8] | | | | | | | |
| | | 23:16 | KEY2[23:16] | | | | | | | |
| | | 31:24 | KEY2[31:24] | | | | | | | |
| 0x8C ... 0xE3 | Reserved | | | | | | | | | |
| 0xE4 | SMC_WPMR | 7:0 | | | | | | | | WPEN |
| | | 15:8 | WPKEY[7:0] | | | | | | | |
| | | 23:16 | WPKEY[15:8] | | | | | | | |
| | | 31:24 | WPKEY[23:16] | | | | | | | |
| 0xE8 | SMC_WPSR | 7:0 | | | | | | | | WPVS |
| | | 15:8 | WPVSRC[7:0] | | | | | | | |

**Bits 23:0 – UBLEN[23:0]** Microblock Length
This field indicates the number of data in the microblock. The microblock contains UBLEN data.

## 36.7 XDMAC Maintenance Software Operations

### 36.7.1 Disabling a Channel

A disable channel request occurs when a write operation is performed in the XDMAC_GD register. If the channel is source peripheral synchronized (bit XDMAC_CCx.TYPE is set and bit XDMAC_CCx.DSYNC is cleared), then pending bytes (bytes located in the FIFO) are written to memory and bit XDMAC_CISx.DIS is set. If the channel is not source peripheral synchronized, the current channel transaction (read or write) is terminated and XDMAC_CISx.DIS is set. XDMAC_GS.STx is cleared by hardware when the current transfer is completed. The channel is no longer active and can be reused.

### 36.7.2 Suspending a Channel

A disable channel request occurs when a write operation is performed in the XDMAC_GD register. If the channel is source peripheral synchronized (bit XDMAC_CCx.TYPE is set and bit XDMAC_CCx.DSYNC is cleared), then pending bytes (bytes located in the FIFO) are written to memory and bit XDMAC_CISx.DIS is set. If the channel is not source peripheral synchronized, the current channel transaction (read or write) is terminated and XDMAC_CISx.DIS is set. XDMAC_GS.STx is cleared by hardware when the current transfer is completed. The channel is no longer active and can be reused.

### 36.7.3 Flushing a Channel

A FIFO flush command is issued by writing to the XDMAC_SWF register. The content of the FIFO is written to memory. XDMAC_CISx.FIS (End of Flush Interrupt Status bit) is set when the last byte is successfully transferred to memory. The channel is not disabled. The flush operation is not blocking, meaning that read operation can be scheduled during the flush write operation. The flush operation is only relevant for peripheral to memory transfer where pending peripheral bytes are buffered into the channel FIFO.

### 36.7.4 Maintenance Operation Priority

#### 36.7.4.1 Disable Operation Priority

- When a disable request occurs on a suspended channel, the XDMAC_GWS.WSx (Channel x Write Suspend bit) is cleared. If the transfer is source peripheral synchronized, the pending bytes are drained to memory. The bit XDMAC_CISx.DIS is set.
- When a disable request follows a flush request, if the flush last transaction is not yet scheduled, the flush request is discarded and the disable procedure is applied. Bit XDMAC_CISx.FIS is not set. Bit XDMAC_CISx.DIS is set when the disable request is completed. If the flush request transaction is already scheduled, the XDMAC_CISx.FIS is set. XDMAC_CISx.DIS is also set when the disable request is completed.

#### 36.7.4.2 Flush Operation Priority

- When a flush request occurs on a suspended channel, if there are pending bytes in the FIFO, they are written out to memory, XDMAC_CISx.FIS is set. If the FIFO is empty, XDMAC_CISx.FIS is also set.
- If the flush operation is performed after a disable request, the flush command is ignored. XDMAC_CISx.FIS is not set.

#### 36.7.4.3 Suspend Operation Priority

If the suspend operation is performed after a disable request, the write suspend operation is ignored.

will only begin to forward the packet to the AHB when enough packet data is stored in the packet buffer. The amount of packet data required to activate the forwarding process is programmable via watermark registers. These registers are located at the same address as the partial store and forward enable bits.
**Note:** The minimum operational value for the TX partial store and forward watermark is 20. There is no operational limit for the RX partial store and forward watermark.

Enabling Partial Store and Forward is a useful means to reduce latency, but there are performance implications. The GMAC DMA uses separate transmit and receive lists of buffer descriptors, with each descriptor describing a buffer area in memory. This allows Ethernet packets to be broken up and scattered around the AHB memory space.

#### 38.6.3.3 Receive AHB Buffers

Received frames, optionally including FCS, are written to receive AHB buffers stored in memory. The receive buffer depth is programmable in the range of 64 Bytes to 16 KBytes through the DMA Configuration register (GMAC_DCFGR), with the default being 128 Bytes.

The start location for each receive AHB buffer is stored in memory in a list of receive buffer descriptors at an address location pointed to by the receive buffer queue pointer. The base address for the receive buffer queue pointer is configured in software using the Receive Buffer Queue Base Address register (GMAC_RBQB).

Each list entry consists of two words. The first is the address of the receive AHB buffer and the second the receive status.

If the length of a receive frame exceeds the AHB buffer length, the status word for the used buffer is written with zeroes except for the “Start of Frame” bit, which is always set for the first buffer in a frame.

Bit zero of the address field is written to 1 to show that the buffer has been used. The receive buffer manager then reads the location of the next receive AHB buffer and fills that with the next part of the received frame data. AHB buffers are filled until the frame is complete and the final buffer descriptor status word contains the complete frame status. See the following table for details of the receive buffer descriptor list.

**Table 38-2. Receive Buffer Descriptor Entry**

| Bit | Function |
|---|---|
| Word 0 | |
| 31:2 | Address of beginning of buffer |
| 1 | Wrap—marks last descriptor in receive buffer descriptor list. |
| 0 | Ownership—needs to be zero for the GMAC to write data to the receive buffer. The GMAC sets this to one once it has successfully written a frame to memory.<br>Software has to clear this bit before the buffer can be used again. |
| Word 1 | |
| 31 | Global all ones broadcast address detected |
| 30 | Multicast hash match |
| 29 | Unicast hash match |
| 28 | – |

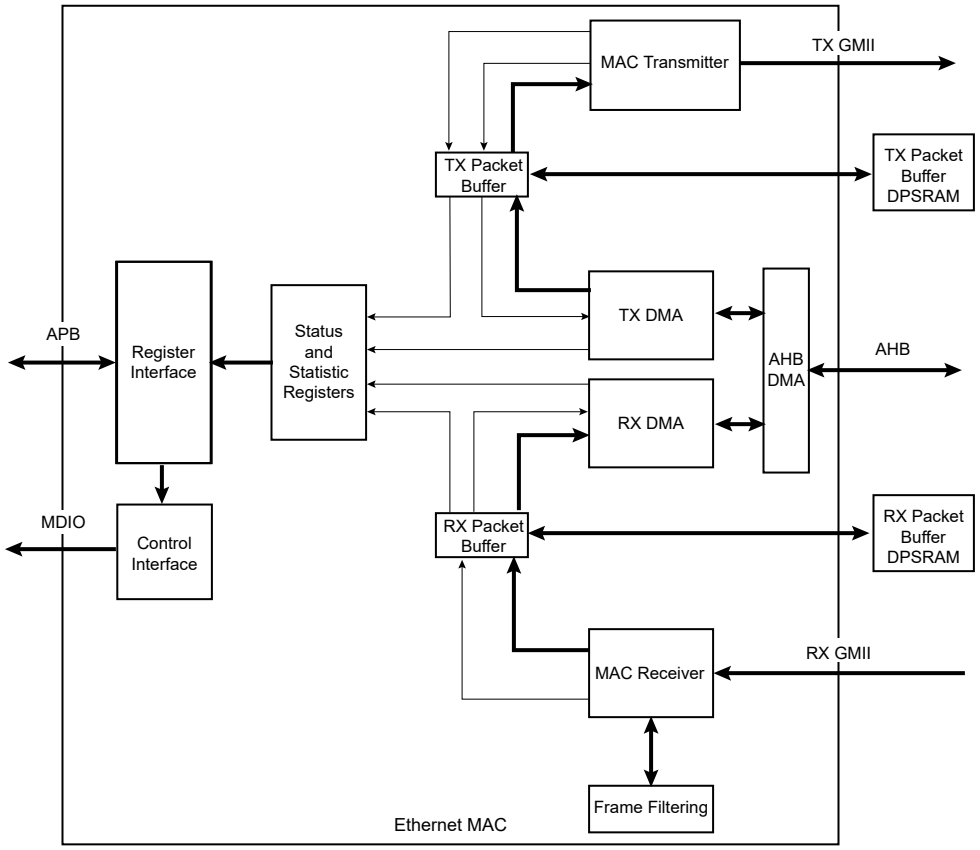
As described above, the DMA can be programmed into a low latency mode, known as Partial Store and Forward. For further details of this mode, see the related Links.

When the DMA is in full store and forward mode, full packets are buffered which provides the possibility to:

- Discard packets with error on the receive path before they are partially written out of the DMA, thus saving AHB bus bandwidth and driver processing overhead,
- Retry collided transmit frames from the buffer, thus saving AHB bus bandwidth,
- Implement transmit IP/TCP/UDP checksum generation offload.

With the packet buffers included, the structure of the GMAC data paths is shown in this image:

**Figure 38-2. Data Paths with Packet Buffers Included**




### 38.6.3.7 Transmit Packet Buffer

The transmitter packet buffer will continue attempting to fetch frame data from the AHB system memory until the packet buffer itself is full, at which point it will attempt to maintain its full level.

To accommodate the status and statistics associated with each frame, three words per packet (or two if the GMAC is configured in 64-bit data path mode) are reserved at the end of the packet data. If the packet is bad and requires to be dropped, the status and statistics are the only information held on that packet. Storing the status in the DPRAM is required in order to decouple the DMA interface of the buffer from the MAC interface, to update the MAC status/statistics and to generate interrupts in the order in which the packets that they represent were fetched from the AHB memory.

If any errors occur on the AHB while reading the transmit frame, the fetching of packet data from AHB memory is halted. The MAC transmitter will continue to fetch packet data, thereby emptying the packet

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0150 | GMAC_ORLO | 7:0 | RXO[7:0] | | | | | | | |
| | | 15:8 | RXO[15:8] | | | | | | | |
| | | 23:16 | RXO[23:16] | | | | | | | |
| | | 31:24 | RXO[31:24] | | | | | | | |
| 0x0154 | GMAC_ORHI | 7:0 | RXO[7:0] | | | | | | | |
| | | 15:8 | RXO[15:8] | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0158 | GMAC_FR | 7:0 | FRX[7:0] | | | | | | | |
| | | 15:8 | FRX[15:8] | | | | | | | |
| | | 23:16 | FRX[23:16] | | | | | | | |
| | | 31:24 | FRX[31:24] | | | | | | | |
| 0x015C | GMAC_BCFR | 7:0 | BFRX[7:0] | | | | | | | |
| | | 15:8 | BFRX[15:8] | | | | | | | |
| | | 23:16 | BFRX[23:16] | | | | | | | |
| | | 31:24 | BFRX[31:24] | | | | | | | |
| 0x0160 | GMAC_MFR | 7:0 | MFRX[7:0] | | | | | | | |
| | | 15:8 | MFRX[15:8] | | | | | | | |
| | | 23:16 | MFRX[23:16] | | | | | | | |
| | | 31:24 | MFRX[31:24] | | | | | | | |
| 0x0164 | GMAC_PFR | 7:0 | PFRX[7:0] | | | | | | | |
| | | 15:8 | PFRX[15:8] | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0168 | GMAC_BFR64 | 7:0 | NFRX[7:0] | | | | | | | |
| | | 15:8 | NFRX[15:8] | | | | | | | |
| | | 23:16 | NFRX[23:16] | | | | | | | |
| | | 31:24 | NFRX[31:24] | | | | | | | |
| 0x016C | GMAC_TBFR127 | 7:0 | NFRX[7:0] | | | | | | | |
| | | 15:8 | NFRX[15:8] | | | | | | | |
| | | 23:16 | NFRX[23:16] | | | | | | | |
| | | 31:24 | NFRX[31:24] | | | | | | | |
| 0x0170 | GMAC_TBFR255 | 7:0 | NFRX[7:0] | | | | | | | |
| | | 15:8 | NFRX[15:8] | | | | | | | |
| | | 23:16 | NFRX[23:16] | | | | | | | |
| | | 31:24 | NFRX[31:24] | | | | | | | |
| 0x0174 | GMAC_TBFR511 | 7:0 | NFRX[7:0] | | | | | | | |
| | | 15:8 | NFRX[15:8] | | | | | | | |
| | | 23:16 | NFRX[23:16] | | | | | | | |
| | | 31:24 | NFRX[31:24] | | | | | | | |
| 0x0178 | GMAC_TBFR1023 | 7:0 | NFRX[7:0] | | | | | | | |
| | | 15:8 | NFRX[15:8] | | | | | | | |
| | | 23:16 | NFRX[23:16] | | | | | | | |
| | | 31:24 | NFRX[31:24] | | | | | | | |
| 0x017C | GMAC_TBFR1518 | 7:0 | NFRX[7:0] | | | | | | | |
| | | 15:8 | NFRX[15:8] | | | | | | | |

- 10 Pipes/Endpoints
- 4096 bytes of Embedded Dual-Port RAM (DPRAM) for Pipes/Endpoints
- Up to 3 Memory Banks per Pipe/Endpoint (not for Control Pipe/Endpoint)
- Flexible Pipe/Endpoint Configuration and Management with Dedicated DMA Channels
- On-chip UTMI Transceiver including Pull-ups/Pull-downs

## 39.3 Block Diagram

The USBHS provides a hardware device to interface a USB link to a data flow stored in a dual-port RAM (DPRAM).

In normal operation (SPDCONF = 0), the UTMI transceiver requires the UTMI PLL (480 MHz). In case of full-speed or low-speed only, for a lower consumption (SPDCONF = 1), the UTMI transceiver only requires 48 MHz.

**Figure 39-1. USBHS Block Diagram**

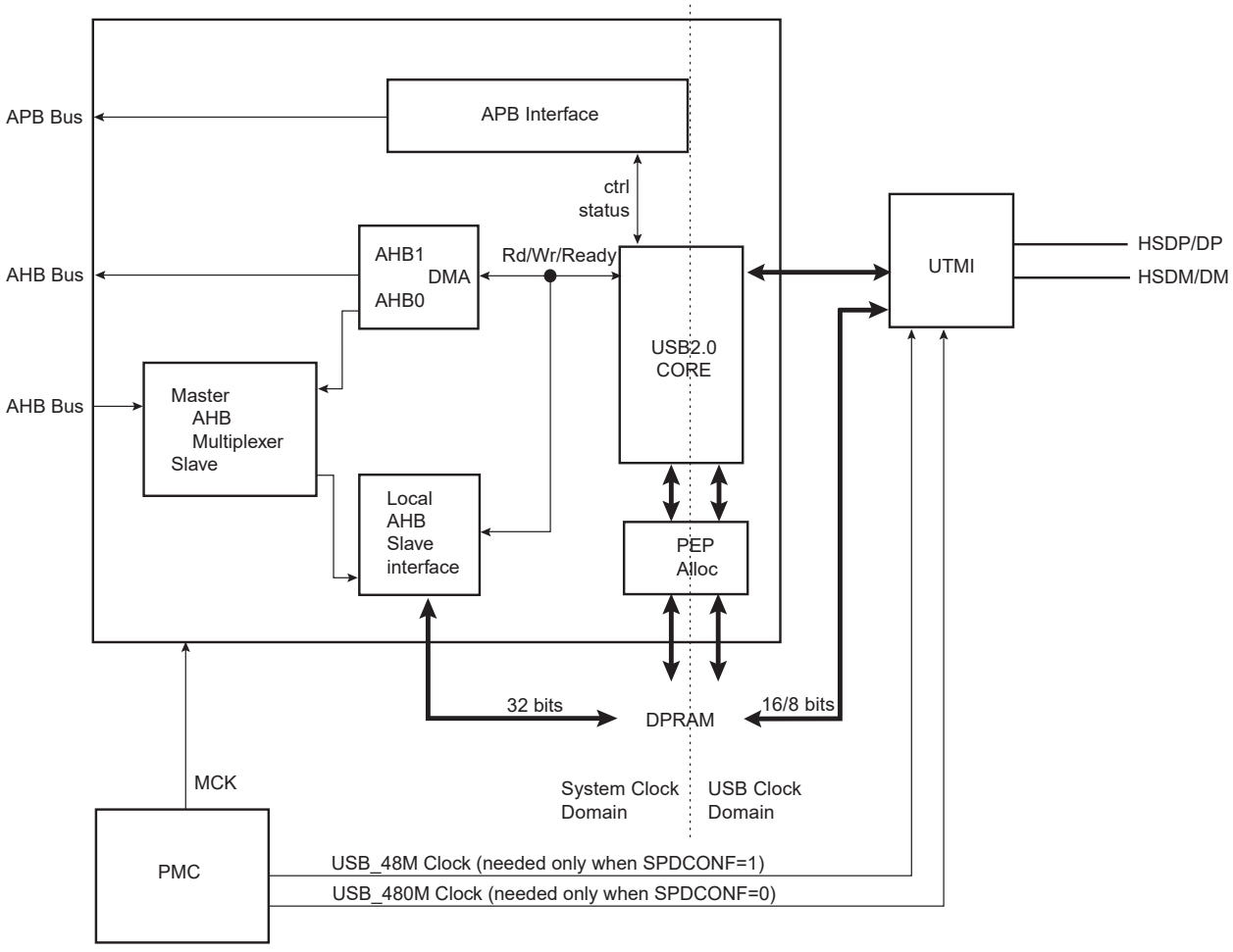
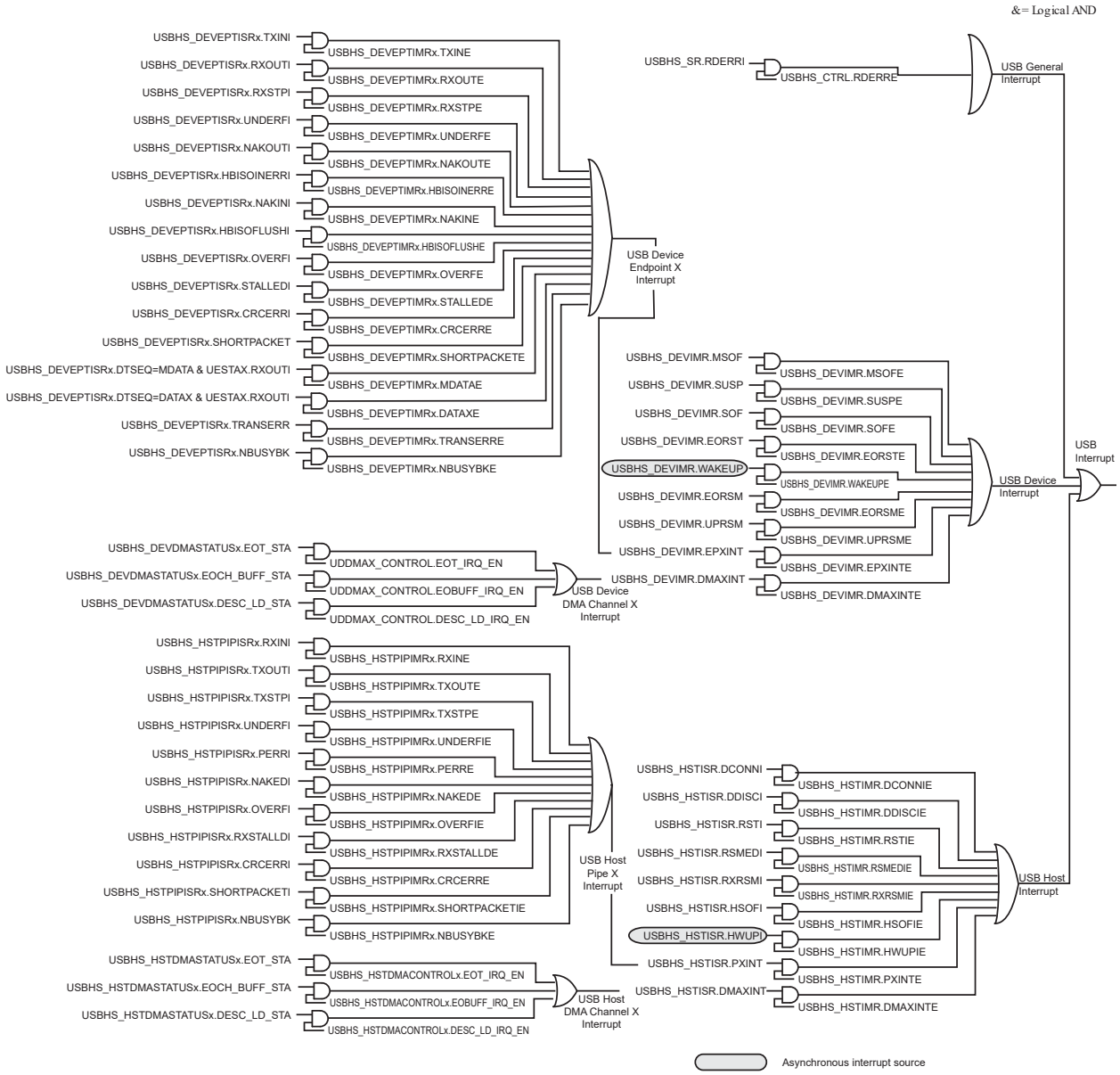


**Figure 39-3. Interrupt System**




See Interrupts in the Device Operation section and Interrupts in the Host Operation section for further details about device and host interrupts.

There are two kinds of general interrupts: processing, i.e., their generation is part of the normal processing, and exception, i.e., errors (not related to CPU exceptions).

### 39.5.1.3 MCU Power Modes

USB Suspend Mode

In Peripheral mode, the Suspend Interrupt bit in the Device Global Interrupt Status register (USBHS_DEVISR.SUSP) indicates that the USB line is in Suspend mode. In this case, the transceiver is automatically set in Suspend mode to reduce consumption.

Clock Frozen

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x0570 | USBHS_HSTPIPICR4 (INTPIPES) | 7:0 | SHORTPACKETIC | RXSTALLDIC | OVERFIC | NAKEDIC | | UNDERFIC | TXOUTIC | RXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0570 | USBHS_HSTPIPICR4 (ISOPIPES) | 7:0 | SHORTPACKETIC | CRCERRIC | OVERFIC | NAKEDIC | | UNDERFIC | TXOUTIC | RXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0574 | USBHS_HSTPIPICR5 | 7:0 | SHORTPACKETIC | RXSTALLDIC | OVERFIC | NAKEDIC | | TXSTPIC | TXOUTIC | RXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0574 | USBHS_HSTPIPICR5 (INTPIPES) | 7:0 | SHORTPACKETIC | RXSTALLDIC | OVERFIC | NAKEDIC | | UNDERFIC | TXOUTIC | RXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0574 | USBHS_HSTPIPICR5 (ISOPIPES) | 7:0 | SHORTPACKETIC | CRCERRIC | OVERFIC | NAKEDIC | | UNDERFIC | TXOUTIC | RXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0578 | USBHS_HSTPIPICR6 | 7:0 | SHORTPACKETIC | RXSTALLDIC | OVERFIC | NAKEDIC | | TXSTPIC | TXOUTIC | RXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0578 | USBHS_HSTPIPICR6 (INTPIPES) | 7:0 | SHORTPACKETIC | RXSTALLDIC | OVERFIC | NAKEDIC | | UNDERFIC | TXOUTIC | RXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x0578 | USBHS_HSTPIPICR6 (ISOPIPES) | 7:0 | SHORTPACKETIC | CRCERRIC | OVERFIC | NAKEDIC | | UNDERFIC | TXOUTIC | RXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x057C | USBHS_HSTPIPICR7 | 7:0 | SHORTPACKETIC | RXSTALLDIC | OVERFIC | NAKEDIC | | TXSTPIC | TXOUTIC | RXINIC |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 31:24 | | | | | | | | |
| 0x06A4 | USBHS_HSTPIPERR9 | 7:0 | | COUNTER[1:0] | | CRC16 | TIMEOUT | PID | DATAPID | DATATGL |
| | | 15:8 | | | | | | | | |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x06A8 ... 0x06FF | Reserved | | | | | | | | | |
| 0x0700 | USBHS_HSTDMANXTDSC1 | 7:0 | NXT_DSC_ADD[7:0] | | | | | | | |
| | | 15:8 | NXT_DSC_ADD[15:8] | | | | | | | |
| | | 23:16 | NXT_DSC_ADD[23:16] | | | | | | | |
| | | 31:24 | NXT_DSC_ADD[31:24] | | | | | | | |
| 0x0704 | USBHS_HSTDMAADDRESSx | 7:0 | BUFF_ADD[7:0] | | | | | | | |
| | | 15:8 | BUFF_ADD[15:8] | | | | | | | |
| | | 23:16 | BUFF_ADD[23:16] | | | | | | | |
| | | 31:24 | BUFF_ADD[31:24] | | | | | | | |
| 0x0708 | USBHS_HSTDMACONTROLx | 7:0 | BURST_LCK | DESC_LD_IT | END_BUFFIT | END_TR_IT | END_B_EN | END_TR_EN | LDNXT_DSC | CHANN_ENB |
| | | 15:8 | | | | | | | | |
| | | 23:16 | BUFF_LENGTH[7:0] | | | | | | | |
| | | 31:24 | BUFF_LENGTH[15:8] | | | | | | | |
| 0x070C | USBHS_HSTDMASTATUSx | 7:0 | | DESC_LDST | END_BF_ST | END_TR_ST | | | CHANN_ACT | CHANN_ENB |
| | | 15:8 | | | | | | | | |
| | | 23:16 | BUFF_COUNT[7:0] | | | | | | | |
| | | 31:24 | BUFF_COUNT[15:8] | | | | | | | |
| 0x0710 | USBHS_HSTDMANXTDSC2 | 7:0 | NXT_DSC_ADD[7:0] | | | | | | | |
| | | 15:8 | NXT_DSC_ADD[15:8] | | | | | | | |
| | | 23:16 | NXT_DSC_ADD[23:16] | | | | | | | |
| | | 31:24 | NXT_DSC_ADD[31:24] | | | | | | | |
| 0x0714 | USBHS_HSTDMAADDRESSx | 7:0 | BUFF_ADD[7:0] | | | | | | | |
| | | 15:8 | BUFF_ADD[15:8] | | | | | | | |
| | | 23:16 | BUFF_ADD[23:16] | | | | | | | |
| | | 31:24 | BUFF_ADD[31:24] | | | | | | | |
| 0x0718 | USBHS_HSTDMACONTROLx | 7:0 | BURST_LCK | DESC_LD_IT | END_BUFFIT | END_TR_IT | END_B_EN | END_TR_EN | LDNXT_DSC | CHANN_ENB |
| | | 15:8 | | | | | | | | |
| | | 23:16 | BUFF_LENGTH[7:0] | | | | | | | |
| | | 31:24 | BUFF_LENGTH[15:8] | | | | | | | |
| 0x071C | USBHS_HSTDMASTATUSx | 7:0 | | DESC_LDST | END_BF_ST | END_TR_ST | | | CHANN_ACT | CHANN_ENB |
| | | 15:8 | | | | | | | | |
| | | 23:16 | BUFF_COUNT[7:0] | | | | | | | |
| | | 31:24 | BUFF_COUNT[15:8] | | | | | | | |
| 0x0720 | USBHS_HSTDMANXTDSC3 | 7:0 | NXT_DSC_ADD[7:0] | | | | | | | |
| | | 15:8 | NXT_DSC_ADD[15:8] | | | | | | | |
| | | 23:16 | NXT_DSC_ADD[23:16] | | | | | | | |
| | | 31:24 | NXT_DSC_ADD[31:24] | | | | | | | |
| 0x0724 | USBHS_HSTDMAADDRESSx | 7:0 | BUFF_ADD[7:0] | | | | | | | |
| | | 15:8 | BUFF_ADD[15:8] | | | | | | | |

### 39.6.40 Host Address 2 Register

**Name:** USBHS_HSTADDR2
**Offset:** 0x0428
**Reset:** 0x00000000
**Property:** Read/Write

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | HSTADDRP7[6:0] | | | | | | |
| Access | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | HSTADDRP6[6:0] | | | | | | |
| Access | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | | HSTADDRP5[6:0] | | | | | | |
| Access | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | | HSTADDRP4[6:0] | | | | | | |
| Access | | | | | | | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 30:24 – HSTADDRP7[6:0]** USB Host Address
This field contains the address of the Pipe7 of the USB device.

This field is cleared when a USB reset is requested.

**Bits 22:16 – HSTADDRP6[6:0]** USB Host Address
This field contains the address of the Pipe6 of the USB device.

This field is cleared when a USB reset is requested.

**Bits 14:8 – HSTADDRP5[6:0]** USB Host Address
This field contains the address of the Pipe5 of the USB device.

This field is cleared when a USB reset is requested.

**Bits 6:0 – HSTADDRP4[6:0]** USB Host Address
This field contains the address of the Pipe4 of the USB device.

This field is cleared when a USB reset is requested.

| Offset | Name | Bit Pos. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x30 | HSMCI_RDR | 7:0 | DATA[7:0] | | | | | | | |
| | | 15:8 | DATA[15:8] | | | | | | | |
| | | 23:16 | DATA[23:16] | | | | | | | |
| | | 31:24 | DATA[31:24] | | | | | | | |
| 0x34 | HSMCI_TDR | 7:0 | DATA[7:0] | | | | | | | |
| | | 15:8 | DATA[15:8] | | | | | | | |
| | | 23:16 | DATA[23:16] | | | | | | | |
| | | 31:24 | DATA[31:24] | | | | | | | |
| 0x38 ... 0x3F | Reserved | | | | | | | | | |
| 0x40 | HSMCI_SR | 7:0 | | | NOTBUSY | DTIP | BLKE | TXRDY | RXRDY | CMDRDY |
| | | 15:8 | | | CSRCV | SDIOWAIT | | | | SDIOIRQA |
| | | 23:16 | CSTOE | DTOE | DCRCE | RTOE | RENDE | RCRCE | RDIRE | RINDE |
| | | 31:24 | UNRE | OVRE | ACKRCVE | ACKRCV | XFRDONE | FIFOEMPTY | | BLKOVRE |
| 0x44 | HSMCI_IER | 7:0 | | | NOTBUSY | DTIP | BLKE | TXRDY | RXRDY | CMDRDY |
| | | 15:8 | | | CSRCV | SDIOWAIT | | | | SDIOIRQA |
| | | 23:16 | CSTOE | DTOE | DCRCE | RTOE | RENDE | RCRCE | RDIRE | RINDE |
| | | 31:24 | UNRE | OVRE | ACKRCVE | ACKRCV | XFRDONE | FIFOEMPTY | | BLKOVRE |
| 0x48 | HSMCI_IDR | 7:0 | | | NOTBUSY | DTIP | BLKE | TXRDY | RXRDY | CMDRDY |
| | | 15:8 | | | CSRCV | SDIOWAIT | | | | SDIOIRQA |
| | | 23:16 | CSTOE | DTOE | DCRCE | RTOE | RENDE | RCRCE | RDIRE | RINDE |
| | | 31:24 | UNRE | OVRE | ACKRCVE | ACKRCV | XFRDONE | FIFOEMPTY | | BLKOVRE |
| 0x4C | HSMCI_IMR | 7:0 | | | NOTBUSY | DTIP | BLKE | TXRDY | RXRDY | CMDRDY |
| | | 15:8 | | | CSRCV | SDIOWAIT | | | | SDIOIRQA |
| | | 23:16 | CSTOE | DTOE | DCRCE | RTOE | RENDE | RCRCE | RDIRE | RINDE |
| | | 31:24 | UNRE | OVRE | ACKRCVE | ACKRCV | XFRDONE | FIFOEMPTY | | BLKOVRE |
| 0x50 | HSMCI_DMA | 7:0 | | CHKSIZE[2:0] | | | | | | |
| | | 15:8 | | | | | | | | DMAEN |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x54 | HSMCI_CFG | 7:0 | | | | FERRCTRL | | | | FIFOMODE |
| | | 15:8 | | | | LSYNC | | | | HSMODE |
| | | 23:16 | | | | | | | | |
| | | 31:24 | | | | | | | | |
| 0x58 ... 0xE3 | Reserved | | | | | | | | | |
| 0xE4 | HSMCI_WPMR | 7:0 | | | | | | | | WPEN |
| | | 15:8 | WPKEY[7:0] | | | | | | | |
| | | 23:16 | WPKEY[15:8] | | | | | | | |
| | | 31:24 | WPKEY[23:16] | | | | | | | |
| 0xE8 | HSMCI_WPSR | 7:0 | | | | | | | | WPVS |
| | | 15:8 | WPVSRC[7:0] | | | | | | | |
| | | 23:16 | WPVSRC[15:8] | | | | | | | |
| | | 31:24 | | | | | | | | |

1: A data or address byte has not been acknowledged by the slave component. Set at the same time as TXCOMP.

- NACK used in Slave Read mode:

0: Each data byte has been correctly received by the master.

1: In Read mode, a data byte has not been acknowledged by the master. When NACK is set, the user must not fill TWIHS_THR even if TXRDY is set, because it means that the master stops the data transfer or re-initiate it.

**Note:** In Slave Write mode, all data are acknowledged by the TWIHS.

**Bit 7 – UNRE** Underrun Error (cleared on read)
This bit is used only if clock stretching is disabled.

| Value | Description |
|---|---|
| 0 | TWIHS_THR has been filled on time. |
| 1 | TWIHS_THR has not been filled on time. |

**Bit 6 – OVRE** Overrun Error (cleared on read)
This bit is used only if clock stretching is disabled.

| Value | Description |
|---|---|
| 0 | TWIHS_RHR has not been loaded while RXRDY was set. |
| 1 | TWIHS_RHR has been loaded while RXRDY was set. Reset by read in TWIHS_SR when TXCOMP is set. |

**Bit 5 – GACC** General Call Access (cleared on read)
This bit is used in Slave mode only.

GACC behavior can be seen in Master Performs a General Call.

| Value | Description |
|---|---|
| 0 | No general call has been detected. |
| 1 | A general call has been detected. After the detection of general call, if need be, the user may acknowledge this access and decode the following bytes and respond according to the value of the bytes. |

**Bit 4 – SVACC** Slave Access
This bit is used in Slave mode only.

SVACC behavior can be seen in Read Access Ordered by a Master, Clock Stretching in Read Mode, Repeated Start and Reversal from Read Mode to Write Mode and Repeated Start and Reversal from Write Mode to Read Mode.

| Value | Description |
|---|---|
| 0 | TWIHS is not addressed. SVACC is automatically cleared after a NACK or a STOP condition is detected. |
| 1 | Indicates that the address decoding sequence has matched (A master has sent SADR). SVACC remains high until a NACK or a STOP condition is detected. |

### 47.6.8 UART Transmit Holding Register

**Name:** UART_THR
**Offset:** 0x1C
**Reset:** –
**Property:** Write-only

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TXCHR[7:0] | | | | | | | |
| Access | W | W | W | W | W | W | W | W |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | – |

**Bits 7:0 – TXCHR[7:0]** Character to be Transmitted
Next character to be transmitted after the current character if TXRDY is not set.

**Figure 48-8. Control Packet Tx Device Protocol: End**

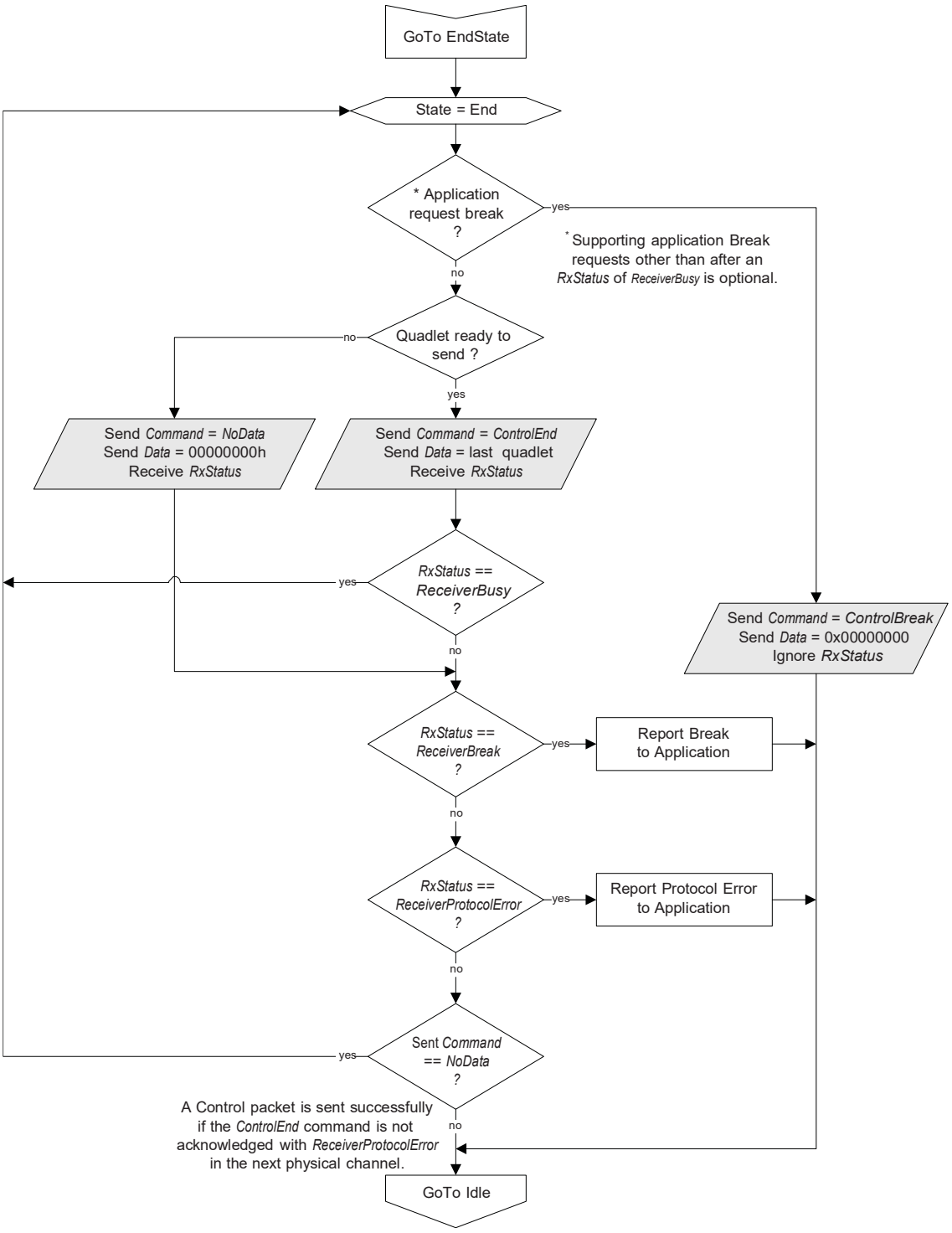
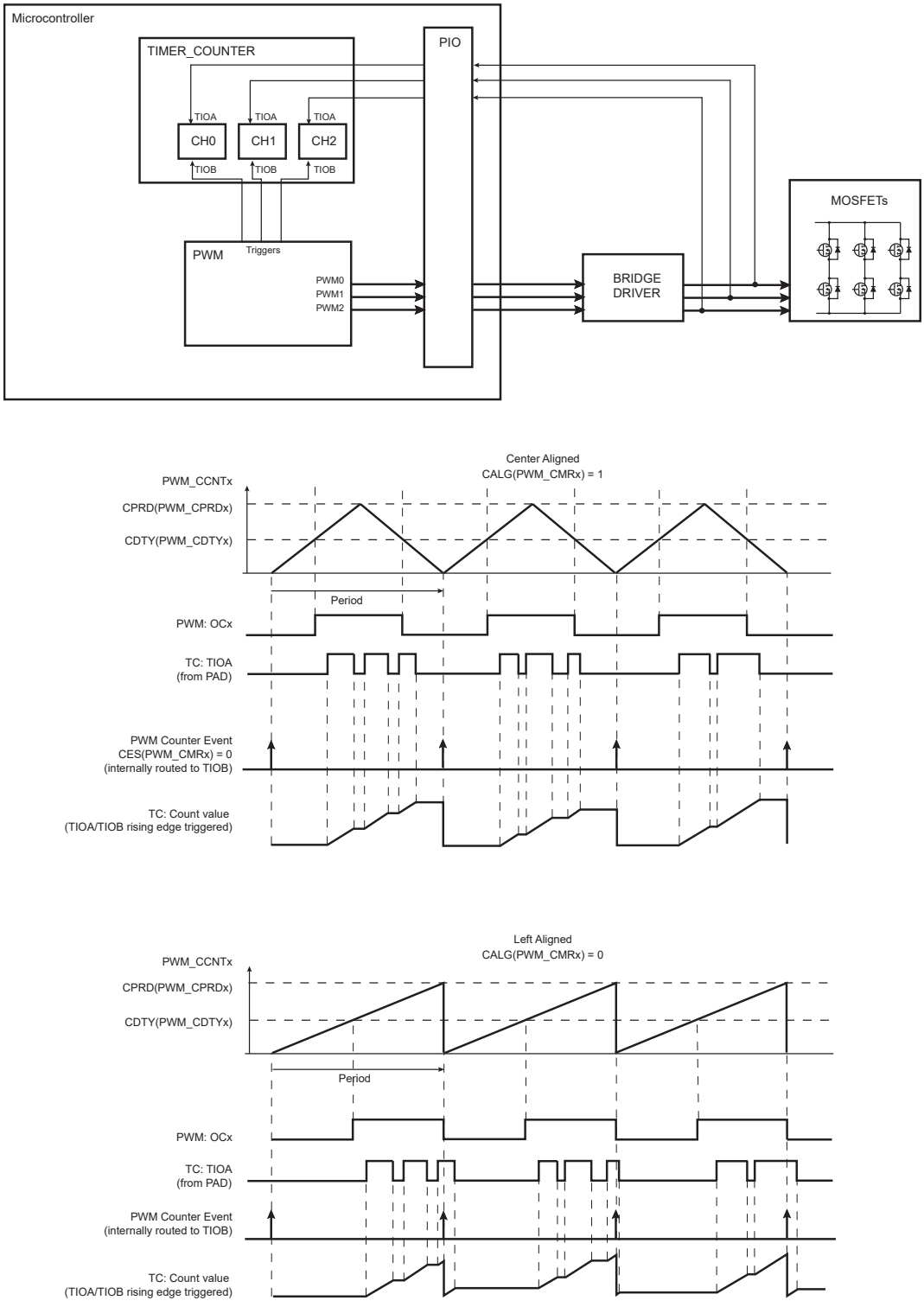


**Figure 51-7. Triggering the TC: Cumulated "ON" Time Measurement**




### 51.6.2.4 2-bit Gray Up/Down Counter for Stepper Motor

A pair of channels may provide a 2-bit gray count waveform on two outputs. Dead-time generator and other downstream logic can be configured on these channels.

Up or Down Count mode can be configured on-the-fly by means of PWM_SMMR configuration registers.

The AFEC can apply different gain and offset on each channel.

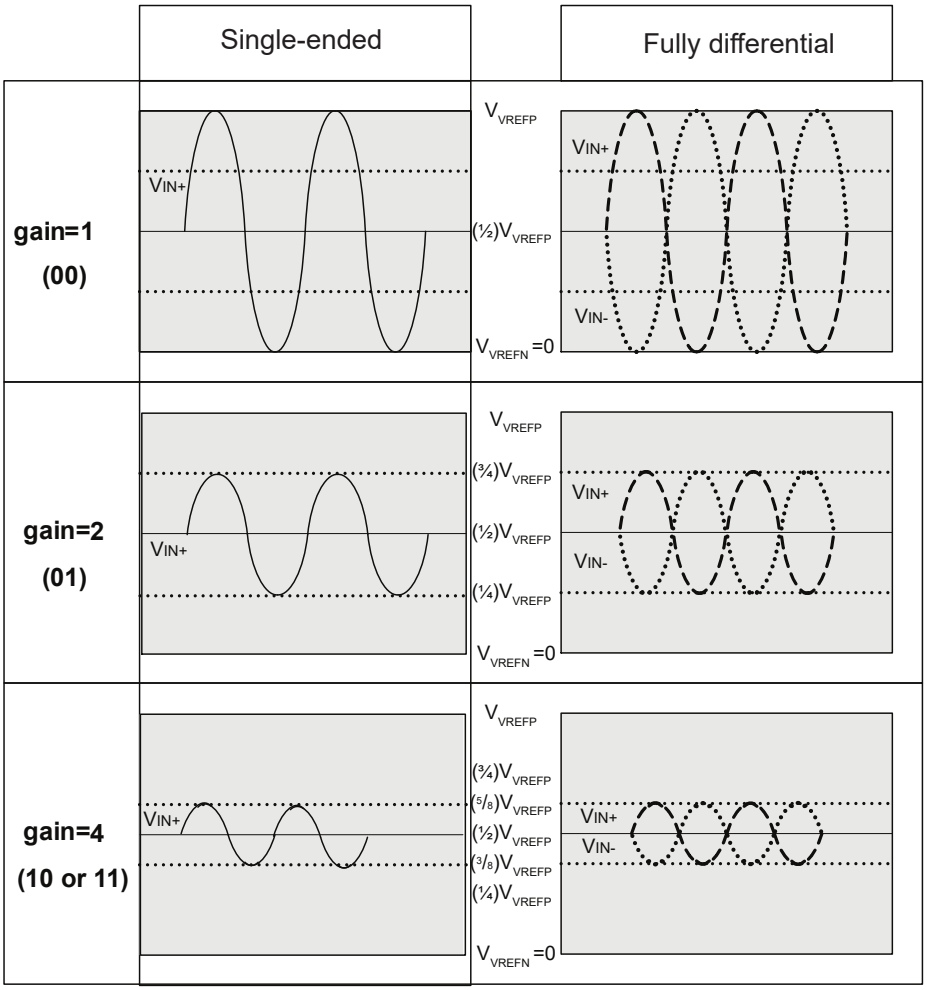
The gain is configured in the GAIN field of the Channel Gain Register (AFEC_CGR) as shown in the following table.

**Table 52-5. Gain of the Sample-and-Hold Unit**

| GAIN | GAIN (DIFFx = 0) | GAIN (DIFFx = 1) |
|---|---|---|
| 0 | 1 | 1 |
| 1 | 2 | 2 |
| 2 | 4 | 4 |
| 3 | 4 | 4 |

The analog offset of the AFE is configured in the AOFF field in the Channel Offset Compensation register (AFEC_COCR). The offset is only available in Single-ended mode. The field AOFF must be configured to 512 (mid scale of the DAC) when there is no offset error to compensate.To compensate for an offset error of n LSB (positive or negative), the field AOFF must be configured to 512 + n.

**Figure 52-7. Analog Full Scale Ranges in Single-Ended/Differential Applications Versus Gain**



### 52.7.14 AFEC Overrun Status Register

**Name:** AFEC_OVER
**Offset:** 0x4C
**Reset:** 0x00000000
**Property:** Read-only

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| Access | | | | | | | | |
| Reset | | | | | | | | |

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | | | | | OVRE11 | OVRE10 | OVRE9 | OVRE8 |
| Access | | | | | R | R | R | R |
| Reset | | | | | 0 | 0 | 0 | 0 |

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | OVRE7 | OVRE6 | OVRE5 | OVRE4 | OVRE3 | OVRE2 | OVRE1 | OVRE0 |
| Access | R | R | R | R | R | R | R | R |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 – OVREx** Overrun Error x
An overrun error does not always mean that the unread data has been replaced by a new valid data. See Enhanced Resolution Mode and Digital Averaging Function for details.

| Value | Description |
|---|---|
| 0 | No overrun error on the corresponding channel since the last read of AFEC_OVER. |
| 1 | There has been an overrun error on the corresponding channel since the last read of AFEC_OVER. |

| Value | Description |
|---|---|
| 0 | Automatic monitoring mode is disabled. |
| 1 | The ICM passes through the Main List once to calculate the message digest of the monitored area. When WRAP = 1 in ICM_RCFG, the ICM begins monitoring. |

**Bits 7:4 – BBC[3:0]** Bus Burden Control
This field is used to control the burden of the ICM system bus. The number of system clock cycles between the end of the current processing and the next block transfer is set to $2^{BBC}$. Up to 32,768 cycles can be inserted.

**Bit 2 – SLBDIS** Secondary List Branching Disable

| Value | Description |
|---|---|
| 0 | Branching to the Secondary List is permitted. |
| 1 | Branching to the Secondary List is forbidden. The NEXT field of the ICM_RNEXT structure member has no effect and is always considered as zero. |

**Bit 1 – EOMDIS** End of Monitoring Disable

| Value | Description |
|---|---|
| 0 | End of Monitoring is permitted. |
| 1 | End of Monitoring is forbidden. The EOM bit of the ICM_RCFG structure member has no effect. |

**Bit 0 – WBDIS** Write Back Disable
When ASCD is set, WBDIS has no effect.

| Value | Description |
|---|---|
| 0 | Write Back operations are permitted. |
| 1 | Write Back operations are forbidden. Context register CDWBN bit is internally set to one and cannot be modified by a linked list element. ICM_RCFG.CDWBN has no effect. |

# 58. Electrical Characteristics for SAM V70/V71

## 58.1 Absolute Maximum Ratings

**Table 58-1. Absolute Maximum Ratings***

| | |
|---|---|
| Storage Temperature -60°C to + 150°C<br>Voltage on Input Pins<br>with Respect to Ground -0.3V to + 4.0V<br>Maximum Operating Voltage<br>VDDPLL, VDDUTMIC, VDDCORE 1.4V<br>Maximum Operating Voltage<br>VDDIO, VDDUTMII, VDDPLLUSB, VDDIN 4.0V<br>Total DC Output Current on all I/O lines: 150 mA | *Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. |

**Table 58-2. Recommended Thermal Operating Conditions**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $T_A$ | Operating Temperature | – | -40 | – | 105 | °C |
| $T_J$ | Junction Temperature | – | -40 | – | 125 | °C |
| $R_{JA}$ | Junction-to-ambient Thermal Resistance | TFBGA144 | – | 45 | – | °C/W |
| | | LQFP144 | - | 36 | - | |
| | | TFBGA100 | – | 47 | – | |
| | | LQFP100 | – | 41 | – | |
| | | LQFP64 | – | 46 | – | |
| $P_D$ | Power Dissipation | At$T_A$= 85°C, TFBGA144 | – | – | – | mW |
| | | At$T_A$= 105°C TFBGA144 | – | – | 425 | |
| $P_D$ | Power Dissipation | At $T_A$ = 85°C,LQFP144 | – | – | 1047 | mW |
| | | At $T_A$ = 105°C,LQFP144 | – | – | 523 | mW |