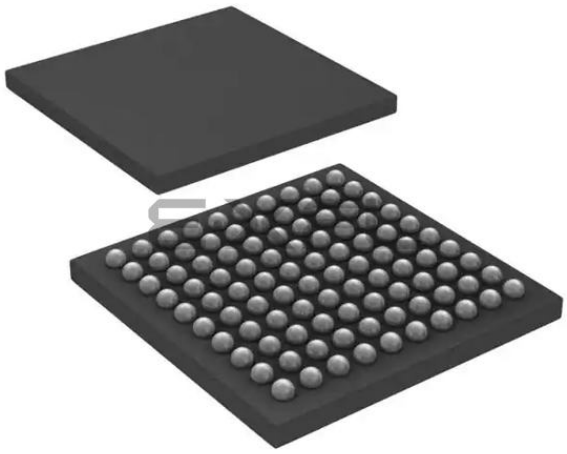


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70n20b-cfnt

23.5.3 Supply Controller Mode Register

Name: SUPC_MR
Offset: 0x08
Reset: 0x00005A00
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	KEY[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
				OSCBYPASS			BKUPRETON	
Access				R/W			R/W	
Reset				0			0	

Bit	15	14	13	12	11	10	9	8
		ONREG	BODDIS	BODRSTEN				
Access		R/W	R/W	R/W				
Reset		1	0	1				

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 31:24 – KEY[7:0] Password Key

Value	Name	Description
0xA5	PASSWD	Writing any other value in this field aborts the write operation.

Bit 20 – OSCBYPASS Oscillator Bypass
Note: This bit is located in the VDDIO domain.

Value	Description
0	(NO_EFFECT): No effect. Clock selection depends on the value of SUPC_CR.XTALSEL.
1	(BYPASS): The 32.768 kHz crystal oscillator is bypassed if SUPC_CR.XTALSEL is set. OSCBYPASS must be set prior to setting XTALSEL.

Bit 17 – BKUPRETON SRAM On In Backup Mode

Value	Description
0	SRAM (Backup) switched off in Backup mode.
1	SRAM (Backup) switched on in Backup mode. Note: This bit is located in the VDDIO domain.

Bit 14 – ONREG Voltage Regulator Enable
Note: This bit is located in the VDDIO domain.

Value	Name	Description
0	NO_TIMEVENT	No time event has occurred since the last clear.
1	TIMEVENT	At least one time event has occurred since the last clear.

Bit 2 – SEC Second Event

Value	Name	Description
0	NO_SECEVENT	No second event has occurred since the last clear.
1	SECEVENT	At least one second event has occurred since the last clear.

Bit 1 – ALARM Alarm Flag

Value	Name	Description
0	NO_ALARMEVENT	No alarm matching condition occurred.
1	ALARMEVENT	An alarm matching condition has occurred.

Bit 0 – ACKUPD Acknowledge for Update

Value	Name	Description
0	FREERUN	Time and calendar registers cannot be updated.
1	UPDATE	Time and calendar registers can be updated.

28.5.1 Real-time Timer Mode Register

Name: RTT_MR
Offset: 0x00
Reset: 0x00008000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
								RTC1HZ
Access								
Reset								0

Bit	23	22	21	20	19	18	17	16
				RTTDIS		RTTRST	RTTINCIEN	ALMIEN
Access						R/W	R/W	R/W
Reset				0		0	0	0

Bit	15	14	13	12	11	10	9	8
	RTPRES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RTPRES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 24 – RTC1HZ Real-Time Clock 1Hz Clock Selection

Value	Description
0	The RTT 32-bit counter is driven by the 16-bit prescaler roll-over events.
1	The RTT 32-bit counter is driven by the 1Hz RTC clock.

Bit 20 – RTTDIS Real-time Timer Disable

Value	Description
0	The RTT is enabled.
1	The RTT is disabled (no dynamic power consumption).

Bit 18 – RTTRST Real-time Timer Restart

Value	Description
0	No effect.
1	Reloads and restarts the clock divider with the new programmed value. This also resets the 32-bit counter.

Bit 17 – RTTINCIEN Real-time Timer Increment Interrupt Enable

Value	Name	Description
3	CLK_8	Selected clock divided by 8
4	CLK_16	Selected clock divided by 16
5	CLK_32	Selected clock divided by 32
6	CLK_64	Selected clock divided by 64
7	CLK_3	Selected clock divided by 3

Bits 1:0 – CSS[1:0] Master Clock Source Selection

Value	Name	Description
0	SLOW_CLK	SLCK is selected
1	MAIN_CLK	MAINCK is selected
2	PLLA_CLK	PLLACK is selected
3	UPLL_CLK	UPPLLCKDIV is selected

32.6.1.38 PIO Additional Interrupt Modes Mask Register

Name: PIO_AIMMR
Offset: 0x00B8
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO I/O Line Index
Selects the I/O event type triggering an interrupt.

Value	Description
0	The interrupt source is a both-edge detection event.
1	The interrupt source is described by the registers PIO_ELSR and PIO_FRLHSR.

32.6.1.51 PIO Parallel Capture Interrupt Enable Register

Name: PIO_PCIER
Offset: 0x0154
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect

1: Enables the corresponding interrupt

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access					RXBUFF	ENDRX	OVRE	DRDY
Reset								

Bit 3 – RXBUFF Reception Buffer Full Interrupt Enable

Bit 2 – ENDRX End of Reception Transfer Interrupt Enable

Bit 1 – OVRE Parallel Capture Mode Overrun Error Interrupt Enable

Bit 0 – DRDY Parallel Capture Mode Data Ready Interrupt Enable

Value	Description
0	TDF optimization disabled–the number of TDF wait states is inserted before the next access begins.
1	TDF optimization enabled–the number of TDF wait states is optimized using the setup period of the next read/write access.

Bits 19:16 – TDF_CYCLES[3:0] Data Float Time
This field gives the integer number of clock cycles required by the external device to release the data after the rising edge of the read controlling signal. The SMC always provide one full cycle of bus turnaround after the TDF_CYCLES period. The external bus cannot be used by another chip select during TDF_CYCLES + 1 cycles. From 0 up to 15 TDF_CYCLES can be set.

Bit 12 – DBW Data Bus Width

Value	Name	Description
0	8_BIT	8-bit Data Bus
1	16_BIT	16-bit Data Bus

Bit 8 – BAT Byte Access Type
This field is used only if DBW defines a 16-bit data bus.

Value	Name	Description
0	BYTE_SELECT	Byte select access type: - Write operation is controlled using NCS, NWE, NBS0, NBS1. - Read operation is controlled using NCS, NRD, NBS0, NBS1.
1	BYTE_WRITE	Byte write access type: - Write operation is controlled using NCS, NWR0, NWR1. - Read operation is controlled using NCS and NRD.

Bits 5:4 – EXNW_MODE[1:0] NWAIT Mode
The NWAIT signal is used to extend the current read or write signal. It is only taken into account during the pulse phase of the read and write controlling signal. When the use of NWAIT is enabled, at least one cycle hold duration must be programmed for the read and write controlling signal.

Value	Name	Description
0	DISABLED	Disabled–The NWAIT input signal is ignored on the corresponding chip select.
1	Reserved	
2	FROZEN	Frozen Mode–If asserted, the NWAIT signal freezes the current read or write cycle. After deassertion, the read/write cycle is resumed from the point where it was stopped.
3	READY	Ready Mode–The NWAIT signal indicates the availability of the external device at the end of the pulse of the controlling read or write signal, to complete the access. If high, the access normally completes. If low, the access is extended until NWAIT returns high.

Bit 1 – WRITE_MODE Write Mode

Value	Description
0	The write operation is controlled by the NCS signal.

Offset	Name	Bit Pos.								
		15:8								
		23:16								
		31:24								
0x98	XDMAC_CIM1	7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
		15:8								
		23:16								
		31:24								
0x9C	XDMAC_CIS1	7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
		15:8								
		23:16								
		31:24								
0xA0	XDMAC_CSA1	7:0	SA[7:0]							
		15:8	SA[15:8]							
		23:16	SA[23:16]							
		31:24	SA[31:24]							
0xA4	XDMAC_CDA1	7:0	DA[7:0]							
		15:8	DA[15:8]							
		23:16	DA[23:16]							
		31:24	DA[31:24]							
0xA8	XDMAC_CNDA1	7:0	NDA[5:0]							NDAIF
		15:8	NDA[13:6]							
		23:16	NDA[21:14]							
		31:24	NDA[29:22]							
0xAC	XDMAC_CNDC1	7:0				NDVIEW[1:0]		NDDUP	NDSUP	NDE
		15:8								
		23:16								
		31:24								
0xB0	XDMAC_CUBC1	7:0	UBLEN[7:0]							
		15:8	UBLEN[15:8]							
		23:16	UBLEN[23:16]							
		31:24								
0xB4	XDMAC_CBC1	7:0	BLEN[7:0]							
		15:8					BLEN[11:8]			
		23:16								
		31:24								
0xB8	XDMAC_CC1	7:0	MEMSET	SWREQ		DSYNC		MBSIZE[1:0]		TYPE
		15:8		DIF	SIF	DWIDTH[1:0]		CSIZE[2:0]		
		23:16	WRIP	RDIP	INITD		DAM[1:0]		SAM[1:0]	
		31:24		PERID[6:0]						
0xBC	XDMAC_CDS_MSP1	7:0	SDS_MSP[7:0]							
		15:8	SDS_MSP[15:8]							
		23:16	DDS_MSP[7:0]							
		31:24	DDS_MSP[15:8]							
0xC0	XDMAC_CSUS1	7:0	SUBS[7:0]							
		15:8	SUBS[15:8]							
		23:16	SUBS[23:16]							

buffer and allowing any good (non-erroneous) frames to be transmitted successfully. Once these have been fully transmitted, the status/statistics for the erroneous frame will be updated and software will be informed via an interrupt that an AHB error occurred. This way, the error is reported in the correct packet order.

The transmit packet buffer will only attempt to read more frame data from the AHB when space is available in the packet buffer memory. If space is not available it must wait until the a packet fetched by the MAC completes transmission and is subsequently removed from the packet buffer memory.
Note: If full store and forward mode is active and if a single frame is fetched that is too large for the packet buffer memory, the frame is flushed and the DMA halted with an error status. This is because a complete frame must be written into the packet buffer before transmission can begin, and therefore the minimum packet buffer memory size should be chosen to satisfy the maximum frame to be transmitted in the application.

In full store and forward mode, once the complete transmit frame is written into the packet buffer memory, a trigger is sent across to the MAC transmitter, which will then begin reading the frame from the packet buffer memory. Since the whole frame is present and stable in the packet buffer memory an underflow of the transmitter is not possible. The frame is kept in the packet buffer until notification is received from the MAC that the frame data has either been successfully transmitted or can no longer be retransmitted (too many retries in half duplex mode). When this notification is received the frame is flushed from memory to make room for a new frame to be fetched from AHB system memory.

In Partial Store and Forward mode, a trigger is sent across to the MAC transmitter as soon as sufficient packet data is available, which will then begin fetching the frame from the packet buffer memory. If, after this point, the MAC transmitter is able to fetch data from the packet buffer faster than the AHB DMA can fill it, an underflow of the transmitter is possible. In this case, the transmission is terminated early, and the packet buffer is completely flushed. Transmission can only be restarted by writing a '1' to the Transmit Start bit in the Network Control register (GMAC_NCR.TSTART).

In half duplex mode, the frame is kept in the packet buffer until notification is received from the MAC that the frame data has either been successfully transmitted or can no longer be retransmitted (too many retries in half duplex mode). When this notification is received the frame is flushed from memory to make room for a new frame to be fetched from AHB system memory.

In full duplex mode, the frame is removed from the packet buffer on the fly.

Other than underflow, the only MAC related errors that can occur are due to collisions during half duplex transmissions. When a collision occurs the frame still exists in the packet buffer memory so can be retried directly from there. After sixteen failed transmit attempts, the frame will be flushed from the packet buffer.

38.6.3.8 Receive Packet Buffer

The receive packet buffer stores frames from the MAC receiver along with their status and statistics. Frames with errors are flushed from the packet buffer memory, while good frames are pushed onto the DMA AHB interface.

The receiver packet buffer monitors the FIFO write interface from the MAC receiver and translates the FIFO pushes into packet buffer writes. At the end of the received frame the status and statistics are buffered so that the information can be used when the frame is read out. When programmed in full store and forward mode and the frame has an error, the frame data is immediately flushed from the packet buffer memory allowing subsequent frames to utilize the freed up space. The status and statistics for bad frames are still used to update the GMAC registers.

38.8.73 GMAC Jabbers Received Register

Name: GMAC_JR
Offset: 0x18C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							JRX[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	JRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – JRX[9:0] Jabbers Received
This bit field counts the number of frames received exceeding 1518 Bytes in length (1536 Bytes if GMAC_NCFGR.MAXFS is written to '1') and have either a CRC error, an alignment error or a receive symbol error.

39.6.29 Device DMA Channel x Control Register

Name: USBHS_DEVDMACONTROLx
Offset: 0x0308 + x*0x10 [x=0..6]
Reset: 0
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	BUFF_LENGTH[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	BUFF_LENGTH[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	BURST_LCK	DESC_LD_IT	END_BUFFIT	END_TR_IT	END_B_EN	END_TR_EN	LDNXT_DSC	CHANN_ENB
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – BUFF_LENGTH[15:0] Buffer Byte Length (Write-only)
This field determines the number of bytes to be transferred until end of buffer. The maximum channel transfer size (32 KBytes) is reached when this field is 0 (default value). If the transfer size is unknown, this field should be set to 0, but the transfer end may occur earlier under USB device control.

When this field is written, the USBHS_DEVDMASTATUSx.BUFF_COUNT field is updated with the write value.

Notes: 1. Bits [31:2] are only writable when issuing a channel Control Command other than “Stop Now”.

2. For reliability, it is highly recommended to wait for both the USBHS_DEVDMASTATUSx.CHAN_ACT and the USBHS_DEVDMASTATUSx.CHAN_ENB flags to be at 0, thus ensuring the channel has been stopped before issuing a command other than “Stop Now”.

Bit 7 – BURST_LCK Burst Lock Enable

Value	Description
0	The DMA never locks bus access.
1	USB packets AHB data bursts are locked for maximum optimization of the bus bandwidth usage and maximization of fly-by AHB burst duration.

Bit 6 – DESC_LD_IT Descriptor Loaded Interrupt Enable

39.6.53 Host Pipe x Set Register (Isochronous Pipes)

Name: USBHS_HSTPIPIFRx (ISOPIPES)
Offset: 0x0590 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

This register view is relevant only if PTYPE = 0x1 in "Host Pipe x Configuration Register".

For additional information, see "Host Pipe x Status Register (Isochronous Pipes)".

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Sets the corresponding bit in USBHS_HSTPIPISRx, which may be useful for test or debug purposes.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				NBUSYBKS				
Access								
Reset				0				

Bit	7	6	5	4	3	2	1	0
	SHORTPACKETIS	CRCERRIS	OVERFIS	NAKEDIS	PERRIS	UNDERFIS	TXOUTIS	RXINIS
Access								
Reset	0	0	0	0	0	0	0	0

Bit 12 – NBUSYBKS Number of Busy Banks Set

Bit 7 – SHORTPACKETIS Short Packet Interrupt Set

Bit 6 – CRCERRIS CRC Error Interrupt Set

Bit 5 – OVERFIS Overflow Interrupt Set

Bit 4 – NAKEDIS NAKed Interrupt Set

Bit 3 – PERRIS Pipe Error Interrupt Set

Value	Description
0	Cleared when USBHS_HSTPIPIDR.OVERFIEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.OVERFIE).
1	Set when USBHS_HSTPIPIER.OVERFIES = 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.OVERFIE).

Bit 4 – NAKEDE NAKed Interrupt Enable

Value	Description
0	Cleared when USBHS_HSTPIPIDR.NAKEDEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.NAKEDE).
1	Set when USBHS_HSTPIPIER.NAKEDES = 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.NAKEDE).

Bit 3 – PERRE Pipe Error Interrupt Enable

Value	Description
0	Cleared when USBHS_HSTPIPIDR.PERREC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.PERRE).
1	Set when USBHS_HSTPIPIER.PERRES = 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.PERRE).

Bit 2 – TXSTPE Transmitted SETUP Interrupt Enable

Value	Description
0	Cleared when USBHS_HSTPIPIDR.TXSTPEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.TXSTPE).
1	Set when USBHS_HSTPIPIER.TXSTPES = 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.TXSTPE).

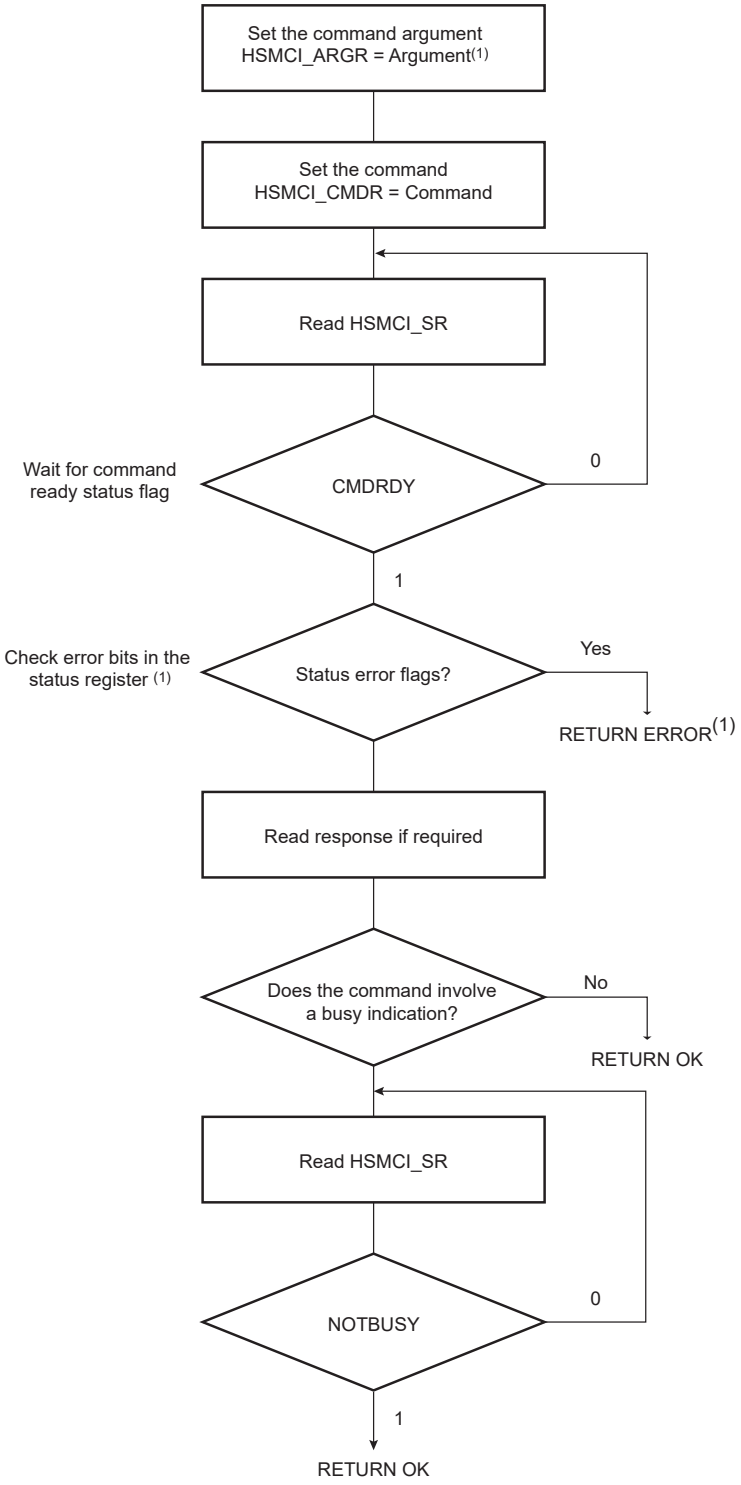
Bit 1 – TXOUTE Transmitted OUT Data Interrupt Enable

Value	Description
0	Cleared when USBHS_HSTPIPIDR.TXOUTEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.TXOUTE).
1	Set when USBHS_HSTPIPIER.TXOUTES = 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.TXOUTE).

Bit 0 – RXINE Received IN Data Interrupt Enable

Value	Description
0	Cleared when USBHS_HSTPIPIDR.RXINEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.RXINE).
1	Set when USBHS_HSTPIPIER.RXINES = 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.RXINE).

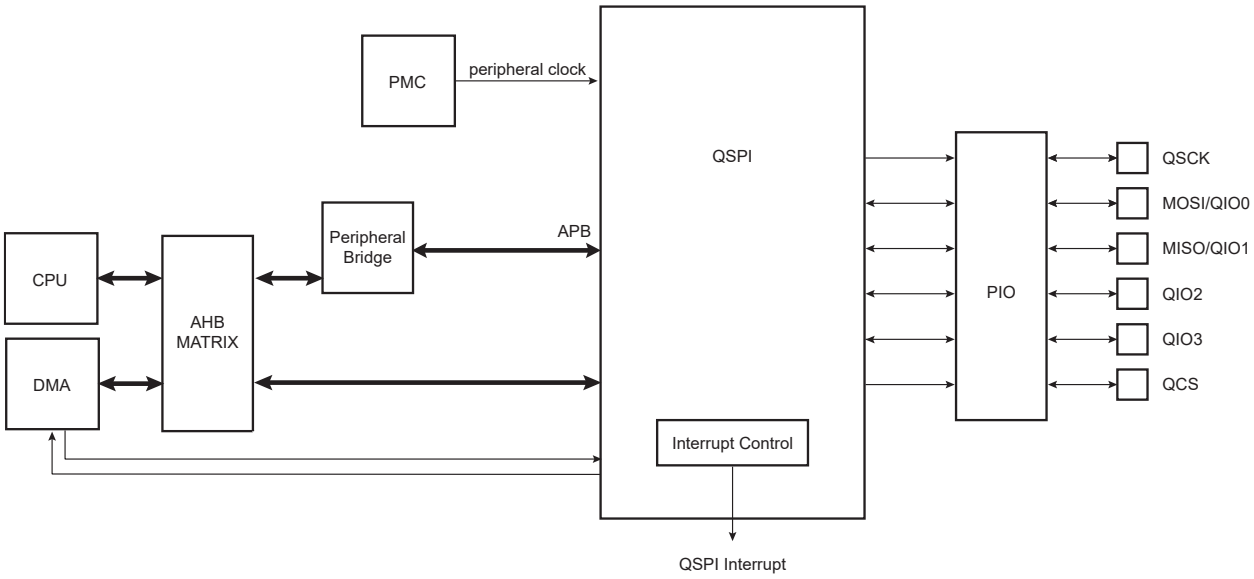
Figure 40-7. Command/Response Functional Flow Diagram



Note: If the command is SEND_OP_COND, the CRC error flag is always present (refer to R3 response in the High Speed MultiMedia Card specification) .

42.3 Block Diagram

Figure 42-1. Block Diagram



42.4 Signal Description

Table 42-1. Signal Description

Pin Name	Pin Description	Type
QSCK	Serial Clock	Output
MOSI (QIO0) (1)(2)	Data Output (Data Input Output 0)	Output (Input/Output)
MISO (QIO1) (1)(2)	Data Input (Data Input Output 1)	Input (Input/Output)
QIO2 (3)	Data Input Output 2	Input/Output
QIO3 (3)	Data Input Output 3	Input/Output
QCS	Peripheral Chip Select	Output

Note:

1. MOSI and MISO are used for single-bit SPI operation.
2. QIO0–QIO1 are used for Dual SPI operation.
3. QIO0–QIO3 are used for Quad SPI operation.

42.5 Product Dependencies

42.5.1 I/O Lines

The pins used for interfacing the compliant external devices may be multiplexed with PIO lines. The programmer must first program the PIO controllers to assign the QSPI pins to their peripheral functions.

44.9.18 SSC Write Protection Status Register

Name: SSC_WPSR
Offset: 0xE8
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	WPVSRC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	WPVSRC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
								WPVS
Access								R
Reset								0

Bits 23:8 – WPVSRC[15:0] Write Protect Violation Source
When WPVS = 1, WPVSRC indicates the register address offset at which a write access has been attempted.

Bit 0 – WPVS Write Protection Violation Status

Value	Description
0	No write protection violation has occurred since the last read of the SSC_WPSR.
1	A write protection violation has occurred since the last read of the SSC_WPSR. If this violation is an unauthorized attempt to write a protected register, the associated violation is reported into field WPVSRC.

Offset	Name	Bit Pos.								
0x58	TC_RB1	7:0	RB[7:0]							
		15:8	RB[15:8]							
		23:16	RB[23:16]							
		31:24	RB[31:24]							
0x5C	TC_RC1	7:0	RC[7:0]							
		15:8	RC[15:8]							
		23:16	RC[23:16]							
		31:24	RC[31:24]							
0x60	TC_SR1	7:0	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
		15:8								
		23:16						MTIOB	MTIOA	CLKSTA
		31:24								
0x64	TC_IER1	7:0	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
		15:8								
		23:16								
		31:24								
0x68	TC_IDR1	7:0	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
		15:8								
		23:16								
		31:24								
0x6C	TC_IMR1	7:0	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
		15:8								
		23:16								
		31:24								
0x70	TC_EMR1	7:0			TRIGSRCB[1:0]				TRIGSRCA[1:0]	
		15:8								NODIVCLK
		23:16								
		31:24								
0x74 ... 0x7F	Reserved									
0x80	TC_CCR2	7:0						SWTRG	CLKDIS	CLKEN
		15:8								
		23:16								
		31:24								
0x84	TC_CMR2	7:0	LDBDIS	LDBSTOP	BURST[1:0]		CLKI	TCCLKS[2:0]		
		15:8	WAVE	CPCTRG				ABETRG	ETRGEDG[1:0]	
		23:16		SBSMPLR[2:0]			LDRB[1:0]		LDRA[1:0]	
		31:24								
0x84	TC_CMR2	7:0	CPCDIS	CPCSTOP	BURST[1:0]		CLKI	TCCLKS[2:0]		
		15:8	WAVE	WAVSEL[1:0]		ENETRG	EEVT[1:0]		EEVTEDG[1:0]	
		23:16	ASWTRG[1:0]		AEEVT[1:0]		ACPC[1:0]		ACPA[1:0]	
		31:24	BSWTRG[1:0]		BEEVT[1:0]		BCPC[1:0]		BCPB[1:0]	
0x88	TC_SMMR2	7:0							DOWN	GCEN
		15:8								
		23:16								

converted to a gain error by the AFE. The noise generated by V_{VREFP} is converted by the AFE to count noise.

Table 59-30. VREFP Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VREFP}	Voltage Range	Full operational	1.7	–	VDDIN	V
	RMS Noise (see **Note 2**)	Bandwidth up to 1.74MHz VREFP=1.7V	–	–	120	µV
R_{VREFP}	Input DC Impedance	AFE reference resistance bridge (see **Note 1**)	–	4.7	–	kOhm
Vin	Input Linear Range (see **Note 3**)	Operational Range	2	-	98	%VVREFP
I_{VREFP}	Current	V_{VREFP} = 3.3V	–	0.8	–	mA

Note:

1. When the AFE is in Sleep mode, the VREFP impedance has a minimum of 10 MOhm.
2. Requested noise on VREFP.
3. Electrical parameters specified inside the operational range. Exceeding this range can introduce additional INL error up to +/- 5 LSB and temperature dependency up to +/-10 LSB.

59.8.3 AFE Timings

Table 59-31. AFE Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{AFE\ Clock}$	Clock Frequency	–	4	20	40	MHz
$t_{AFE\ Clock}$	Clock Period	–	25	50	250	ns
f_S	Sampling Frequency (see **Note 1**)	–	–	–	1.74	MHz
t_{START}	AFE Startup Time	Sleep mode to Normal mode	–	–	4	µs
		Fast Wake-up mode to Normal mode	-	-	2	µs

Note:

1. $f_s = 1 / t_{AFE\_conv}$ in Free Run mode; otherwise defined by the trigger timing.

59.8.4 AFE Transfer Function

The first operation of the AFE is a sampling function relative to V_{DAC}. V_{DAC} is generated by an internal DAC0 or DAC1. All operations after the Sample-and-Hold are differential relative to an internal common mode voltage $V_{CM} = V_{VREFP}/2$.

In Differential mode, the Sample-and-Hold common mode voltage is equal to $V_{DAC} = V_{VREFP}/2$ (set by software DAC0 and DAC1 to code 512).

In Single-ended mode, V_{DAC} is the common mode voltage. V_{DAC} is the output of DAC0 or DAC1 voltage. All operations after the Sample-and-Hold are differential, including those in Single-ended mode.

For the formula example, the internal DAC0 or DAC1 is set for the code 512.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_S	Settling Time	Overdrive > 100 mV (ACC_ACR.ISEL = 0)	–	–	1.5	µs
		Overdrive > 100 mV (ACC_ACR.ISEL = 1)	–	–	0.15	

59.10 Temperature Sensor

The temperature sensor is connected to channel 11 of the AFE0.

The temperature sensor provides an output voltage (V_{TEMP}) that is proportional to absolute temperature (PTAT).

Improvement of the raw performance of the temperature sensor acquisition can be achieved by performing a single temperature point calibration to remove the initial inaccuracies (V_{TEMP} and ADC offsets).

Table 59-42. Temperature Sensor Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{TEMP}	Output Voltage via AD11	T_A = 25°C	0.64	0.72	0.8	V
dV_{TEMP}/dT	Temperature Sensitivity (Slope Voltage versus Temperature)	–	2.06	2.33	2.60	mV/°C
t_S	VTEMP Settling Time	When V_{TEMP} is sampled by the AFEC, the required track-and-hold time to ensure 1°C accurate settling	–	–	1	µs
–	Temperature Accuracy	After offset calibration over T_A range [-40°C : +105°C]	-10	–	10	°C
t_{START}	Startup Time	–	–	–	30	µs
I_{VDDIN}	Current Consumption	–	–	130	270	µA

Note: AFE Gain Error and Offset error considered calibrated. This calibration at ambient temperature is not a feature of the product and is performed by the user's application.

59.11 12-bit DAC Characteristics

Table 59-43. Analog Power Supply Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VDDIN}	Current Consumption	Sleep mode (Clock OFF)	–	10	–	µA
		Normal mode with one output on, DACC_ACR.IBCTLCHx =3 (see **Note 1**) FS = 1 MSps, no R_{LOAD}, V_{DDIN} = 3.3V	–	200	800	

Date	Changes
	Added Figure 53-2, “Conversion Sequence in Trigger Mode”and Figure 53-3, “Conversion Sequence in Free-running Mode”. Section 53.6.4.1 “Trigger Mode”: removed fragment ‘(either DATRG pin or timer counter events)’. Section 53.6.4.2 “Free-Running Mode”: added sentence on FIFO. Updated Figure 53-3, “Conversion Sequence in Free-running Mode”. Updated Section 53.6.4.3 “Max Speed Mode” and added Figure 53-4, “Conversion Sequence in Max Speed Mode”. Updated Section 53.6.4.4 “Bypass Mode”. Deleted section “DACC Timings”. Table 53-4 “Register Mapping”: modified reset value for DACC_MR. Section 53.7.2 “DACC Mode Register”: added bit ZERO (bit 5) and bit description. Section 53.7.3 “DACC Trigger Register”: bit description changed for TRGSEL bit. Removed bits ENDTX0, ENDTX1, TXBUFE0 and TXBUFE1 from Section 53.7.8 “DACC Interrupt Enable Register”, Section 53.7.9 “DACC Interrupt Disable Register”, Section 53.7.10 “DACC Interrupt Mask Register” and Section 53.7.11 “DACC Interrupt Status Register”.
	Section 55. “Integrity Check Monitor (ICM)” Section 55.5.2.2 “ICM Region Configuration Structure Member”: removed MRPROT field. Section 55.6.1 “ICM Configuration Register”: removed fields HAPROT and DAPROT; updated description DUALBUFF field
	Updated Section 58. “Electrical Characteristics”.
	Updated Section 59. “Mechanical Characteristics”.
	Added Section 60. “Schematic Checklist”.
	Added Section 63. “Errata”.

Table 62-5. SAM E70/S70/V70/V71 Datasheet Rev. 44003B – Revision History

Date	Changes
24-Feb-15	“Description”: updated details on PWM, 16-bit timers, RTC, RTT and Backup mode. Added note to QFN64 package on availability.
	“Features”: updated details on PWM. Added note to QFN64 package on availability.
	Section 1. “Configuration Summary” Table 1-1 “Configuration Summary”: Modifications made to Timer Counter Channels I/O, USART/UART, QSPI, SPI, USART SPI.
	Section 2. “Block Diagram”: added AHBP block. Added Backup RAM block. Removed TRACECTL. Changed block name to Serial Wire Debug/JTAG Boundary Scan (was JTAG