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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70n20b-cnt

16. Debug and Test Features

16.1 Description

The device features a number of complementary debug and test capabilities. The Serial Wire Debug Port (SW-DP) is used for standard debugging functions, such as downloading code and single-stepping through programs. It also embeds a serial wire trace.

16.2 Embedded Characteristics

- Debug access to all memory and registers in the system, including Cortex-M register bank, when the core is running, halted, or held in reset.
- Serial Wire Debug Port (SW-DP) debug access
- Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
- Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Instrumentation Trace Macrocell (ITM) for support of printf style debugging
- 6-pin Embedded Trace Macrocell (ETM) for instruction trace stream, including CoreSight™ Trace Port Interface Unit (TPIU)
- IEEE1149.1 JTAG Boundary scan on All Digital Pins

16.3 Associated Documents

The SAM E70/S70/V70/V71 implements the standard ARM CoreSight macrocell. For information on CoreSight, the following reference documents are available from the ARM web site (www.arm.com):

- Cortex-M7 User Guide Reference Manual (ARM DUI 0644)
- Cortex-M7 Technical Reference Manual (ARM DDI 0489)
- CoreSight Technology System Design Guide (ARM DGI 0012)
- CoreSight Components Technical Reference Manual (ARM DDI 0314)
- ARM Debug Interface v5 Architecture Specification (Doc. ARM IHI 0031)
- ARMv7-M Architecture Reference Manual (ARM DDI 0403)

28.5 Register Summary

Offset	Name	Bit Pos.								
0x00	RTT_MR	7:0	RTPRES[7:0]							
		15:8	RTPRES[15:8]							
		23:16				RTTDIS		RTTRST	RTTINCIEN	ALMIEN
		31:24								RTC1HZ
0x04	RTT_AR	7:0	ALMV[7:0]							
		15:8	ALMV[15:8]							
		23:16	ALMV[23:16]							
		31:24	ALMV[31:24]							
0x08	RTT_VR	7:0	CRTV[7:0]							
		15:8	CRTV[15:8]							
		23:16	CRTV[23:16]							
		31:24	CRTV[31:24]							
0x0C	RTT_SR	7:0							RTTINC	ALMS
		15:8								
		23:16								
		31:24								

28.5.4 Real-time Timer Status Register

Name: RTT_SR
Offset: 0x0C
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							RTTINC	ALMS
Access							R	R
Reset							0	0

Bit 1 – RTTINC Prescaler Roll-over Status (cleared on read)

Value	Description
0	No prescaler roll-over occurred since the last read of the RTT_SR.
1	Prescaler roll-over occurred since the last read of the RTT_SR.

Bit 0 – ALMS Real-time Alarm Status (cleared on read)

Value	Description
0	The Real-time Alarm has not occurred since the last read of RTT_SR.
1	The Real-time Alarm occurred since the last read of RTT_SR.

- The frequency of peripheral clock must be strictly superior to two times the frequency of the clock of the device which generates the parallel data.

32.5.14.4 Programming Sequence

32.5.14.4.1 Without DMA

1. Write PIO_PCIDR and PIO_PCIER in order to configure the Parallel Capture mode interrupt mask.
2. Write PIO_PCMR to set the fields DSIZE, ALWYS, HALFS and FRSTS in order to configure the Parallel Capture mode WITHOUT enabling the Parallel Capture mode.
3. Write PIO_PCMR to set the PCEN bit to one in order to enable the Parallel Capture mode WITHOUT changing the previous configuration.
4. Wait for a data ready by polling the DRDY flag in PIO_PCISR or by waiting for the corresponding interrupt.
5. Check OVRE flag in PIO_PCISR.
6. Read the data in PIO_PCRHR.
7. If new data are expected, go to step 4.
8. Write PIO_PCMR to set the PCEN bit to zero in order to disable the Parallel Capture mode WITHOUT changing the previous configuration.

32.5.14.4.2 With DMA

1. Write PIO_PCIDR and PIO_PCIER in order to configure the Parallel Capture mode interrupt mask.
2. Configure DMA transfer in DMA registers.
3. Write PIO_PCMR to set the fields DSIZE, ALWYS, HALFS and FRSTS in order to configure the Parallel Capture mode WITHOUT enabling the Parallel Capture mode.
4. Write PIO_PCMR to set PCEN bit to one in order to enable the Parallel Capture mode WITHOUT changing the previous configuration.
5. Wait for the DMA status flag to indicate that the buffer transfer is complete.
6. Check OVRE flag in PIO_PCISR.
7. If a new buffer transfer is expected, go to step 5.
8. Write PIO_PCMR to set the PCEN bit to zero in order to disable the Parallel Capture mode WITHOUT changing the previous configuration.

32.5.15 I/O Lines Programming Example

The programming example shown in the following table is used to obtain the following configuration:

- 4-bit output port on I/O lines 0 to 3 (should be written in a single write operation), open-drain, with pullup resistor
- Four output signals on I/O lines 4 to 7 (to drive LEDs for example), driven high and low, no pullup resistor, no pulldown resistor
- Four input signals on I/O lines 8 to 11 (to read push-button states for example), with pullup resistors, glitch filters and input change interrupts
- Four input signals on I/O line 12 to 15 to read an external device status (polled, thus no input change interrupt), no pullup resistor, no glitch filter
- I/O lines 16 to 19 assigned to peripheral A functions with pullup resistor
- I/O lines 20 to 23 assigned to peripheral B functions with pulldown resistor
- I/O lines 24 to 27 assigned to peripheral C with input change interrupt, no pullup resistor and no pulldown resistor
- I/O lines 28 to 31 assigned to peripheral D, no pullup resistor and no pulldown resistor

38.8.84 GMAC 1588 Timer Seconds High Register

Name: GMAC_TSH
Offset: 0x1C0
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TCS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TCS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – TCS[15:0] Timer Count in Seconds
This register is writable. It increments by 1 when the IEEE 1588 nanoseconds counter counts to one second. It may also be incremented when the Timer Adjust Register is written.

39.5.2.12 Management of IN Endpoints

Overview

IN packets are sent by the USB device controller upon IN requests from the host. All data which acknowledges or not the bank can be written when it is full.

The endpoint must be configured first.

The USBHS_DEVEPTISRx.TXINI bit is set at the same time as USBHS_DEVEPTIMRx.FIFOCON when the current bank is free. This triggers a PEP_x interrupt if the Transmitted IN Data Interrupt Enable (USBHS_DEVEPTIMRx.TXINE) bit is one.

USBHS_DEVEPTISRx.TXINI is cleared by software (by writing a one to the Transmitted IN Data Interrupt Clear bit (USBHS_DEVEPTIDRx.TXINIC) to acknowledge the interrupt, which has no effect on the endpoint FIFO.

The user then writes into the FIFO and writes a one to the FIFO Control Clear (USBHS_DEVEPTIDRx.FIFOCONC) bit to clear the USBHS_DEVEPTIMRx.FIFOCON bit. This allows the USBHS to send the data. If the IN endpoint is composed of multiple banks, this also switches to the next bank. The USBHS_DEVEPTISRx.TXINI and USBHS_DEVEPTIMRx.FIFOCON bits are updated in accordance with the status of the next bank.

USBHS_DEVEPTISRx.TXINI is always cleared before clearing USBHS_DEVEPTIMRx.FIFOCON.

The USBHS_DEVEPTISRx.RWALL bit is set when the current bank is not full, i.e., when the software can write further data into the FIFO.

Figure 39-11. Example of an IN Endpoint with one Data Bank

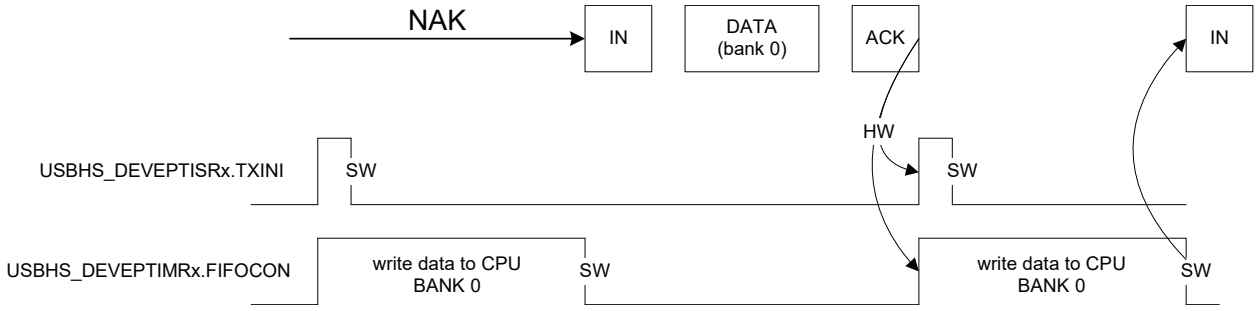
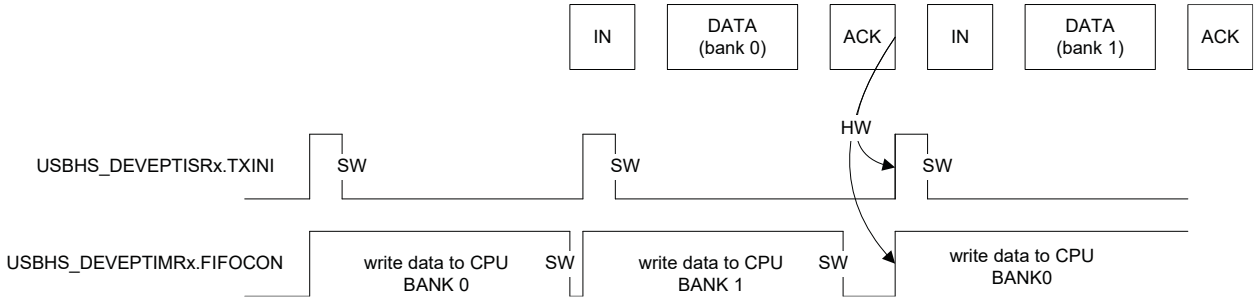


Figure 39-12. Example of an IN Endpoint with two Data Banks



Detailed Description

The data is written as follows:

- When the bank is empty, USBHS_DEVEPTISRx.TXINI and USBHS_DEVEPTIMRx.FIFOCON are set, which triggers a PEP_x interrupt if USBHS_DEVEPTIMRx.TXINE = 1.
- The user acknowledges the interrupt by clearing USBHS_DEVEPTISRx.TXINI.

Offset	Name	Bit Pos.								
		31:24								
0x05C8	USBHS_HSTPIPIMR2 (INTPIPES)	7:0	SHORTPACKETIE	RXSTALLDE	OVERFIE	NAKEDE	PERRE	UNDERFIE	TXOUTE	RXINE
		15:8		FIFOCON		NBUSYBKE				
		23:16						RSTDT	PFREEZE	PDISHDMA
		31:24								
0x05C8	USBHS_HSTPIPIMR2 (ISOPIPES)	7:0	SHORTPACKETIE	CRCERRE	OVERFIE	NAKEDE	PERRE	UNDERFIE	TXOUTE	RXINE
		15:8		FIFOCON		NBUSYBKE				
		23:16						RSTDT	PFREEZE	PDISHDMA
		31:24								
0x05CC	USBHS_HSTPIPIMR3	7:0	SHORTPACKETIE	RXSTALLDE	OVERFIE	NAKEDE	PERRE	TXSTPE	TXOUTE	RXINE
		15:8		FIFOCON		NBUSYBKE				
		23:16						RSTDT	PFREEZE	PDISHDMA
		31:24								
0x05CC	USBHS_HSTPIPIMR3 (INTPIPES)	7:0	SHORTPACKETIE	RXSTALLDE	OVERFIE	NAKEDE	PERRE	UNDERFIE	TXOUTE	RXINE
		15:8		FIFOCON		NBUSYBKE				
		23:16						RSTDT	PFREEZE	PDISHDMA
		31:24								
0x05CC	USBHS_HSTPIPIMR3 (ISOPIPES)	7:0	SHORTPACKETIE	CRCERRE	OVERFIE	NAKEDE	PERRE	UNDERFIE	TXOUTE	RXINE
		15:8		FIFOCON		NBUSYBKE				
		23:16						RSTDT	PFREEZE	PDISHDMA
		31:24								
0x05D0	USBHS_HSTPIPIMR4	7:0	SHORTPACKETIE	RXSTALLDE	OVERFIE	NAKEDE	PERRE	TXSTPE	TXOUTE	RXINE
		15:8		FIFOCON		NBUSYBKE				
		23:16						RSTDT	PFREEZE	PDISHDMA
		31:24								
0x05D0	USBHS_HSTPIPIMR4 (INTPIPES)	7:0	SHORTPACKETIE	RXSTALLDE	OVERFIE	NAKEDE	PERRE	UNDERFIE	TXOUTE	RXINE
		15:8		FIFOCON		NBUSYBKE				
		23:16						RSTDT	PFREEZE	PDISHDMA
		31:24								
0x05D0	USBHS_HSTPIPIMR4 (ISOPIPES)	7:0	SHORTPACKETIE	CRCERRE	OVERFIE	NAKEDE	PERRE	UNDERFIE	TXOUTE	RXINE
		15:8		FIFOCON		NBUSYBKE				
		23:16						RSTDT	PFREEZE	PDISHDMA
		31:24								
0x05D4	USBHS_HSTPIPIMR5	7:0	SHORTPACKETIE	RXSTALLDE	OVERFIE	NAKEDE	PERRE	TXSTPE	TXOUTE	RXINE
		15:8		FIFOCON		NBUSYBKE				
		23:16						RSTDT	PFREEZE	PDISHDMA
		31:24								

39.6.3 General Status Clear Register

Name: USBHS_SCR
Offset: 0x0808
Property: Write-only

This register always reads as zero.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				RDERRIC				
Access								
Reset								

Bit 4 – RDERRIC Remote Device Connection Error Interrupt Clear

Value	Description
0	No effect.
1	Clears the RDERRI bit in USBHS_SR.

Value	Description
0	No effect.
1	Disables the QSPI.

Bit 0 – QSPIEN QSPI Enable

Value	Description
0	No effect.
1	Enables the QSPI to transfer and receive data.

43.7.13 TWIHS SleepWalking Matching Register

Name: TWIHS_SWMR
Offset: 0x4C
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the TWIHS Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	DATAM[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
		SADR3[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
		SADR2[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		SADR1[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 31:24 – DATAM[7:0] Data Match
The TWIHS module extends the SleepWalking matching process to the first received data, comparing it with DATAM if DATAMEN bit is enabled.

Bits 22:16 – SADR3[6:0] Slave Address 3
Slave address 3. The TWIHS module matches on this additional address if SADR3EN bit is enabled.

Bits 14:8 – SADR2[6:0] Slave Address 2
Slave address 2. The TWIHS module matches on this additional address if SADR2EN bit is enabled.

Bits 6:0 – SADR1[6:0] Slave Address 1
Slave address 1. The TWIHS module matches on this additional address if SADR1EN bit is enabled.

45.6.3 Master, Controller and Slave Modes

In Master and Controller modes, the I2SC provides the master clock, the serial clock and the word select. I2SC_MCK, I2SC_CK, and I2SC_WS pins are outputs.

In Controller mode, the I2SC receiver and transmitter are disabled. Only the clocks are enabled and used by an external receiver and/or transmitter.

In Slave mode, the I2SC receives the serial clock and the word select from an external master. I2SC_CK and I2SC_WS pins are inputs.

The mode is selected by writing the MODE field in the I2SC_MR. Since the MODE field changes the direction of the I2SC_WS and I2SC_SCK pins, the I2SC_MR must be written when the I2SC is stopped.

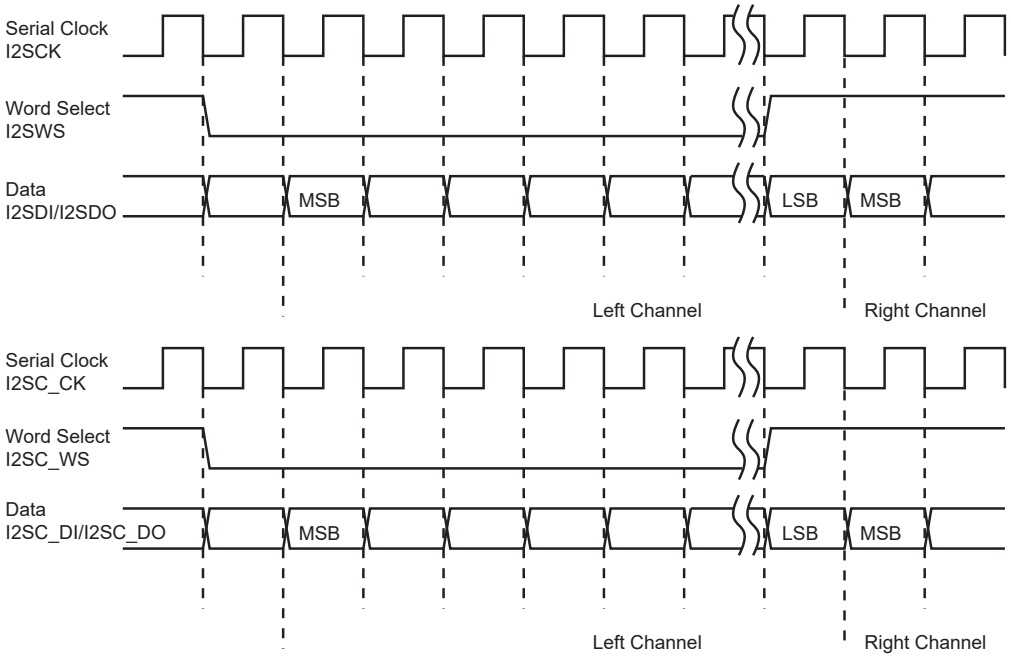
Related Links

19. Bus Matrix (MATRIX)

45.6.4 I²S Reception and Transmission Sequence

As specified in the I²S protocol, data bits are left-justified in the word select time slot, with the MSB transmitted first, starting one clock period after the transition on the word select line.

Figure 45-2. I²S Reception and Transmission Sequence



Data bits are sent on the falling edge of the serial clock and sampled on the rising edge of the serial clock. The word select line indicates the channel in transmission, a low level for the left channel and a high level for the right channel.

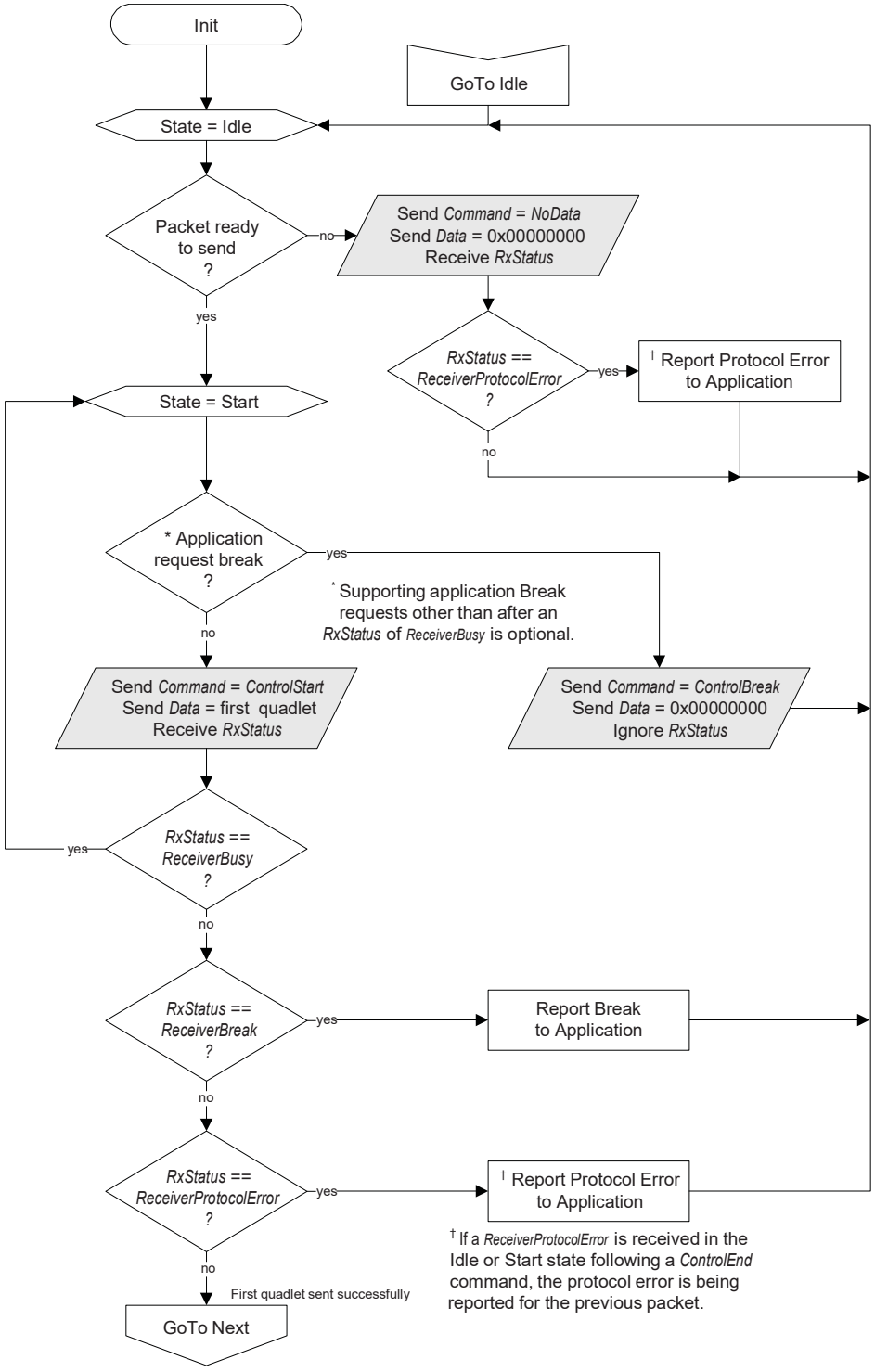
The length of transmitted words can be chosen among 8, 16, 18, 20, 24, and 32 bits by writing the I2SC_MR.DATALENGTH field.

If the time slot allows for more data bits than written in the I2SC_MR.DATALENGTH field, zeroes are appended to the transmitted data word or extra received bits are discarded.

45.6.5 Serial Clock and Word Select Generation

The generation of clocks in the I2SC is described in figure ”Mono”.

Figure 48-6. Control Packet Tx Device Protocol: Start



Bit 1 – LKSYSCMD Network Lock System Command Detected in the System Quadlet (cleared by writing a 0)
Set by hardware, cleared by software.

Bit 0 – RSTSYSCMD Reset System Command Detected in the System Quadlet (cleared by writing a 0)
Set by hardware, cleared by software.

48.7.5 MediaLB System Data Register

Name: MLB_MSD
Offset: 0x024
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	SD3[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	SD2[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SD1[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SD0[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:24 – SD3[7:0] System Data (Byte 3)
Updated with MediaLB Data[31:24] when a MediaLB software system command is received in the system quadlet. If MLB_MSS.SWSYSCMD is already set, then SD3 is not updated.

Bits 23:16 – SD2[7:0] System Data (Byte 2)
Updated with MediaLB Data[23:16] when a MediaLB software system command is received in the system quadlet. If MLB_MSS.SWSYSCMD is already set, then SD2 is not updated.

Bits 15:8 – SD1[7:0] System Data (Byte 1)
Updated with MediaLB Data[15:8] when a MediaLB software system command is received in the system quadlet. If MLB_MSS.SWSYSCMD is already set, then SD1 is not updated.

Bits 7:0 – SD0[7:0] System Data (Byte 0)
Updated with MediaLB Data[7:0] when a MediaLB software system command is received in the system quadlet. If MLB_MSS.SWSYSCMD is already set, then SD0 is not updated.

51.7.2 PWM Enable Register

Name: PWM_ENA
Offset: 0x04
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					CHID3	CHID2	CHID1	CHID0
Access					W	W	W	W
Reset					0	0	0	–

Bits 0, 1, 2, 3 – CHIDx Channel ID

Value	Description
0	No effect.
1	Enable PWM output for channel x.

Value	Name	Description
2	SUT16	16 periods of AFE clock
3	SUT24	24 periods of AFE clock
4	SUT64	64 periods of AFE clock
5	SUT80	80 periods of AFE clock
6	SUT96	96 periods of AFE clock
7	SUT112	112 periods of AFE clock
8	SUT512	512 periods of AFE clock
9	SUT576	576 periods of AFE clock
10	SUT640	640 periods of AFE clock
11	SUT704	704 periods of AFE clock
12	SUT768	768 periods of AFE clock
13	SUT832	832 periods of AFE clock
14	SUT896	896 periods of AFE clock
15	SUT960	960 periods of AFE clock

Bits 15:8 – PRESCAL[7:0] Prescaler Rate Selection
PRESCAL = $f_{peripheral\ clock}$/ $f_{AFE\ Clock}$ - 1

When PRESCAL is cleared, no conversion is performed.

Bit 7 – FREERUN Free Run Mode

Value	Name	Description
0	OFF	Normal mode
1	ON	Free Run mode: never wait for any trigger.

Bit 6 – FWUP Fast Wakeup

Value	Name	Description
0	OFF	Normal Sleep mode: the sleep mode is defined by the SLEEP bit.
1	ON	Fast Wakeup Sleep mode: the voltage reference is ON between conversions and AFE is OFF.

Bit 5 – SLEEP Sleep Mode

Value	Name	Description
0	NORMAL	Normal mode: the AFE and reference voltage circuitry are kept ON between conversions.
1	SLEEP	Sleep mode: the AFE and reference voltage circuitry are OFF between conversions.

Bits 3:1 – TRGSEL[2:0] Trigger Selection

Value	Name	Description
0	AFEC_TRIG0	AFE0_ADTRG for AFEC0 / AFE1_ADTRG for AFEC1
1	AFEC_TRIG1	TIOA Output of the Timer Counter Channel 0 for AFEC0/TIOA Output of the Timer Counter Channel 3 for AFEC1
2	AFEC_TRIG2	TIOA Output of the Timer Counter Channel 1 for AFEC0/TIOA Output of the Timer Counter Channel 4 for AFEC1

53. Digital-to-Analog Converter Controller (DACC)

53.1 Description

The Digital-to-Analog Converter Controller (DACC) offers up to two single-ended analog outputs or one differential analog output, making it possible for the digital-to-analog conversion to drive up to two independent analog lines.

The DACC supports 12-bit resolution.

The DACC operates in Free-running mode, Max speed mode, Trigger mode or Interpolation mode.

The DACC integrates a Bypass mode which minimizes power consumption in case of a limited sampling rate conversion.

Each channel connects with a separate DMA channel. This feature reduces both power consumption and processor intervention.

53.2 Embedded Characteristics

- Up to Two Independent Single-Ended Analog Outputs or One Differential Analog Output
- 12-bit Resolution
- Integrated Interpolation Filter with 2×, 4×, 8×, 16× or 32× Oversampling Ratio (OSR)
- Reduced Number of System Bus Accesses (Word Transfer Mode)
- Individual Control of Each Analog Channel
- Hardware Triggers
  - One Trigger Selection Per Channel
    – External trigger pin
    – Internal events
- DMA Support
- One Internal FIFO per Channel
- Register Write Protection

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
P_D	Power Dissipation	At T_A = 85°C, TFBGA100	–	–	814	mW
		At T_A = 105°C, TFBGA100	–	–	407	mW
P_D	Power Dissipation	At T_A = 85°C, LQFP100	–	–	938	mW
		At T_A = 105°C, LQFP100	–	–	469	mW
P_D	Power Dissipation	At T_A = 85°C, LQFP64	–	–	833	mW
		At T_A = 105°C, LQFP64	–	–	417	mW

58.2 DC Characteristics

The following characteristics are applicable to the operating temperature range: T_A [-40°C : +105°C], unless otherwise specified.

Table 58-3. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDCORE}	DC Supply Core	–	1.20	–	1.32	V
	Allowable Voltage Ripple	rms value 10 kHz to 20 MHz	–	–	20	mV
	Rising Slope	–	1.20	–	30	V/ms
V_{DDIO}	DC Supply I/Os, Backup	(See **Note 1**)	3.0	3.3	3.6	V
	Allowable Voltage Ripple	rms value 10 kHz to 10 MHz	–	–	30	mV
	Rising Slope	–	6.5	–	30	V/ms
V_{DDIN}	DC Supply Voltage Regulator	(See **Note 1**)	3.0	3.3	3.6	V

58.13.1.13.3 MII Mode

Table 58-71. GMAC MII Mode Timings

Symbol	Parameter	Min	Max	Unit
$GMAC_4$	Setup for GCOL from GTXCK rising	10	–	ns
$GMAC_5$	Hold for GCOL from GTXCK rising	10	–	
$GMAC_6$	Setup for GCRS from GTXCK rising	10	–	
$GMAC_7$	Hold for GCRS from GTXCK rising	10	–	
$GMAC_8$	GTXER toggling from GTXCK rising	10	25	
$GMAC_9$	GTXEN toggling from GTXCK rising	10	25	
$GMAC_{10}$	GTX toggling from GTXCK rising	10	25	
$GMAC_{11}$	Setup for GRX from GRXCK	10	–	
$GMAC_{12}$	Hold for GRX from GRXCK	10	–	
$GMAC_{13}$	Setup for GRXER from GRXCK	10	–	
$GMAC_{14}$	Hold for GRXER from GRXCK	10	–	
$GMAC_{15}$	Setup for GRXDV from GRXCK	10	–	
$GMAC_{16}$	Hold for GRXDV from GRXCK	10	–	

Date	Changes
	Section 39.6.3.9 ”Priority Queueing in the DMA”: added Table 39-5 “Queue Size” and updated queue sizes. Section 39.6.15 ”Time Stamp Unit”: changed pin reference from “TIOB11/PD22” to “TIOA11/PD21”. Section 39.6.18 ”Energy-efficient Ethernet Support”: removed all references to Gigabit Ethernet. Updated Section 39.6.19 ”802.1Qav Support - Credit-based Shaping”: added definitions of portTransmitRate and IdleSlope; updated content on queue priority management. Section 39.6.20 ”LPI Operation in the GMAC”: Updated steps for transmit and receive paths. Section 39.8.1 ”GMAC Network Control Register” changed description of NRTSM bit. Section 39.8.107 ”GMAC Received LPI Time” and Section 39.8.109 ”GMAC Transmit LPI Time”: corrected ‘PCLK’ to ‘MCK” in field description. Section 39.8.115 ”GMAC Credit-Based Shaping IdleSlope Register for Queue A” and Section 39.8.116 ”GMAC Credit-Based Shaping IdleSlope Register for Queue B”: updated example for calculation of IdleSlope.
	Section 41. ”Serial Peripheral Interface (SPI)” Section 41.7.4 ”SPI Slave Mode”: added paragraph on SFERR flag. Updated Section 41.7.5 ”Register Write Protection”. Section 41.8.1 ”SPI Control Register”: below register table, added “This register can only be written if the WPCREN bit is cleared in the SPI Write Protection Mode Register.” Section 41.8.6 ”SPI Interrupt Enable Register”, Section 41.8.7 ”SPI Interrupt Disable Register”: below each register table, added “This register can only be written if the WPITEN bit is cleared in the SPI Write Protection Mode Register.” Section 41.8.5 ”SPI Status Register”: added bit SFERR at index 12 and bit description. Section 41.8.10 ”SPI Write Protection Mode Register”: added bit WPITEN at index 1 and bit description. Added bit WPCREN at index 2 and bit description.
12-Oct-16	Section 42. ”Quad Serial Peripheral Interface (QSPI)” Section 42.1 ”Description”: added Note on device support. Section 42.6.5 ”QSPI Serial Memory Mode”: updated text on data transfer constraint. Figure 42-9 “Instruction Transmission Flow Diagram”: corrected typos: --- “Wait for flag QSPI_SR.INSTRE ... “ (was “QSPI_CR“) --- “Wait for flag QSPI_SR.CSR ... “ (was “QSPI_CR“) - Added new instruction: “Read QSPI_SR (dummy read) to clear QSPI_SR.INSTRE and QSPI_SR.CSR“. Updated Figure 42-8 “Instruction Frame”, Figure 42-10 “Continuous Read Mode”, Figure 42-16 “Instruction Transmission Waveform 6”, Figure 42-17 “Instruction Transmission Waveform 7” and Figure 42-19 “Instruction Transmission Waveform 9”.