Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70n21a-ant

11.1.5.4 Lock Regions

Several lock bits are used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Table 11-2. Flash Lock Bits

Flash Size (Kbytes)	Number of Lock Bits	Lock Region Size
2048	128	16 Kbytes
1024	64	16 Kbytes
512	32	16 Kbytes

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

11.1.5.5 Security Bit Feature

The SAM E70/S70/V70/V71 features a security bit based on the GPNVM bit 0. When security is enabled, any access to the Flash, SRAM, core registers and internal peripherals, either through the SW-DP, the ETM interface or the Fast Flash Programming Interface, is blocked. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled through the command “Set General-purpose NVM Bit 0” of the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash, SRAM, Core registers, Internal Peripherals are permitted.

11.1.5.6 Unique Identifier

The device contains a unique identifier of 2 pages of 512 bytes. These 2 pages are read-only and cannot be erased even by the ERASE pin.

The sequence to read the unique identifier area is described in 22.4.3.8 Unique Identifier Area.

The mapping is as follows:

- Bytes [0..15]: 128 bits for unique identifier
- Bytes[16..1023]: Reserved

11.1.5.7 User Signature

Each device contains a user signature of 512 bytes that is available to the user. The user signature can be used to store information such as trimming, keys, etc., that the user does not want to be erased by asserting the ERASE pin or by software ERASE command. Read, write and erase of this area is allowed.

11.1.5.8 Fast Flash Programming Interface (FFPI)

The Fast Flash Programming Interface (FFPI) allows programming the device through a multiplexed fully-handshaked parallel port. It allows gang programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The FFPI is enabled and the Fast Programming mode is entered when TST and PA3 and PA4 are tied low.

These additional modes are:

- Rising edge detection
- Falling edge detection
- Low-level detection
- High-level detection

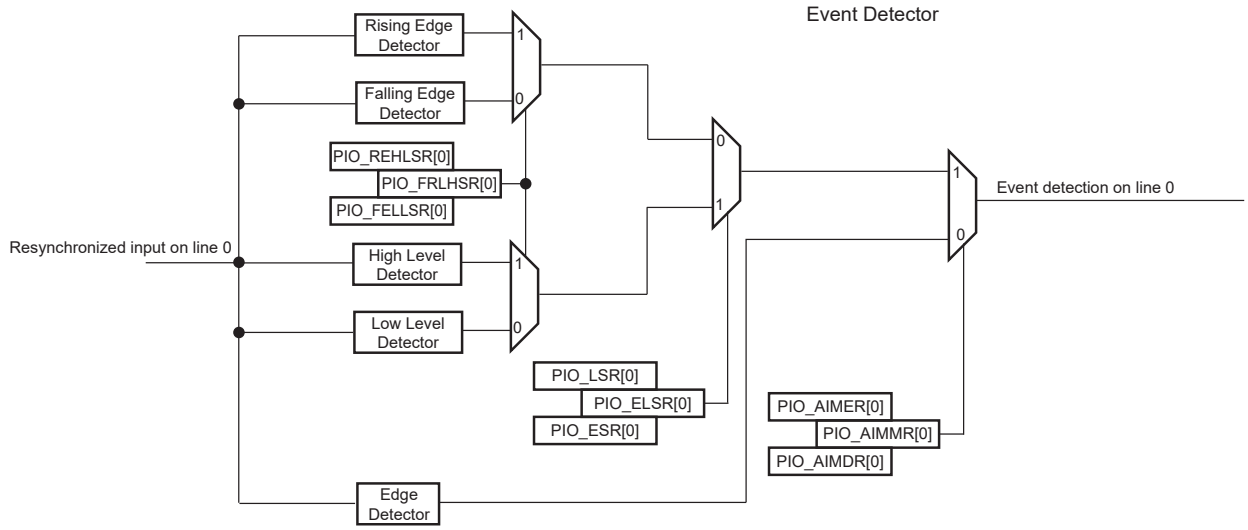
In order to select an additional interrupt mode:

- The type of event detection (edge or level) must be selected by writing in the Edge Select Register (PIO_ESR) and Level Select Register (PIO_LSR) which select, respectively, the edge and level detection. The current status of this selection is accessible through the Edge/Level Status Register (PIO_ELSR).
- The polarity of the event detection (rising/falling edge or high/low-level) must be selected by writing in the Falling Edge/Low-Level Select Register (PIO_FELLSR) and Rising Edge/High-Level Select Register (PIO_REHLSR) which allow to select falling or rising edge (if edge is selected in PIO_ELSR) edge or high- or low-level detection (if level is selected in PIO_ELSR). The current status of this selection is accessible through the Fall/Rise - Low/High Status Register (PIO_FRLHSR).

When an input edge or level is detected on an I/O line, the corresponding bit in the Interrupt Status Register (PIO_ISR) is set. If the corresponding bit in PIO_IMR is set, the PIO Controller interrupt line is asserted.The interrupt signals of the 32 channels are ORed-wired together to generate a single interrupt signal to the interrupt controller.

When the software reads PIO_ISR, all the interrupts are automatically cleared. This signifies that all the interrupts that are pending when PIO_ISR is read must be handled. When an Interrupt is enabled on a “level”, the interrupt is generated as long as the interrupt source is not cleared, even if some read accesses in PIO_ISR are performed.

Figure 32-6. Event Detector on Input Lines (Figure Represents Line 0)



Example of interrupt generation on following lines:

- Rising edge on PIO line 0
- Falling edge on PIO line 1
- Rising edge on PIO line 2
- Low-level on PIO line 3

Offset	Name	Bit Pos.								
		23:16	WPVSRC[15:8]							
		31:24								

35.16.1 Static Memory Controller (SMC) User Interface

The SMC is programmed using the registers listed in the following table. For each Chip Select, a set of four registers is used to program the parameters of the external device connected on it. In the Register Summary, “CS_number” denotes the Chip Select number. 16 bytes (0x10) are required per Chip Select.

Bit 2 – DIM End of Disable Interrupt Mask Bit

Value	Description
0	End of disable interrupt is masked.
1	End of disable interrupt is activated.

Bit 1 – LIM End of Linked List Interrupt Mask Bit

Value	Description
0	End of linked list interrupt is masked.
1	End of linked list interrupt is activated.

Bit 0 – BIM End of Block Interrupt Mask Bit

Value	Description
0	Block interrupt is masked.
1	Block interrupt is activated.

38.8.12 GMAC Interrupt Disable Register

Name: GMAC_IDR
Offset: 0x02C
Reset: –
Property: Write-only

This register is write-only and will always return zero.

The following values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
Access			W	W	R	W	W	W
Reset			–	–	–	–	–	–

Bit	23	22	21	20	19	18	17	16
	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
Access	W	W	W	W	W	W		
Reset	–	–	–	–	–	–		

Bit	15	14	13	12	11	10	9	8
	EXINT	PFTR	PTZ	PFNZ	HRESP	ROVR		
Access	W	W	W	W	W	W		
Reset	–	–	–	–	–	–		

Bit	7	6	5	4	3	2	1	0
	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bit 29 – TSUTIMCMP TSU Timer Comparison

Bit 28 – WOL Wake On LAN

Bit 27 – RXLPISBC Receive LPI indication Status Bit Change
Receive LPI indication status bit change.

Cleared on read.

Bit 26 – SRI TSU Seconds Register Increment

Bit 25 – PDRSFT PDelay Response Frame Transmitted

Bit 24 – PDRQFT PDelay Request Frame Transmitted

Bit 23 – PDRSFR PDelay Response Frame Received

38.8.100 GMAC Transmit LPI Time

Name: GMAC_TXLPITIME
Offset: 0x27C
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	LPITIME[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	LPITIME[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LPITIME[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – LPITIME[23:0] Time in LPI
This field increments once every 16 MCK cycles when the bit TXLPIEN (Enable LPI Transmission (bit 19)) is set in GMAC_NCR.

Cleared on read.

38.8.107 GMAC Credit-Based Shaping IdleSlope Register for Queue B

Name: GMAC_CBSISQB
Offset: 0x4C4
Reset: 0x00000000
Property: Read/Write

Credit-based shaping must be disabled in the GMAC_CBSCR before updating this register.

Bit	31	30	29	28	27	26	25	24
	IS[31:24]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	IS[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	IS[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IS[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – IS[31:0] IdleSlope
IdleSlope value for queue B in bytes/second.

The IdleSlope value is defined as the rate of change of credit when a packet is waiting to be sent. This must not exceed the port transmit rate which is dependent on the speed of operation, e.g., 100 Mb/second = 32'h017D7840.

If 50% of bandwidth was to be allocated to a particular queue in 100 Mb/sec mode, then the IdleSlope value for that queue would be calculated as 32'h017D7840 / 2

Offset	Name	Bit Pos.								
0x0364	USBHS_DEVDMAADDRESS7	7:0	BUFF_ADD[7:0]							
		15:8	BUFF_ADD[15:8]							
		23:16	BUFF_ADD[23:16]							
		31:24	BUFF_ADD[31:24]							
0x0368	USBHS_DEVDMACONTROL7	7:0	BURST_LCK	DESC_LD_IT	END_BUFFIT	END_TR_IT	END_B_EN	END_TR_EN	LDNXT_DSC	CHANN_ENB
		15:8								
		23:16	BUFF_LENGTH[7:0]							
		31:24	BUFF_LENGTH[15:8]							
0x036C	USBHS_DEVDMASTATUS7	7:0		DESC_LDST	END_BF_ST	END_TR_ST			CHANN_ACT	CHANN_ENB
		15:8								
		23:16	BUFF_COUNT[7:0]							
		31:24	BUFF_COUNT[15:8]							
0x0370 ... 0x03FF	Reserved									
0x0400	USBHS_HSTCTRL	7:0								
		15:8			SPDCONF[1:0]			RESUME	RESET	SOFE
		23:16								
		31:24								
0x0404	USBHS_HSTISR	7:0		HWUPI	HSOFI	RXRSMI	RSMEDI	RSTI	DDISCI	DCONNI
		15:8	PEP_7	PEP_6	PEP_5	PEP_4	PEP_3	PEP_2	PEP_1	PEP_0
		23:16							PEP_9	PEP_8
		31:24	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	DMA_0	
0x0408	USBHS_HSTICR	7:0		HWUPIC	HSOFIC	RXRSMIC	RSMEDIC	RSTIC	DDISCIC	DCONNIC
		15:8								
		23:16								
		31:24								
0x040C	USBHS_HSTIFR	7:0		HWUPIS	HSOFIS	RXRSMIS	RSMEDIS	RSTIS	DDISCIS	DCONNIS
		15:8								
		23:16								
		31:24	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	DMA_0	
0x0410	USBHS_HSTIMR	7:0		HWUPIE	HSOFIE	RXRSMIE	RSMEDIE	RSTIE	DDISCIE	DCONNIE
		15:8	PEP_7	PEP_6	PEP_5	PEP_4	PEP_3	PEP_2	PEP_1	PEP_0
		23:16							PEP_9	PEP_8
		31:24	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	DMA_0	
0x0414	USBHS_HSTIDR	7:0		HWUPIEC	HSOFIEC	RXRSMIEC	RSMEDIEC	RSTIEC	DDISCIEC	DCONNIEC
		15:8	PEP_7	PEP_6	PEP_5	PEP_4	PEP_3	PEP_2	PEP_1	PEP_0
		23:16							PEP_9	PEP_8
		31:24	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	DMA_0	
0x0418	USBHS_HSTIER	7:0		HWUPIES	HSOFIES	RXRSMIES	RSMEDIES	RSTIES	DDISCIES	DCONNIES
		15:8	PEP_7	PEP_6	PEP_5	PEP_4	PEP_3	PEP_2	PEP_1	PEP_0
		23:16							PEP_9	PEP_8
		31:24	DMA_6	DMA_5	DMA_4	DMA_3	DMA_2	DMA_1	DMA_0	
0x041C	USBHS_HSTPIP	7:0	PEN7	PEN6	PEN5	PEN4	PEN3	PEN2	PEN1	PEN0
		15:8								PEN8
		23:16	PRST7	PRST6	PRST5	PRST4	PRST3	PRST2	PRST1	PRST0

39.6.26 Device Endpoint Interrupt Enable Register (Isochronous Endpoints)

Name: USBHS_DEVEPTIERx (ISOENPT)
Offset: 0x01F0 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

This register view is relevant only if EPTYPE = 0x1 in "Device Endpoint x Configuration Register".

For additional information, see "Device Endpoint x Mask Register (Isochronous Endpoints)".

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Clears the corresponding bit in USBHS_DEVEPTIMRx.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
						RSTDTS		EPDISHDMAS
Access								
Reset						0		0

Bit	15	14	13	12	11	10	9	8
		FIFOCONS	KILLBKS	NBUSYBKES		ERRORTRANSES	DATAXES	MDATAES
Access								
Reset		0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
	SHORTPACKETES	CRCERRES	OVERFES	HBISOFLUSHES	HBISOINERRES	UNDERFES	RXOUTES	TXINES
Access								
Reset	0	0	0	0	0	0	0	0

Bit 18 – RSTDTS Reset Data Toggle Enable

Bit 16 – EPDISHDMAS Endpoint Interrupts Disable HDMA Request Enable

Bit 14 – FIFOCONS FIFO Control

Bit 13 – KILLBKS Kill IN Bank

Bit 12 – NBUSYBKES Number of Busy Banks Interrupt Enable

Bit 10 – ERRORTRANSES Transaction Error Interrupt Enable

39.6.31 Host General Control Register

Name: USBHS_HSTCTRL
Offset: 0x0400
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
			SPDCONF[1:0]			RESUME	RESET	SOFE
Access								
Reset			0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 13:12 – SPDCONF[1:0] Mode Configuration
This field contains the host speed capability:.

Value	Name	Description
0	NORMAL	The host starts in Full-speed mode and performs a high-speed reset to switch to High-speed mode if the downstream peripheral is high-speed capable.
1	LOW_POWER	For a better consumption, if high speed is not needed.
2	HIGH_SPEED	Forced high speed.
3	FORCED_FS	The host remains in Full-speed mode whatever the peripheral speed capability.

Bit 10 – RESUME Send USB Resume
This bit is cleared when the USB Resume has been sent or when a USB reset is requested.

This bit should be written to one only when the start of frame generation is enabled (SOFE = 1).

Value	Description
0	No effect.
1	Generates a USB Resume on the USB bus.

Value	Name	Description
6	BOR	Boot Operation Request. Start a boot operation mode, the host processor can read boot data from the MMC device directly.
7	EBO	End Boot Operation. This command allows the host processor to terminate the boot operation mode.

Bits 7:6 – RSPTYP[1:0] Response Type

Value	Name	Description
0	NORESP	No response
1	48_BIT	48-bit response
2	136_BIT	136-bit response
3	R1B	R1b response type

Bits 5:0 – CMDNB[5:0] Command Number
This is the command index.

41.8.7 SPI Interrupt Disable Register

Name: SPI_IDR
Offset: 0x18
Reset: –
Property: Write-only

This register can only be written if the WPITEN bit is cleared in the SPI Write Protection Mode Register.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
						UNDES	TXEMPTY	NSSR
Access						W	W	W
Reset						–	–	–

Bit	7	6	5	4	3	2	1	0
					OVRES	MODF	TDRE	RDRF
Access					W	W	W	W
Reset					–	–	–	–

Bit 10 – UNDES Underrun Error Interrupt Disable

Bit 9 – TXEMPTY Transmission Registers Empty Disable

Bit 8 – NSSR NSS Rising Interrupt Disable

Bit 3 – OVRES Overrun Error Interrupt Disable

Bit 2 – MODF Mode Fault Error Interrupt Disable

Bit 1 – TDRE SPI Transmit Data Register Empty Interrupt Disable

Bit 0 – RDRF Receive Data Register Full Interrupt Disable

Figure 43-23. TWIHS Read Operation with Multiple Data Bytes with or without Internal Address

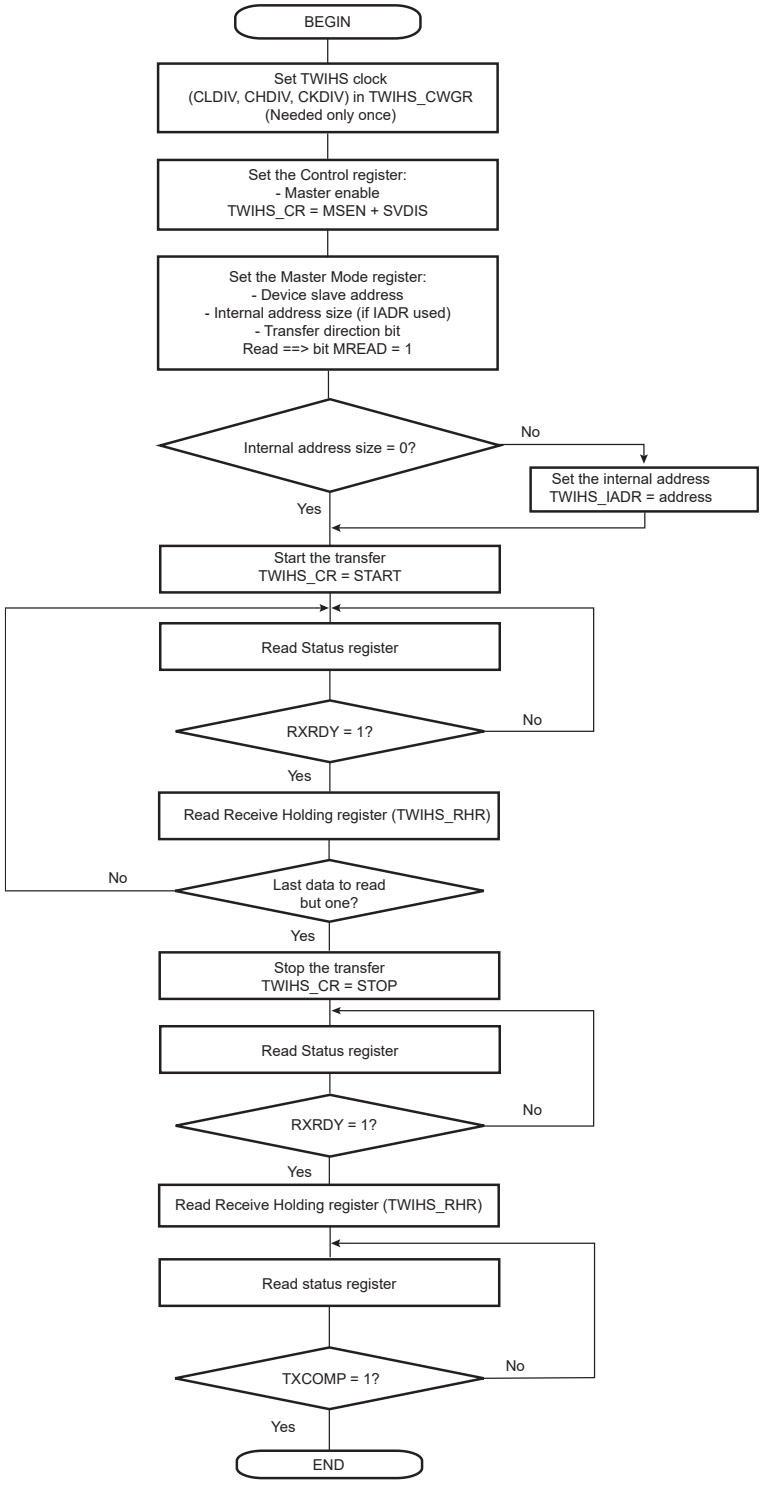
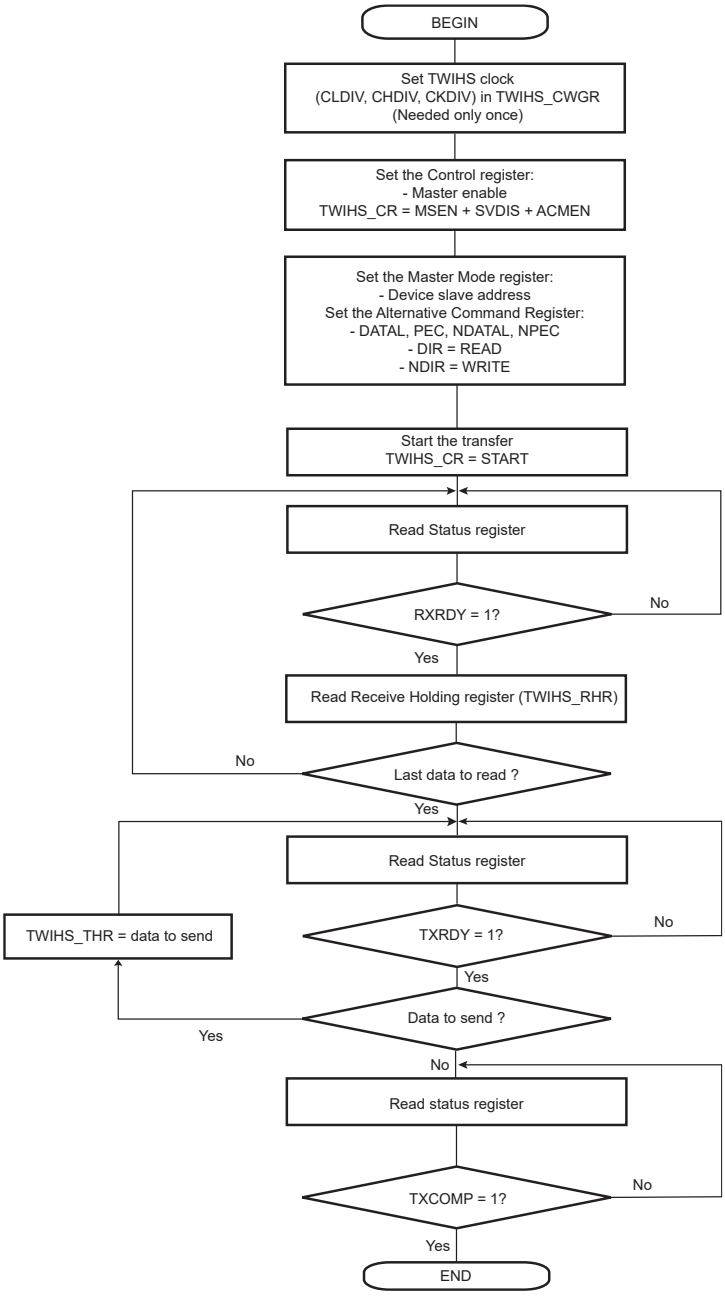


Figure 43-27. TWIHS Read Operation with Multiple Data Bytes + Write with Alternative Command Mode with PEC



43.6.4 Multimaster Mode

43.6.4.1 Definition

In Multimaster mode, more than one master may handle the bus at the same time without data corruption by using arbitration.

46.7.29 USART Number of Errors Register

Name: US_NER
Offset: 0x0044
Reset: 0x0
Property: Read-only

This register is relevant only if USART_MODE = 0x4 or 0x6 in the USART Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

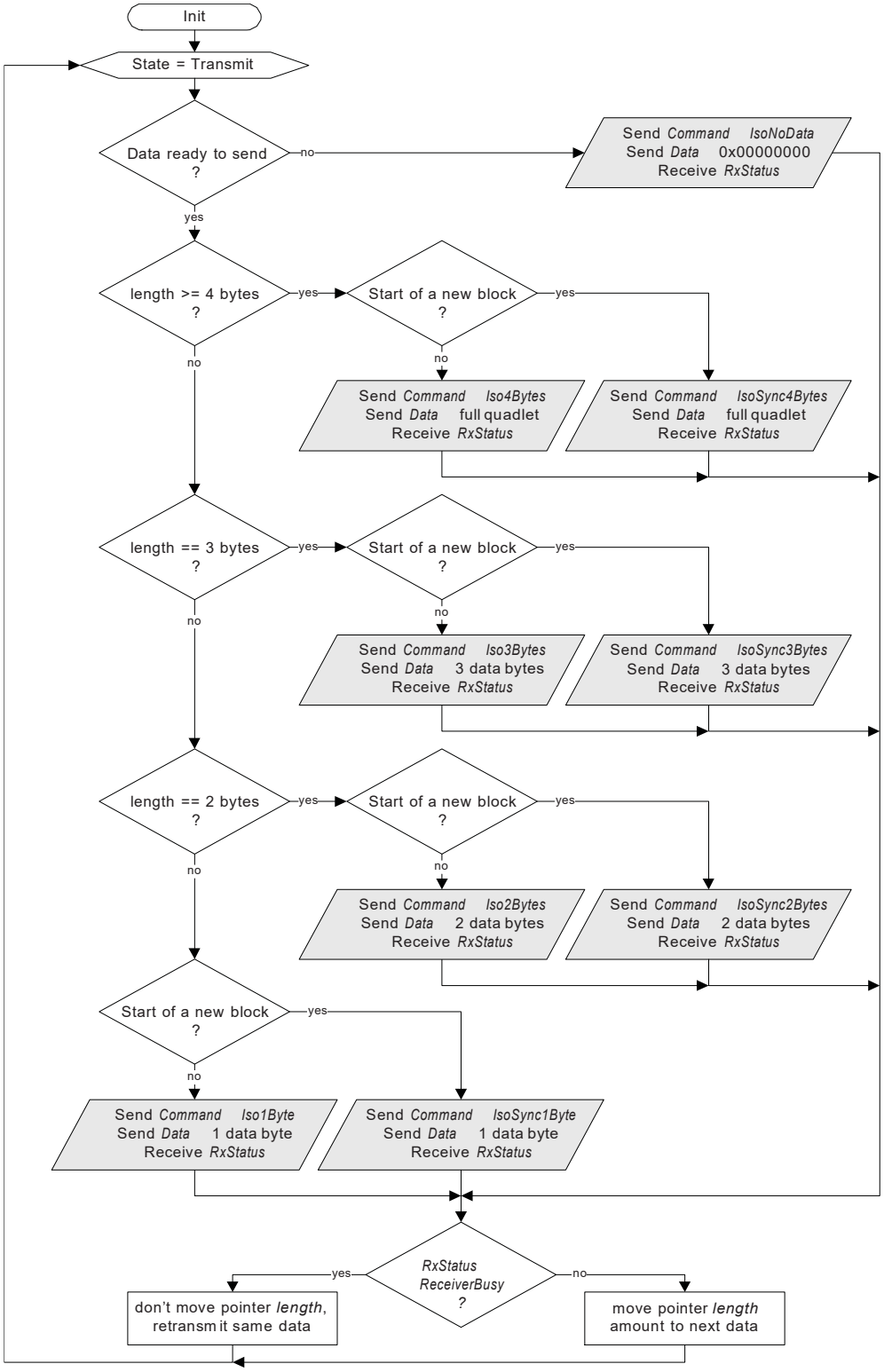
Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	NB_ERRORS[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – NB_ERRORS[7:0] Number of Errors
Total number of errors that occurred during an ISO7816 transfer. This register automatically clears when read.

Figure 48-14. Isochronous Data Tx Device Protocol



53.7.4 DACC Channel Enable Register

Name: DACC_CHER
Offset: 0x10
Reset: –
Property: Write-only

This register can only be written if the WPEN bit is cleared in the DACC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							CH1	CH0
Access							W	W
Reset							0	–

Bits 0, 1 – CHx Channel x Enable

Value	Description
0	No effect.
1	Enables the corresponding channel.

55.5.2.4 ICM Region Next Address Structure Member

Name: ICM_RNEXT
Property: Read/Write

Register offset is calculated as ICM_DSCR+0x00C+RID*(0x10).

Bit	31	30	29	28	27	26	25	24
	NEXT[29:22]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	23	22	21	20	19	18	17	16
	NEXT[21:14]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	15	14	13	12	11	10	9	8
	NEXT[13:6]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	NEXT[5:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset								

Bits 31:2 – NEXT[29:0] Region Transfer Descriptor Next Address
When configured to 0, this field indicates that the current descriptor is the last descriptor of the Secondary List, otherwise it points at a new descriptor of the Secondary List.

55.5.3 ICM Hash Area

The ICM Hash Area is a contiguous area of system memory that the controller and the processor can access. The physical location is configured in the ICM hash area start address register. This address is a multiple of 128 bytes. If the CDWBN bit of the context register is cleared (i.e., Write Back activated), the ICM performs a digest write operation at the following starting location: *(ICM_HASH) + (RID<<5), where RID is the current region context identifier. If the CDWBN bit of the context register is set (i.e., Digest Comparison activated), the ICM performs a digest read operation at the same address.

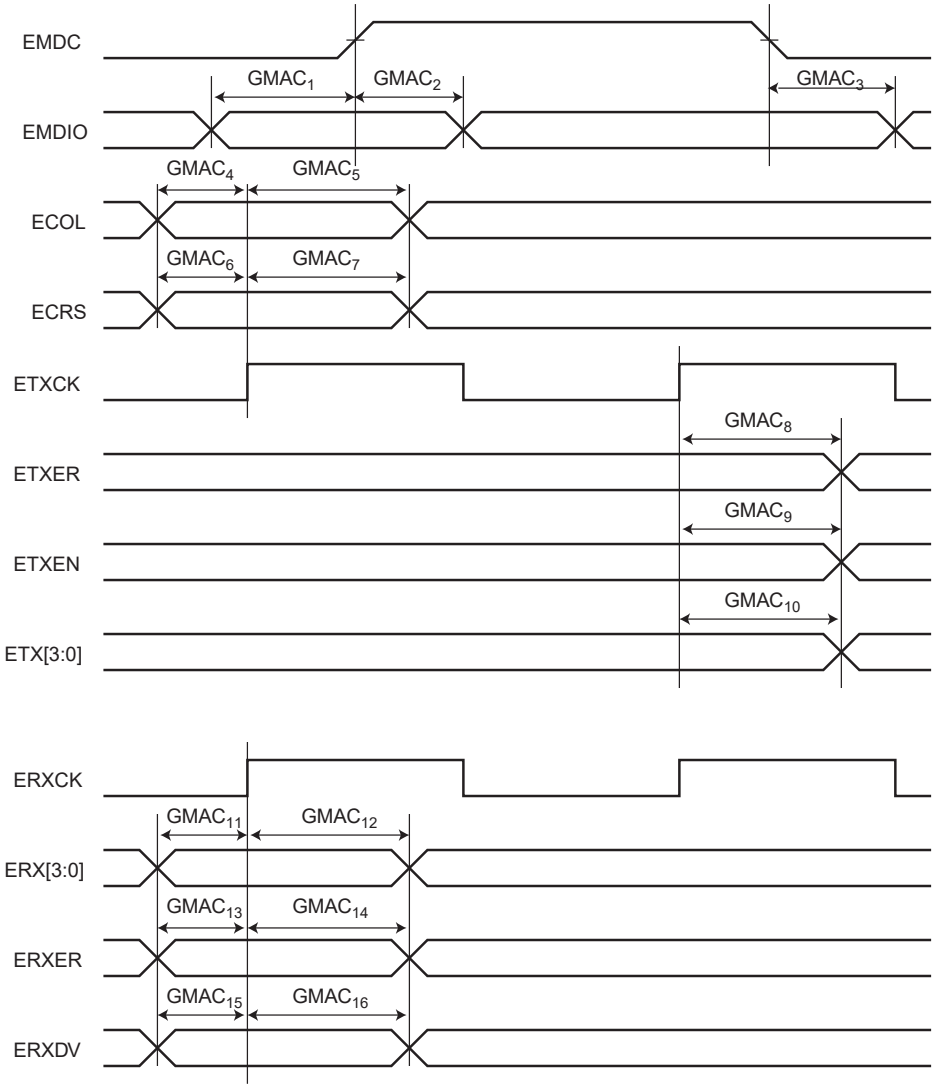
55.5.3.1 Message Digest Example

Considering the following 512-bit message (example given in FIPS 180-2):

“61626380018”

The message is written to memory in a Little Endian (LE) system architecture.

Figure 59-31. GMAC MII Mode Signals



59.13.1.13.4 RMII Mode

Table 59-72. GMAC RMII Mode Timings

Symbol	Parameter	Min	Max	Unit
$GMAC_{21}$	ETXEN toggling from EREFCK rising	2	16	ns
$GMAC_{22}$	ETX toggling from EREFCK rising	2	16	
$GMAC_{23}$	Setup for ERX from EREFCK rising	4	–	
$GMAC_{24}$	Hold for ERX from EREFCK rising	2	–	
$GMAC_{25}$	Setup for ERXER from EREFCK rising	4	–	
$GMAC_{26}$	Hold for ERXER from EREFCK rising	2	–	
$GMAC_{27}$	Setup for ECRSDV from EREFCK rising	4	–	
$GMAC_{28}$	Hold for ECRSDV from EREFCK rising	2	–	

Date	Changes
	AFEC_TEMPCWR. Section 52.7.2 ”AFEC Mode Register”: updated TRACKTIM description.
	Section 53. ”Digital-to-Analog Converter Controller (DACC)” Table 53-1 “DACC Signal Description” : corrected pin names to VREFP and VREFN (were ADVREFP and ADVREFN).
	Section 54. ”Analog Comparator Controller (ACC)” Table 54-1 “ACC Signal Description” : modified Description for DAC0, DAC1 signals. Section 54.7.7 ”ACC Analog Control Register”: updated HYST definition.
	Section 57. ”Advanced Encryption Standard (AES)” Section 57.2 ”Embedded Characteristics”: replaced “12/14/16 Clock Cycles Encryption/Decryption Processing Time...” with “10/12/14 Clock Cycles Encryption/Decryption Inherent Processing Time...”.
	Section 58. ”Electrical Characteristics” Table 58-3 “DC Characteristics” : removed Note 2 on current injection. Table 58-4 “DC Characteristics” : voltage input level defined for the RST and TEST I/O types. Updated max values for IIL and IIH. Updated Table 58-15 “Typical Current Consumption in Wait Mode” . Table 58-30 “VREFP Electrical Characteristics” : updated V_{VREFP} parameter values. Added new Table 58-34 “AFE INL and DNL, fAFE Clock =<20 MHz max, IBCTL=10” and Table 58-35 “AFE INL and DNL, fAFE Clock >20 MHz to 40 MHz, IBCTL=11” . Inserted new Table 58-36 “AFE Offset and Gain Error, VVREFP = 1.7V to 3.3V” . Updated Table 58-40 “DAC Static Performances (1)” . Updated Table 58-46 “Static Performance Characteristics” Added Section 58.13.1.10: “USART in Asynchronous Mode”.
	Section 62. ”Ordering Information” Added Note (2) on availability.
	Section 63. ”Errata” Added: - Section 63.1.16 ”Universal Synchronous Asynchronous Receiver Transmitter (USART)”: “Bad frame detection issue” - Section 63.2.4 ”ARM Cortex-M7”: “All issues related to the ARM r1p1 core are described on the ARM site” - Section 63.2.6 ”Inter-IC Sound Controller (I2SC)”: “I2SC first sent data corrupted” - Section 63.2.12 ”Universal Synchronous Asynchronous Receiver Transmitter (USART)”: “Bad frame detection issue” Deleted: