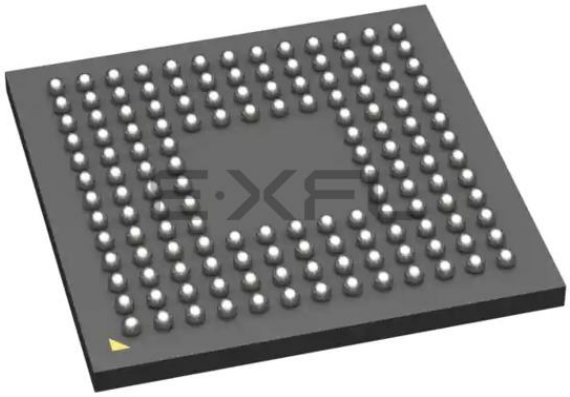

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70q19a-cfn

Offset	Name	Bit Pos.								
		31:24								
0x2C	RTC_VER	7:0					NVCALALR	NVTIMALR	NVCAL	NVTIM
		15:8								
		23:16								
		31:24								

32.6.1.43 PIO Rising Edge/High-Level Select Register

Name: PIO_REHLSR
Offset: 0x00D4
Property: Write-only

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Rising Edge/High-Level Interrupt Selection

Value	Description
0	No effect.
1	The interrupt source is set to a rising edge detection or high-level detection event, depending on PIO_ELSR.

Offset	Name	Bit Pos.								
		23:16	COMPVAL[7:0]							
		31:24	COMPVAL[15:8]							
0x073C	GMAC_ST2CW17	7:0	OFFSSTRT[0:0]	OFFSVAL[6:0]						
		15:8								OFFSSTRT[1:1]
		23:16								
		31:24								
0x0740	GMAC_ST2CW08	7:0	MASKVAL[7:0]							
		15:8	MASKVAL[15:8]							
		23:16	COMPVAL[7:0]							
		31:24	COMPVAL[15:8]							
0x0744	GMAC_ST2CW18	7:0	OFFSSTRT[0:0]	OFFSVAL[6:0]						
		15:8								OFFSSTRT[1:1]
		23:16								
		31:24								
0x0748	GMAC_ST2CW09	7:0	MASKVAL[7:0]							
		15:8	MASKVAL[15:8]							
		23:16	COMPVAL[7:0]							
		31:24	COMPVAL[15:8]							
0x074C	GMAC_ST2CW19	7:0	OFFSSTRT[0:0]	OFFSVAL[6:0]						
		15:8								OFFSSTRT[1:1]
		23:16								
		31:24								
0x0750	GMAC_ST2CW010	7:0	MASKVAL[7:0]							
		15:8	MASKVAL[15:8]							
		23:16	COMPVAL[7:0]							
		31:24	COMPVAL[15:8]							
0x0754	GMAC_ST2CW110	7:0	OFFSSTRT[0:0]	OFFSVAL[6:0]						
		15:8								OFFSSTRT[1:1]
		23:16								
		31:24								
0x0758	GMAC_ST2CW011	7:0	MASKVAL[7:0]							
		15:8	MASKVAL[15:8]							
		23:16	COMPVAL[7:0]							
		31:24	COMPVAL[15:8]							
0x075C	GMAC_ST2CW111	7:0	OFFSSTRT[0:0]	OFFSVAL[6:0]						
		15:8								OFFSSTRT[1:1]

38.8.20 GMAC Hash Register Bottom

Name: GMAC_HRB
Offset: 0x080
Reset: 0x00000000
Property: Read/Write

The unicast hash enable (UNIHEN) and the multicast hash enable (MITIHEN) bits in the Network Configuration Register (GMAC_NCFGR) enable the reception of hash matched frames.

Bit	31	30	29	28	27	26	25	24
	ADDR[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ADDR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ADDR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ADDR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ADDR[31:0] Hash Address
The first 32 bits of the Hash Address Register.

Value	Description
0	Cleared when USBHS_HSTPIPICR.SHORTPACKETIC = 1.
1	Set when a short packet is received by the host controller (packet length inferior to the PSIZE programmed field).

Bit 6 – RXSTALLDI Received STALLed Interrupt

Value	Description
0	Cleared when USBHS_HSTPIPICR.RXSTALLDIC = 1.
1	Set when a STALL handshake has been received on the current bank of the pipe. The pipe is automatically frozen. This triggers an interrupt if USBHS_HSTPIPIMR.RXSTALLE = 1.

Bit 5 – OVERFI Overflow Interrupt

Value	Description
0	Cleared when USBHS_HSTPIPICR.OVERFIC = 1.
1	Set when the current pipe has received more data than the maximum length of the current pipe. An interrupt is triggered if the USBHS_HSTPIPIMR.OVERFIE bit = 1.

Bit 4 – NAKEDI NAKed Interrupt

Value	Description
0	Cleared when USBHS_HSTPIPICR.NAKEDIC = 1.
1	Set when a NAK has been received on the current bank of the pipe. This triggers an interrupt if the USBHS_HSTPIPIMR.NAKEDE bit = 1.

Bit 3 – PERRI Pipe Error Interrupt

Value	Description
0	Cleared when the error source bit is cleared.
1	Set when an error occurs on the current bank of the pipe. This triggers an interrupt if the USBHS_HSTPIPIMR.PERRE bit is set. Refer to the USBHS_HSTPIPERRx register to determine the source of the error.

Bit 2 – UNDERFI Underflow Interrupt
This bit is set, for an isochronous and interrupt IN/OUT pipe, when an error flow occurs. This triggers an interrupt if UNDERFIE = 1.

This bit is set, for an isochronous or interrupt OUT pipe, when a transaction underflow occurs in the current pipe (the pipe cannot send the OUT data packet in time because the current bank is not ready). A zero-length-packet (ZLP) is sent instead.

This bit is set, for an isochronous or interrupt IN pipe, when a transaction flow error occurs in the current pipe, i.e, the current bank of the pipe is not free while a new IN USB packet is received. This packet is not stored in the bank. For an interrupt pipe, the overflowed packet is ACKed to comply with the USB standard.

This bit is cleared when USBHS_HSTPIPICR.UNDERFIEC = 1.

Bit 1 – TXOUTI Transmitted OUT Data Interrupt

Figure 43-21. TWIHS Read Operation with Single Data Byte without Internal Address

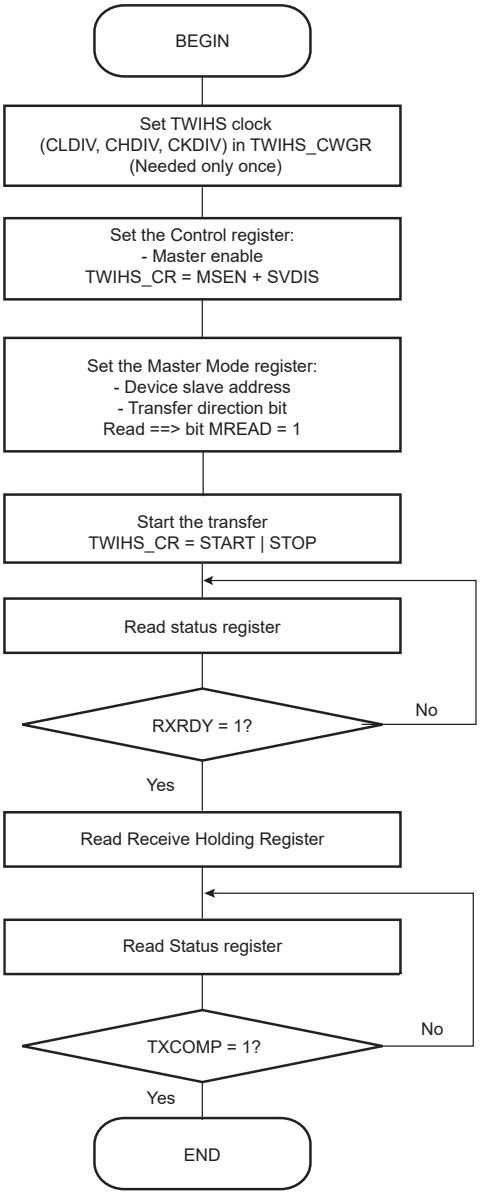
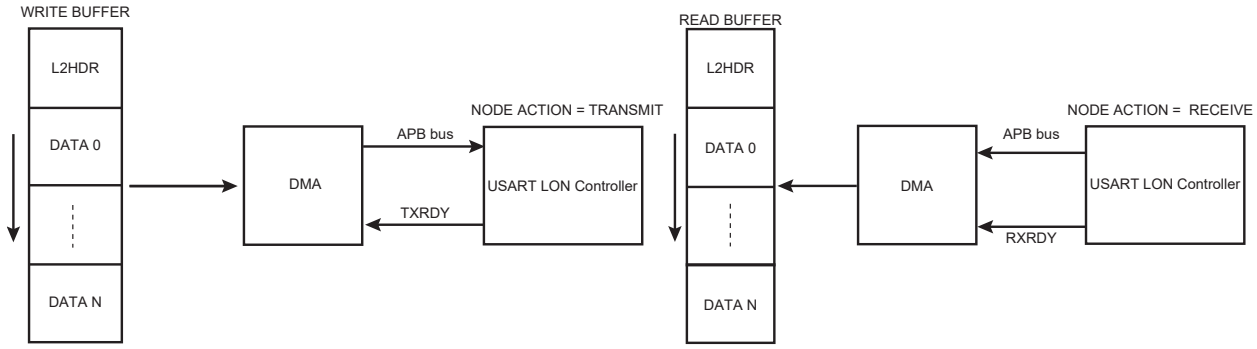


Figure 46-64. DMAM = 0



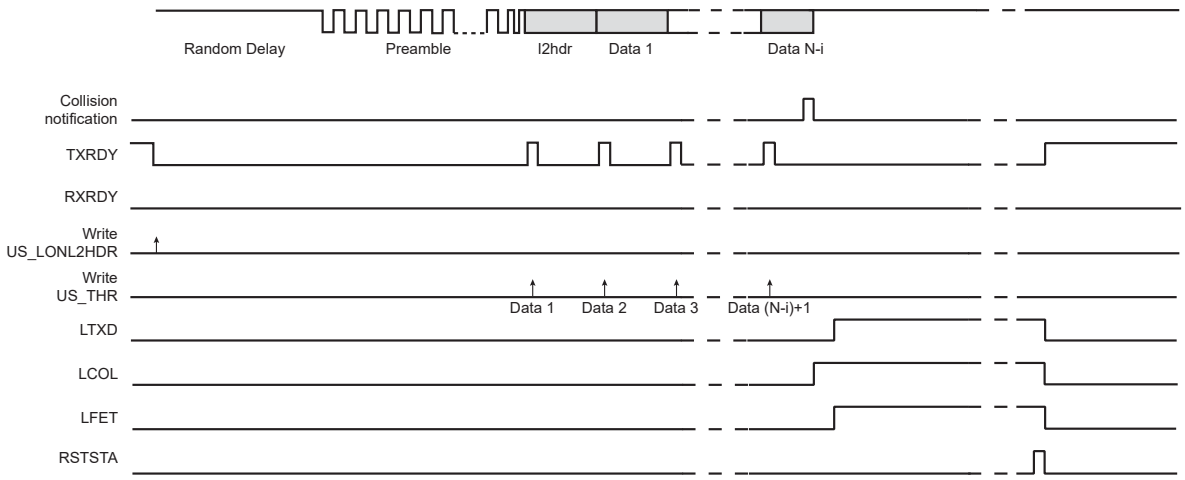
46.6.10.12.2 DMA and Collision Detection

As explained in "comm_type", depending on LON configuration the transmission may be terminated early upon collision notification which means that the DMA transfer may be stopped before its end.

In case of early end of transmission due to collision detection the USART in LON mode acts as follows:

- Send the end of frame trigger.
- Hold down TXRDY avoiding thus any additional DMA transfer.
- Set LTXD, LCOL and LFET flags in US_CSR.
- Wait that the application reconfigure the DMA.
- Wait until LCOL and LFET flags are cleared through US_CR. RSTSTA (it releases the TXRDY signal).

Figure 46-65. DMA, Collision and Early Frame Termination



46.6.11 Test Modes

The USART can be programmed to operate in three different test modes. The internal loopback capability allows on-board diagnostics. In Loopback mode, the USART interface pins are disconnected or not and reconfigured for loopback internally or externally.

46.6.11.1 Normal Mode

Normal mode connects the RXD pin on the receiver input and the transmitter output on the TXD pin.

Bit 9 – TXEMPTY TXEMPTY Interrupt Mask

Bit 8 – TIMEOUT Timeout Interrupt Mask

Bit 7 – PARE Parity Error Interrupt Mask

Bit 6 – FRAME Framing Error Interrupt Mask

Bit 5 – OVRE Overrun Error Interrupt Mask

Bit 2 – RXBRK Receiver Break Interrupt Mask

Bit 1 – TXRDY TXRDY Interrupt Mask

Bit 0 – RXRDY RXRDY Interrupt Mask

MediaLB Devices are encouraged to support dynamic configuration, where a preset DeviceAddress is used to assign the ChannelAddresses for each logical channel. Dynamic configuration avoids collisions of ChannelAddresses on different Devices.

To minimize collisions of DeviceAddresses, programmable Devices should assign the DeviceAddress via firmware. For non-programmable Devices, it is strongly recommended to have only the upper bits fixed, and have the lower bits configurable via pins on the Device. Having the lower bits configurable via pins minimizes collisions with other manufacturer's Devices, as well as allows multiple instances of the same Device to coexist on the same MediaLB bus.

Table 48-4. DeviceAddress Grouping

Device Addresses	Range	Device Type
0x0002..0x017E	–	Reserved
0x0180..0x0186	4	External Host Controller Processors
0x0188..0x018E	4	General Processors
0x0190..0x0196	–	Reserved
0x0198..0x019E	–	Reserved
0x01A0..0x01A6	4	Digital Signal Processors
0x01A8..0x01AE	–	Reserved
0x01B0..0x01B6	4	Decoder Chips
0x01B8..0x01BE	–	Reserved
0x01C0..0x01C6	4	Encoder Chips
0x01C8..0x01CE	–	Reserved
0x01D0..0x01DE	8	Digital-to-Analog Converters (DACs)
0x01E0..0x01E6	–	Reserved
0x01E8..0x01EE	–	Reserved
0x01F0..0x01FC	7	Analog-to-Digital Converters (ADCs)

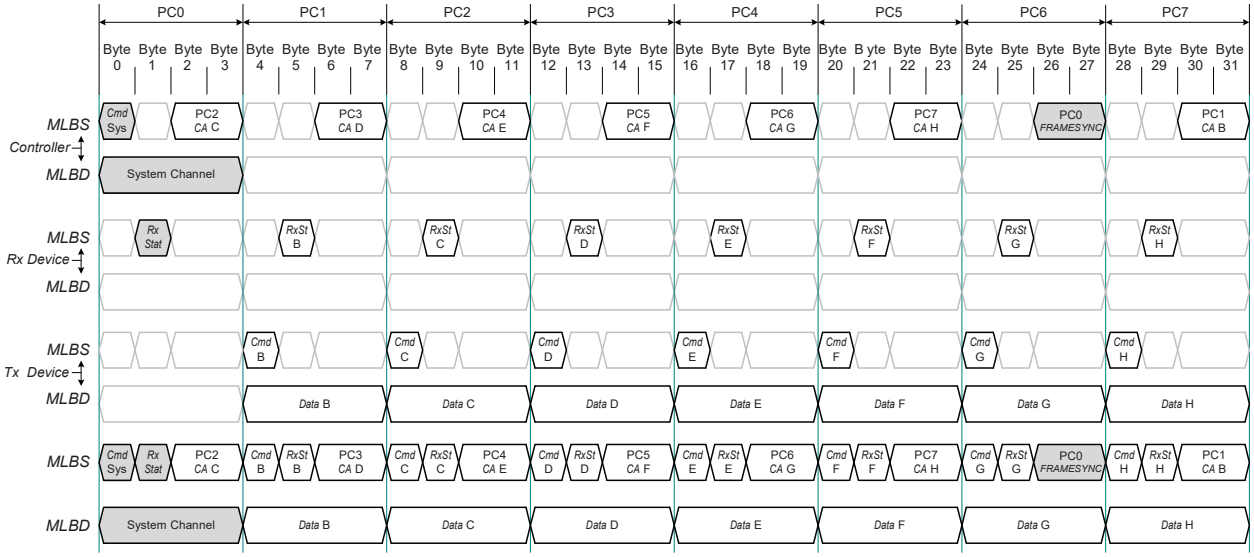
48.6.1.3 Command Bytes

The MediaLB Command field is eight-bits wide and all odd values are reserved; therefore, the LSB of Command is always zero.

Transmitting MediaLB Devices (including the Controller) place Command on the MLBS line to indicate the type of data being transmitted on the MLBD line.

Two types of MediaLB commands are defined: Normal and System. Normal commands are those sent by the transmitting MediaLB Device (or Controller) in non-System Channels. System commands are those sent by the MediaLB Controller in the System Channel.

Figure 48-5. 3-pin MediaLB 256Fs Interface Example



48.6.1.7 Initialization

At power up, the MediaLB Controller might output a MLBReset command in the System Channel (all System commands are optional). Upon reception of the MLBReset command, all MediaLB Devices will cancel any current transmissions or receptions and clear their buffers.

Two scenarios are supported to configure MediaLB Devices and ChannelAddresses:

- Static pre-configured before startup. The system implementor decides which ChannelAddresses are to be used for every communication path on MediaLB. This static MediaLB configuration can be communicated by the EHC to the Controller through pre-defined power-up logical channels or through a secondary port.
- Dynamically at run-time. Dynamic configuration allows the board designer to support multiple build options where the EHC can query to find out if a particular Device is present or not on a particular board. The EHC instructs the Controller to scan for a particular DeviceAddress in the System Channel. The Controller uses the MLBScan command to look for a Device. The Controller then notifies the EHC whether the Device is present or not. If the Device is present, then the EHC can instruct the Controller to set the ChannelAddresses for the Device found. The EHC sends messages to the Controller to set each Indices/Logical channel, and waits the appropriate amount of time between each message as specified in the Devices documentation. When that particular Device is configured, the EHC can instruct the Controller to scan for the next Device.

Since the MediaLB Controller is the interface between the MediaLB Devices and the MOST Network, the Controller provides the MLBC signal and will also continue to operate even when the MOST Network is unlocked. When no activity exists on MediaLB, the Controller can shut off the MLBC placing MediaLB in a low-power state. The ChannelAddress assignments are not affected in low-power state; therefore, the same communication paths exists once MLBC is restarted.

MediaLB Devices are synchronously slaved to the MediaLB Controller through the MLBC signal. Since the Controller is synchronized to the MOST Network, the MLBC signal provides Network synchronization to all MediaLB Devices. Once the Controller starts up MLBC, all MediaLB Devices must synchronize to the MediaLB frame before communication can commence. When not frame-locked, Devices must search for the FRAMESYNC pattern, which defines a byte and physical channel boundary. Additionally, the start of the MediaLB frame (PC0) occurs one quadlet after FRAMESYNC is present on the bus. Even when a

49.5.7.3 Tx Buffer Element

The Tx Buffers section can be configured to hold dedicated Tx Buffers as well as a Tx FIFO / Tx Queue. In case that the Tx Buffers section is shared by dedicated Tx buffers and a Tx FIFO / Tx Queue, the dedicated Tx Buffers start at the beginning of the Tx Buffers section followed by the buffers assigned to the Tx FIFO or Tx Queue. The Tx Handler distinguishes between dedicated Tx Buffers and Tx FIFO / Tx Queue by evaluating the Tx Buffer configuration TXBC.TFQS and TXBC.NDTB. The element size can be configured for storage of CAN FD messages with up to 64 bytes data field via register TXESC.

Table 49-8. Tx Buffer Element

	31			24	23				16	15	8	7	0
T0	ESI	XTD	RTR	ID[28:0]									
T1	MM[7:0]				EFC	reserved	FDF	BRS	DLC[3:0]	reserved			
T2	DB3[7:0]				DB2[7:0]					DB1[7:0]		DB0[7:0]	
T3	DB7[7:0]				DB6[7:0]					DB5[7:0]		DB4[7:0]	
...	...				...					...		...	
Tn	DBm[7:0]				DBm-1[7:0]					DBm-2[7:0]		DBm-3[7:0]	

• T0 Bit 30 ESI: Error State Indicator

T0 Bit 31 ESI: Error State Indicator

0: ESI bit in CAN FD format depends only on error passive flag

1: ESI bit in CAN FD format transmitted recessive

Note: The ESI bit of the transmit buffer is or’ed with the error passive flag to decide the value of the ESI bit in the transmitted FD frame. As required by the CAN FD protocol specification, an error active node may optionally transmit the ESI bit recessive, but an error passive node will always transmit the ESI bit recessive. This feature can be used in gateway applications when a message from an error passive node is routed to another CAN network.

• T0 Bit 30 XTD: Extended Identifier

0: 11-bit standard identifier.

1: 29-bit extended identifier.

• T0 Bit 29 RTR: Remote Transmission Request

0: Transmit data frame.

1: Transmit remote frame.

Note: When RTR = 1, the MCAN transmits a remote frame according to ISO11898-1, even if MCAN_CCCR.FDOE enables the transmission in CAN FD format.

• T0 Bits 28:0 ID[28:0]: Identifier

Standard or extended identifier depending on bit XTD. A standard identifier has to be written to ID[28:18].

• T1 Bits 31:24 MM[7:0]: Message Marker

Written by processor during Tx Buffer configuration. Copied into Tx Event FIFO element for identification of Tx message status.

49.6.44 MCAN Transmit Buffer Cancellation Finished Interrupt Enable

Name: MCAN_TXBCIE
Offset: 0xE4
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	CFIE31	CFIE30	CFIE29	CFIE28	CFIE27	CFIE26	CFIE25	CFIE24
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CFIE23	CFIE22	CFIE21	CFIE20	CFIE19	CFIE18	CFIE17	CFIE16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

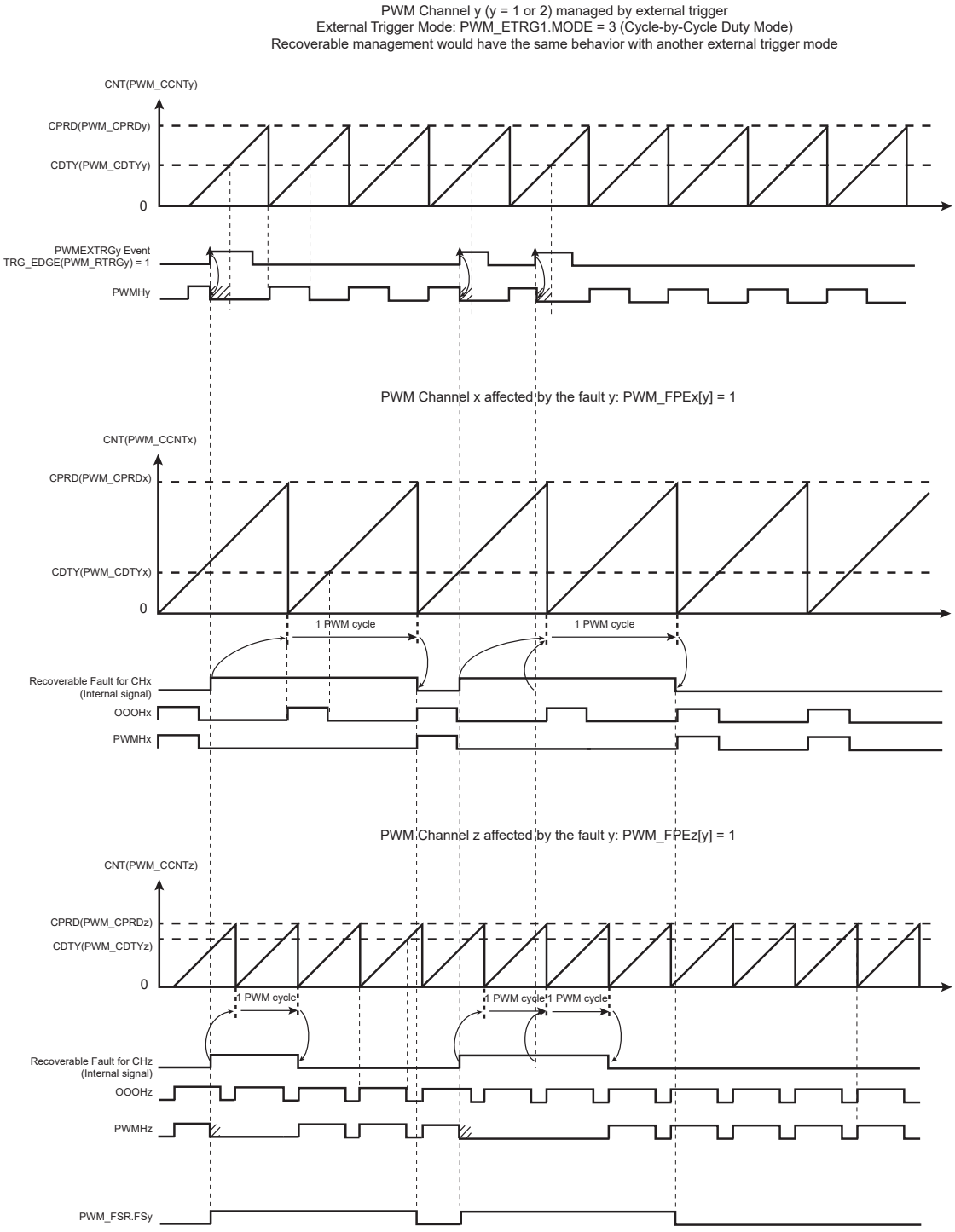
Bit	15	14	13	12	11	10	9	8
	CFIE15	CFIE14	CFIE13	CFIE12	CFIE11	CFIE10	CFIE9	CFIE8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CFIE7	CFIE6	CFIE5	CFIE4	CFIE3	CFIE2	CFIE1	CFIE0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – CFIEx Cancellation Finished Interrupt Enable for Transmit Buffer x
Each Transmit Buffer has its own Cancellation Finished Interrupt Enable bit.

Value	Description
0	Cancellation finished interrupt disabled.
1	Cancellation finished interrupt enabled.

Figure 51-17. Recoverable Fault Management



51.6.2.8 Spread Spectrum Counter

The PWM macrocell includes a spread spectrum counter allowing the generation of a constantly varying duty cycle on the output PWM waveform (only for the channel 0). This feature may be useful to minimize electromagnetic interference or to reduce the acoustic noise of a PWM driven motor.

This is achieved by varying the effective period in a range defined by a spread spectrum value which is programmed by the field SPRD in the PWM Spread Spectrum Register (PWM_SSPR). The effective

52.4 Signal Description

Table 52-1. AFEC Signal Description

Pin Name	Description
VREFP	Reference voltage
VREFN	Reference voltage
AFE_AD0—AFE_AD11(1)	Analog input channels
AFE_ADTRG	External trigger

Note:

1. AFE_AD11 is not an actual pin but is connected to a temperature sensor.

52.5 Product Dependencies

52.5.1 I/O Lines

The digital input AFE_ADTRG is multiplexed with digital functions on the I/O line and the selection of AFE_ADTRG is made using the PIO Controller.

The analog inputs AFE_ADx are multiplexed with digital functions on the I/O lines. AFE_ADx inputs are selected as inputs of the AFEC when writing a one in the corresponding CHx bit of AFEC_CHER and the digital functions are not selected.

52.5.2 Power Management

The AFEC is not continuously clocked. The programmer must first enable the AFEC peripheral clock in the Power Management Controller (PMC) before using the AFEC. However, if the application does not require AFEC operations, the peripheral clock can be stopped when not needed and restarted when necessary.

When the AFEC is in Sleep mode, the peripheral clock must always be enabled.

52.5.3 Interrupt Sources

The AFEC interrupt line is connected on one of the internal sources of the Interrupt Controller. Using the AFEC interrupt requires the interrupt controller to be programmed first.

52.5.4 Temperature Sensor

The temperature sensor is connected to Channel 11 of the AFEC.

The temperature sensor provides an output voltage V_T that is proportional to the absolute temperature (PTAT).

52.5.5 Timer Triggers

Timer Counters may or may not be used as hardware triggers depending on user requirements. Thus, some or all of the timer counters may be unconnected.

52.5.6 PWM Event Lines

PWM event lines may or may not be used as hardware triggers, depending on user requirements.

Value	Name	Description
0	DISABLED	One data to convert is written to the FIFO per access to DACC.
1	ENABLED	Two data to convert are written to the FIFO per access to DACC (reduces the number of requests to DMA and the number of system bus accesses).

Bits 0, 1 – MAXSx Max Speed Mode for Channel x

Value	Name	Description
0	TRIG_EVENT	Trigger mode or Free-running mode enabled. (See TRGENx.DACC_TRIGR.)
1	MAXIMUM	Max speed mode enabled.

Value	Description
0	Automatic monitoring mode is disabled.
1	The ICM passes through the Main List once to calculate the message digest of the monitored area. When WRAP = 1 in ICM_RCFG, the ICM begins monitoring.

Bits 7:4 – BBC[3:0] Bus Burden Control
This field is used to control the burden of the ICM system bus. The number of system clock cycles between the end of the current processing and the next block transfer is set to 2^{BBC}. Up to 32,768 cycles can be inserted.

Bit 2 – SLBDIS Secondary List Branching Disable

Value	Description
0	Branching to the Secondary List is permitted.
1	Branching to the Secondary List is forbidden. The NEXT field of the ICM_RNEXT structure member has no effect and is always considered as zero.

Bit 1 – EOMDIS End of Monitoring Disable

Value	Description
0	End of Monitoring is permitted.
1	End of Monitoring is forbidden. The EOM bit of the ICM_RCFG structure member has no effect.

Bit 0 – WBDIS Write Back Disable
When ASCD is set, WBDIS has no effect.

Value	Description
0	Write Back operations are permitted.
1	Write Back operations are forbidden. Context register CDWBN bit is internally set to one and cannot be modified by a linked list element. ICM_RCFG.CDWBN has no effect.

Bits 11:8 – RBE[3:0] Region Bus Error Interrupt Mask

Value	Description
0	When RBE[i] is set to zero, the interrupt is disabled for region i.
1	When RBE[i] is set to one, the interrupt is enabled for region i.

Bits 7:4 – RDM[3:0] Region Digest Mismatch Interrupt Mask

Value	Description
0	When RDM[i] is set to zero, the interrupt is disabled for region i.
1	When RDM[i] is set to one, the interrupt is enabled for region i.

Bits 3:0 – RHC[3:0] Region Hash Completed Interrupt Mask

Value	Description
0	When RHC[i] is set to zero, the interrupt is disabled for region i.
1	When RHC[i] is set to one, the interrupt is enabled for region i.

- N = 12 when KEYSIZE = 1
- N = 14 when KEYSIZE = 2

The processing time represents the number of clock cycles that the AES needs in order to perform one encryption/decryption.

Note: The best performance is achieved with PROCDLY equal to 0.

Bit 3 – DUALBUFF Dual Input Buffer

Value	Name	Description
0	INACTIVE	AES_IDATARx cannot be written during processing of previous block.
1	ACTIVE	AES_IDATARx can be written during processing of previous block when SMOD = 2. It speeds up the overall runtime of large files.

Bit 1 – GTAGEN GCM Automatic Tag Generation Enable

Value	Description
0	Automatic GCM Tag generation disabled.
1	Automatic GCM Tag generation enabled.

Bit 0 – CIPHER Processing Mode

Value	Description
0	Decrypts data.
1	Encrypts data.

Symbol	Parameter	Conditions			Min	Max	Unit
		Load	V_{DDIO}	Drive Level			
				High	–	55	
$PulseminH_1$	Pin Group 1 (1) High Level Pulse Width	10 pF	3.0V	High	6.1	9.2	ns
$PulseminL_1$	Pin Group 1 (1) Low Level Pulse Width	10 pF	3.0V	High	6.1	9.2	ns
FreqMax2	Pin Group 2 (2)Maximum output frequency	10 pF	3.0V	High	–	125	MHz
				Low	–	100	
$PulseminH_2$	Pin Group 2 (2) High Level Pulse Width	10 pF	3.0V	High	3.4	4.1	ns
$PulseminL_2$	Pin Group 2 (2) Low Level Pulse Width	10 pF	3.0V	High	3.4	4.1	ns
FreqMax3	Pin Group3(3) Maximum output frequency	30 pF	3.0V	High	–	75	MHz
				Low	–	50	
$PulseminH_3$	Pin Group 3 (3) High Level Pulse Width	30 pF	3.0V	High	6.0	7.3	ns
$PulseminL_3$	Pin Group 3 (3) Low Level Pulse Width	30 pF		High	6.0	7.3	ns
FreqMax4	Pin Group 4(4) Maximum output frequency	40 pF	3.0V	–	–	51	MHz
$PulseminH_4$	Pin Group 4(4) High Level Pulse Width	40 pF	3.0V	–	7.8	11.2	ns
$PulseminL_4$	Pin Group 4(4) Low Level Pulse Width	40 pF	3.0V	–	7.8	11.2	ns

Note:

1. Pin Group 1 = GPIO, CLOCK
2. Pin Group 2 = GPIO_CLK
3. Pin Group 3 = GPIO_AD
4. Pin Group 4 = GPIO_MLB

58.13.1.4 MediaLB Characteristics

The system has been constrained to achieve the timings in 256×Fs and 512×Fs in compliance with the MediaLB (MLB) specification.

Note: 1024×Fs timings are achieved under STH conditions only.

58.13.1.5 QSPI Characteristics

Figure 58-17. QSPI Master Mode with (CPOL= NCPHA = 0) or (CPOL= NCPHA= 1)