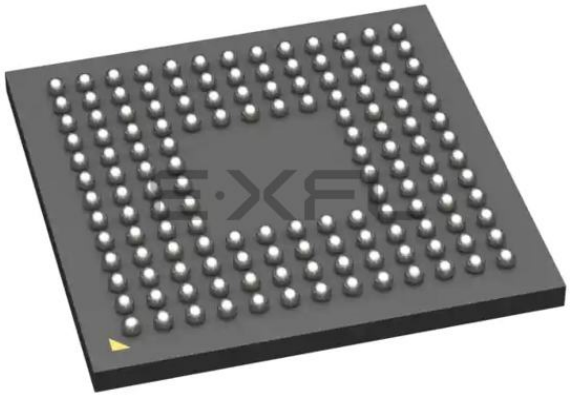

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Applications of "Embedded - Microcontrollers"

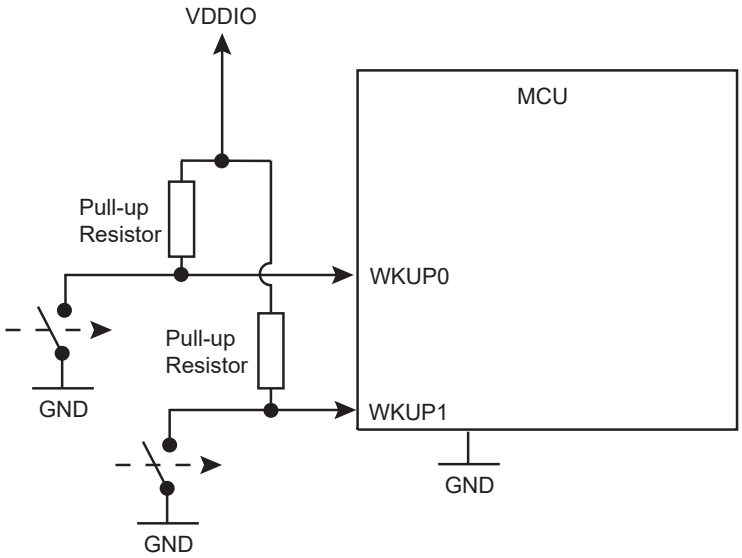
Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70q19a-cfnt

A debounce event (tamper detection) can perform an immediate clear (0 delay) on the first half the general-purpose backup registers (GPBR). SUPC_WUMR.LPDBCCLR bit must be set.

Note that it is not mandatory to use the RTCOUTx pin when using the WKUP0/WKUP1 pins as tampering inputs in any mode. Using the RTCOUTx pin provides a “sampling mode” to further reduce the power consumption of the tamper detection circuitry. If RTCOUTx is not used, the RTC must be configured to create an internal sampling point for the debouncer logic. The period of time between two samples can be configured by programming RTC_MR.TPERIOD.

The following figure illustrates the use of WKUPx without the RTCOUTx pin.

Figure 23-11. Using WKUP Pins Without RTCOUTx Pins



Related Links

27. Real-time Clock (RTC)

23.4.9.3 Clock Alarms

The RTC and the RTT alarms can generate a wakeup of the core power supply. This can be enabled by setting, respectively, SUPC_WUMR.RTCEN and SUPC_WUMR.RTTEN.

The Supply Controller does not provide any status as the information is available in the user interface of either the Real-Time Timer or the Real-Time Clock.

23.4.9.4 Supply Monitor Detection

The supply monitor can generate a wakeup of the core power supply. See "Supply Monitor".

23.4.10 Register Write Protection

To prevent any single software error from corrupting SYSC behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the ”System Controller Write Protection Mode Register” (SYSC_WPMR).

The following registers can be write-protected:

- RSTC Mode Register
- RTT Mode Register
- RTT Alarm Register
- RTC Control Register

31. Power Management Controller (PMC)

31.1 Description

The Power Management Controller (PMC) optimizes power consumption by controlling all system and user peripheral clocks. The PMC enables/disables the clock inputs to many of the peripherals and the Cortex-M7 processor.

The Supply Controller selects either the Slow RC oscillator or the 32.768 kHz crystal oscillator as the source of SLCK. The unused oscillator is disabled automatically so that power consumption is optimized.

By default, at startup, the chip runs out of MCK using the Main RC oscillator running at 12 MHz.

31.2 Embedded Characteristics

The Power Management Controller provides the following clocks:

- Master Clock (MCK), programmable from a few hundred Hz to the maximum operating frequency of the device. It is available to the modules running permanently, such as the Enhanced Embedded Flash Controller
- Processor Clock (HCLK), automatically switched off when entering the processor in Sleep mode
- Free-running processor Clock (FCLK)
- The Cortex-M7 SysTick external clock
- USB Clock (USB_48M), required by the USB peripheral
- Peripheral Clocks with independent ON/OFF control, provided to the peripherals
- Programmable Clock Outputs (PCKx), selected from the clock generator outputs to drive the device PCK pins
- Clock sources independent of MCK and HCLK, provided by internal PCKx for USART, UART, TC, Embedded Trace Macrocell (ETM) and CAN Clocks
- Generic Clock (GCLK) with controllable division and ON/OFF control, independent of MCK and HCLK. Provided to selected peripherals.

The Power Management Controller also provides the following features on clocks:

- A Main crystal oscillator failure detector
- A 32.768 kHz crystal oscillator frequency monitor
- A frequency counter on Main crystal oscillator or Main RC oscillator
- An on-the-fly adjustable Main RC oscillator frequency

31.20.31 PMC SleepWalking Disable Register 1

Name: PMC_SLPWK_DR1
Offset: 0x0138
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
		PID62		PID60	PID59	PID58	PID57	PID56
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
			PID53	PID52	PID51	PID50	PID49	PID48
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	PID47	PID46	PID45	PID44	PID43	PID42	PID41	PID40
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	PID39		PID37		PID35	PID34	PID33	PID32
Access								
Reset								

Bits 0:3,5,7:28,30 – PID Peripheral Clock x Disable

Value	Description
0	No effect.
1	Disables the corresponding peripheral clock.

33. External Bus Interface (EBI)

33.1 Description

The External Bus Interface (EBI) is designed to ensure the successful data transfer between several external devices and the embedded Memory Controller of an ARM-based device.

The Static Memory and SDRAM Controllers are all featured external Memory Controllers on the EBI. These external Memory Controllers are capable of handling several types of external memory and peripheral devices, such as SRAM, PROM, EPROM, EEPROM, Flash and SDR-SDRAM. The EBI operates with a 3.3V power supply

1.8V or

(VDDIO).

The EBI also supports the NAND Flash protocols via integrated circuitry that greatly reduces the requirements for external components. Furthermore, the EBI handles data transfers with up to six external devices, each assigned to six address spaces defined by the embedded Memory Controller. Data transfers are performed through a 16-bit or 32-bit data bus, an address bus of up to 24 bits, up to four chip select lines (NCS[3:0]) and several control pins that are generally multiplexed between the different external Memory Controllers.

33.2 Embedded Characteristics

- Integrates two External Memory Controllers
  - Static Memory Controller
  - SDR-SDRAM Controller
- Integrates NAND Flash Logic
- Up to 24-bit Address Bus (up to 16 Mbytes linear per chip select)
- Up to four Chip Selects, Configurable Assignment
  - Static Memory Controller on NCS0, NCS1, NCS2, NCS3
  - SDR-SDRAM Controller (SDCS) or Static Memory Controller on NCS1
  - NAND Flash support on NCS0, NCS1, NSCS2 and NCS3

34.7.11 SDRAMC OCMS Register

Name: SDRAMC_OCMS
Offset: 0x2C
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								SDR_SE
Access								R/W
Reset								0

Bit 0 – SDR_SE SDRAM Memory Controller Scrambling Enable

Value	Description
0	Disables off-chip scrambling for SDR-SDRAM access.
1	Enables off-chip scrambling for SDR-SDRAM access.

Bit 0 – CGDISREG Configuration Registers Clock Gating Disable

Value	Description
0	The automatic clock gating is enabled for the configuration registers.
1	The automatic clock gating is disabled for the configuration registers.

38.8.85 GMAC 1588 Timer Seconds Low Register

Name: GMAC_TSL
Offset: 0x1D0
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	TCS[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TCS[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TCS[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TCS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – TCS[31:0] Timer Count in Seconds
This register is writable. It increments by 1 when the IEEE 1588 nanoseconds counter counts to one second. It may also be incremented when the Timer Adjust Register is written.

Bit 6 – STALLEDEC STALLed Interrupt Clear

Bit 5 – OVERFEC Overflow Interrupt Clear

Bit 4 – NAKINEC NAKed IN Interrupt Clear

Bit 3 – NAKOUTEC NAKed OUT Interrupt Clear

Bit 2 – RXSTPEC Received SETUP Interrupt Clear

Bit 1 – RXOUTEC Received OUT Data Interrupt Clear

Bit 0 – TXINEC Transmitted IN Interrupt Clear

43.7.15 TWIHS Write Protection Mode Register

Name: TWIHS_WPMR
Offset: 0xE4
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	WPKEY[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	WPKEY[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	WPKEY[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
								WPEN
Access								R/W
Reset								0

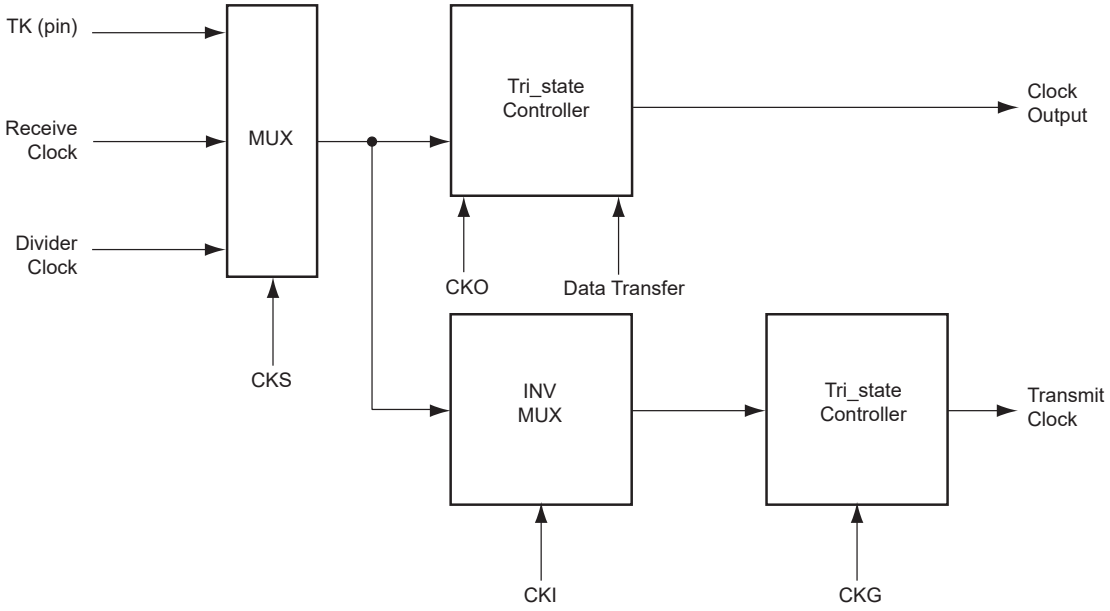
Bits 31:8 – WPKEY[23:0] Write Protection Key

Value	Name	Description
0x545749	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

Bit 0 – WPEN Write Protection Enable
See Register Write Protection for the list of registers that can be write-protected.

Value	Description
0	Disables the write protection if WPKEY corresponds to 0x545749 (“TWI” in ASCII).
1	Enables the write protection if WPKEY corresponds to 0x545749 (“TWI” in ASCII).

Figure 44-9. Transmit Clock Management

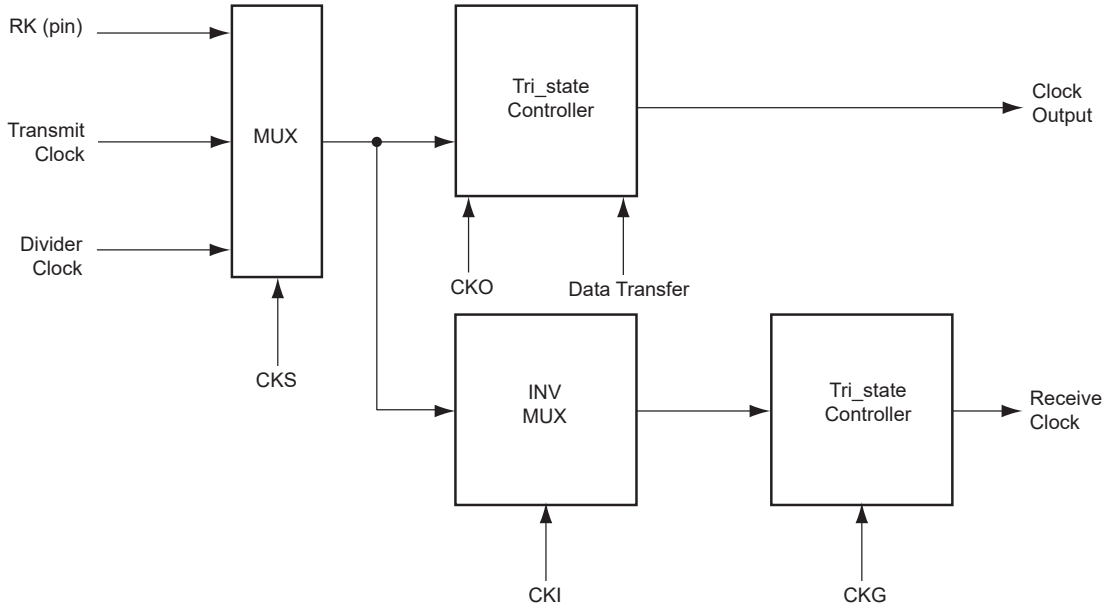


44.8.1.3 Receive Clock Management

The receive clock is generated from the transmit clock or the divider clock or an external clock scanned on the RK I/O pad. The Receive Clock is selected by the CKS field in SSC_RCMR (Receive Clock Mode Register). Receive Clocks can be inverted independently by the CKI bits in SSC_RCMR.

The receiver can also drive the RK I/O pad continuously or be limited to the current data transfer. The clock output is configured by the SSC_RCMR. The Receive Clock Inversion (CKI) bits have no effect on the clock outputs. Programming the SSC_RCMR to select RK pin (CKS field) and at the same time Continuous Receive Clock (CKO field) can lead to unpredictable results.

Figure 44-10. Receive Clock Management



46.7.1 USART Control Register

Name: US_CR
Offset: 0x0000
Property: Write-only

For SPI control, see “USART Control Register (SPI_MODE)”.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								
			LINWKUP	LINABT	RTSDIS	RTSEN	DTRDIS	DTREN

Bit	15	14	13	12	11	10	9	8
Access								
Reset								
	RETTO	RSTNACK	RSTIT	SENDA	STTTO	STPBRK	STTBRK	RSTSTA

Bit	7	6	5	4	3	2	1	0
Access								
Reset								
	TXDIS	TXEN	RXDIS	RXEN	RSTTX	RSTRX		

Bit 21 – LINWKUP Send LIN Wakeup Signal

Value	Description
0	No effect.
1	Sends a wakeup signal on the LIN bus.

Bit 20 – LINABT Abort LIN Transmission

Value	Description
0	No effect.
1	Abort the current LIN transmission.

Bit 19 – RTSDIS Request to Send Pin Control

Value	Description
0	No effect.
1	Drives RTS pin to 0 if US_MR.USART_MODE field = 2, else drives RTS pin to 1 if US_MR.USART_MODE field = 0.

Bit 18 – RTSEN Request to Send Pin Control

Value	Description
0	The USART does not filter the receive line.
1	The USART filters the receive line using a three-sample filter (1/16-bit clock) (2 over 3 majority).

Bits 26:24 – MAX_ITERATION[2:0] Maximum Number of Automatic Iteration

Value	Description
0-7	Defines the maximum number of iterations in ISO7816 mode, protocol T = 0.

Bit 23 – INVDATA Inverted Data

Value	Description
0	The data field transmitted on TXD line is the same as the one written in US_THR or the content read in US_RHR is the same as RXD line. Normal mode of operation.
1	The data field transmitted on TXD line is inverted (voltage polarity only) compared to the value written on US_THR or the content read in US_RHR is inverted compared to what is received on RXD line (or ISO7816 IO line). Inverted mode of operation, useful for contactless card application. To be used with configuration bit MSBF.

Bit 22 – VAR_SYNC Variable Synchronization of Command/Data Sync Start Frame Delimiter

Value	Description
0	User defined configuration of command or data sync field depending on MODSYNC value.
1	The sync field is updated when a character is written into US_THR.

Bit 21 – DSNACK Disable Successive NACK

Value	Description
0	NACK is sent on the ISO line as soon as a parity error occurs in the received character (unless INACK is set).
1	Successive parity errors are counted up to the value specified in the MAX_ITERATION field. These parity errors generate a NACK on the ISO line. As soon as this value is reached, no additional NACK is sent on the ISO line. The flag ITER is asserted. Note: MAX_ITERATION field must be set to 0 if DSNACK is cleared.

Bit 20 – INACK Inhibit Non Acknowledge

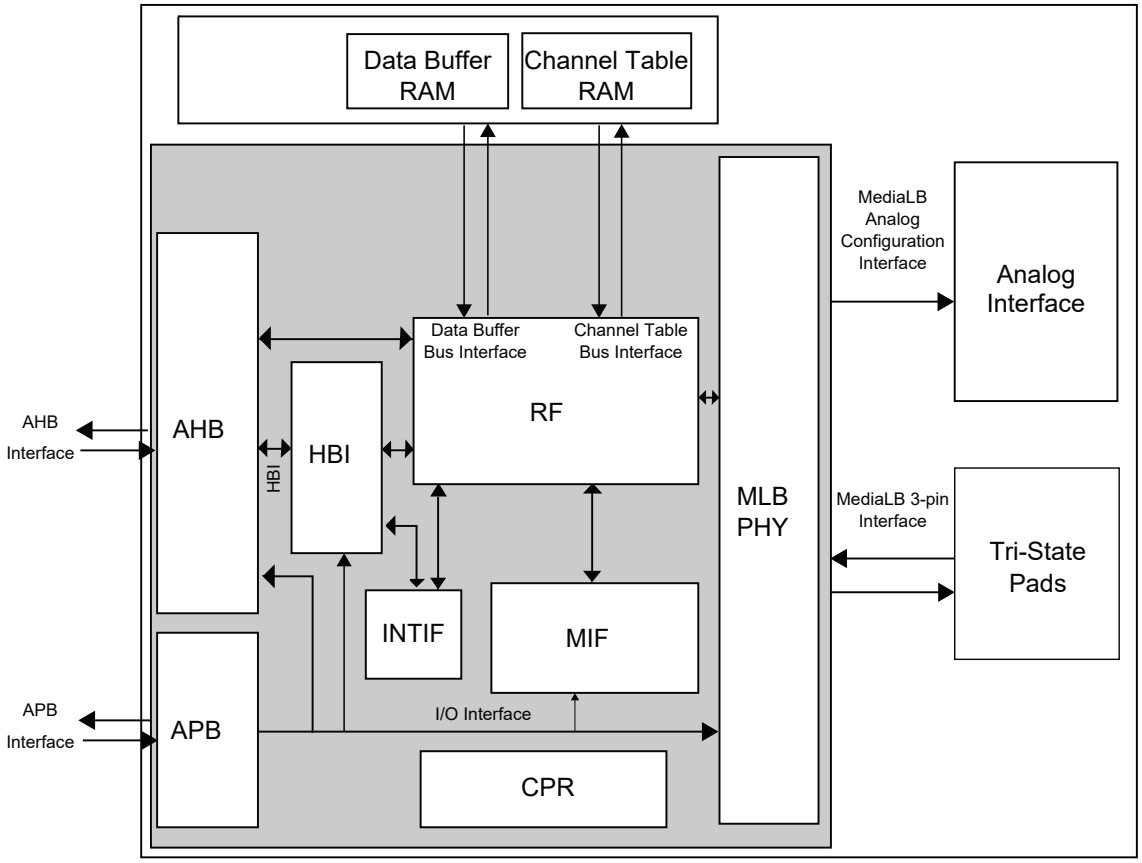
Value	Description
0	The NACK is generated.
1	The NACK is not generated.

Bit 19 – OVER Oversampling Mode

Value	Description
0	16X Oversampling
1	8X Oversampling

Bit 18 – CLKO Clock Output Select

Figure 48-1. 3-Pin MLB Block Diagram



48.4 Signal Description

48.4.1 Definition of Terms

The following terms will be used when referring to specific implementations of MediaLB.

Table 48-1. MediaLB Definition of Terms

Names	Description
Media Local Bus:	
MLBC	General reference to the Clock line of a Media Local Bus: on a 3-pin MediaLB interface, connects to the MLBCLK pin
MLBS	General reference to the Signal line of a Media Local Bus: on a 3-pin MediaLB interface, connects to the MLBSIG pin
MLBD	General reference to the Data line of a Media Local Bus: on a 3-pin MediaLB interface, connects to the MLBDAT pin
3-pin MediaLB Interface:	
MLBCLK	MediaLB Controller (output) pin connected to MLBC.

49.5.4.1 Acceptance Filtering

The MCAN offers the possibility to configure two sets of acceptance filters, one for standard identifiers and one for extended identifiers. These filters can be assigned to an Rx Buffer or to Rx FIFO 0,1. For acceptance filtering each list of filters is executed from element #0 until the first matching element. Acceptance filtering stops at the first matching element. The following filter elements are not evaluated for this message.

The main features are:

- Each filter element can be configured as
  - range filter (from - to)
  - filter for one or two dedicated IDs
  - classic bit mask filter
- Each filter element is configurable for acceptance or rejection filtering
- Each filter element can be enabled / disabled individually
- Filters are checked sequentially, execution stops with the first matching filter element

Related configuration registers are:

- Global Filter Configuration (MCAN_GFC)
- Standard ID Filter Configuration (MCAN_SIDFC)
- Extended ID Filter Configuration (MCAN_XIDFC)
- Extended ID and Mask (MCAN_XIDAM)

Depending on the configuration of the filter element (SFEC/EFEC) a match triggers one of the following actions:

- Store received frame in FIFO 0 or FIFO 1
- Store received frame in Rx Buffer
- Store received frame in Rx Buffer and generate pulse at filter event pin
- Reject received frame
- Set High Priority Message interrupt flag (MCAN_IR.HPM)
- Set High Priority Message interrupt flag (MCAN_IR.HPM) and store received frame in FIFO 0 or FIFO 1

Acceptance filtering is started after the complete identifier has been received. After acceptance filtering has completed, and if a matching Rx Buffer or Rx FIFO has been found, the Message Handler starts writing the received message data in portions of 32 bit to the matching Rx Buffer or Rx FIFO. If the CAN protocol controller has detected an error condition (e.g. CRC error), this message is discarded with the following impact on the effected Rx Buffer or Rx FIFO:

- Rx Buffer
  New Data flag of matching Rx Buffer is not set, but Rx Buffer (partly) overwritten with received data. For error type, see MCAN_PSR.LEC and MCAN_PSR.DLEC.
- Rx FIFO
  Put index of matching Rx FIFO is not updated, but related Rx FIFO element (partly) overwritten with received data. For error type, see MCAN_PSR.LEC and MCAN_PSR.DLEC. In case the matching Rx FIFO is operated in Overwrite mode, the boundary conditions described in Rx FIFO Overwrite Mode have to be considered.

49.6.35 MCAN Tx Buffer Configuration

Name: MCAN_TXBC
Offset: 0xC0
Reset: 0x00000000
Property: Read/Write

This register can only be written if the bits CCE and INIT are set in MCAN CC Control Register.

The sum of TFQS and NDTB may not exceed 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers.

Bit	31	30	29	28	27	26	25	24
		TFQM	TFQS[5:0]					
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
			NDTB[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TBSA[13:6]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TBSA[5:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit 30 – TFQM Tx FIFO/Queue Mode

Value	Description
0	Tx FIFO operation.
1	Tx Queue operation.

Bits 29:24 – TFQS[5:0] Transmit FIFO/Queue Size

Value	Description
0	No Tx FIFO/Queue.
1-32	Number of Tx Buffers used for Tx FIFO/Queue.
>32	Values greater than 32 are interpreted as 32.

Bits 21:16 – NDTB[5:0] Number of Dedicated Transmit Buffers

Value	Description
0	No dedicated Tx Buffers.
1-32	Number of dedicated Tx Buffers.
>32	Values greater than 32 are interpreted as 32.

- SYNC: Each channel has a synchronization signal SYNC. When asserted, this signal has the same effect as a software trigger. The SYNC signals of all channels are asserted simultaneously by writing TC_BCR with SYNC set.
- Compare RC Trigger: RC is implemented in each channel and can provide a trigger when the counter value matches the RC value if TC_CMRx.CPCTRG is set .

The channel can also be configured to have an external trigger. In Capture mode, the external trigger signal can be selected between TIOAx and TIOBx. In Waveform mode, an external event can be programmed on one of the following signals: TIOBx, XC0, XC1 or XC2. This external event can then be programmed to perform a trigger by setting TC_CMRx.ENETRG.

If an external trigger is used, the duration of the pulses must be longer than the peripheral clock period in order to be detected.

50.6.7 Capture Mode

Capture mode is entered by clearing TC_CMRx.WAVE.

Capture mode allows the TC channel to perform measurements such as pulse timing, frequency, period, duty cycle and phase on TIOAx and TIOBx signals which are considered as inputs.

The figure Figure 50-6 shows the configuration of the TC channel when programmed in Capture mode.

50.6.8 Capture Registers A and B

Registers A and B (TC_RA and TC_RB) are used as capture registers. They can be loaded with the counter value when a programmable event occurs on the signal TIOAx.

TC_CMRx.LDRA defines the TIOAx selected edge for the loading of TC_RA, and TC_CMRx.LDRB defines the TIOAx selected edge for the loading of TC_RB.

The subsampling ratio defined by TC_CMRx.SBSMPLR is applied to these selected edges, so that the loading of Register A and Register B occurs once every 1, 2, 4, 8 or 16 selected edges.

TC_RA is loaded only if it has not been loaded since the last trigger or if TC_RB has been loaded since the last loading of TC_RA.

TC_RB is loaded only if TC_RA has been loaded since the last trigger or the last loading of TC_RB.

Loading TC_RA or TC_RB before the read of the last value loaded sets TC_SR.LOVRS. In this case, the old value is overwritten.

When DMA is used (on channel 0), the Register AB (TC_RAB) address must be configured as source address of the transfer. TC_RAB provides the next unread value from TC_RA and TC_RB. It may be read by the DMA after a request has been triggered upon loading TC_RA or TC_RB.

50.6.9 Transfer with DMAC in Capture Mode

The DMAC can perform access from the TC to system memory in Capture mode only.

The following figure illustrates how TC_RA and TC_RB can be loaded in the system memory without processor intervention.

52.7.25 AFEC Correction Select Register

Name: AFEC_COSR
Offset: 0xD0
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the AFEC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								CSEL
Access								R/W
Reset								0

Bit 0 – CSEL Sample & Hold unit Correction Select
Selects the Sample & Hold unit to be displayed in the AFEC_CVR.

56.6.1 TRNG Control Register

Name: TRNG_CR
Offset: 0x00
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
	WAKEY[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	WAKEY[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	WAKEY[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bit	7	6	5	4	3	2	1	0
								ENABLE
Access								W
Reset								–

Bits 31:8 – WAKEY[23:0] Register Write Access Key

Value	Name	Description
0x524E47	PASSWD	Writing any other value in this field aborts the write operation.

Bit 0 – ENABLE Enables the TRNG to Provide Random Values

Value	Description
0	Disables the TRNG.
1	Enables the TRNG if 0x524E47 (“RNG” in ASCII) is written in KEY field at the same time.

where, C_{PCB} is the capacitance of the printed circuit board (PCB) track layout from the crystal to the pin.

58.4.7 3 to 20 MHz Crystal Characteristics

Table 58-24. 3 to 20 MHz Crystal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistor	Fundamental at 3 MHz	–	–	150	Ohm
		Fundamental at 8 MHz			140	
		Fundamental at 12 MHz			120	
		Fundamental at 16 MHz			80	
		Fundamental at 20 MHz			50	
C_M	Motional capacitance	Fundamental at 3 MHz	3	–	8	fF
		Fundamental at 8–20 MHz	1.6	–	8	
C_{SHUNT}	Shunt capacitance	–	–	–	7	pF
$C_{CRYSTAL}$	Allowed Crystal Capacitance Load	From crystal specification	12.5	–	17.5	pF
P_{ON}	Drive Level	3 MHz	–	–	15	µW
		8 MHz	–	–	30	
		12 MHz, 20 MHz	–	–	50	

58.4.8 3 to 20 MHz XIN Clock Input Characteristics in Bypass Mode

Table 58-25. 3 to 20 MHz XIN Clock Input Characteristics in Bypass Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPXIN})$	XIN Clock Frequency	(see **Note 1**)	–	–	20	MHz
t_{CHXIN}	XIN Clock High Half-period	(see **Note 1**)	25	–	–	ns
t_{CLXIN}	XIN Clock Low Half-period	(see **Note 1**)	25	–	–	ns
V_{XIN_IL}	V_{XIN} Input Low-level Voltage	(see **Note 1**)	Min of V_{IL} for CLOCK pad	–	Max of V_{IL} for CLOCK pad	V
V_{XIN_IH}	V_{XIN} Input High-level Voltage	(see **Note 1**)	Min of V_{IH} for CLOCK pad	–	Max of V_{IH} for CLOCK pad	V

Note:

1. These characteristics apply only when the 3–20 MHz crystal oscillator is in Bypass mode.

58.4.9 Crystal Oscillator Design Considerations

58.4.9.1 Choosing a Crystal

When choosing a crystal for the 32768 Hz Slow Clock Oscillator or for the 3–20 MHz oscillator, several parameters must be taken into account. Important parameters between crystal and product specifications are as follows:

Symbol	Parameter	Conditions	Min	Max	Unit
		1.8V domain	0.8	–	ns
SPI_{12}	NPCS setup to SPCK rising (slave)	3.3V domain	3.9	–	ns
		1.8V domain	4.4	–	ns
SPI_{13}	NPCS hold after SPCK falling (slave)	3.3V domain	0	–	ns
		1.8V domain	0	–	ns
SPI_{14}	NPCS setup to SPCK falling (slave)	3.3V domain	4.0	–	ns
		1.8V domain	4.1	–	ns
SPI_{15}	NPCS hold after SPCK falling (slave)	3.3V domain	0	–	ns
		1.8V domain	0	–	ns

Timings are given for the 3.3V domain, with V_{DDIO} from 2.85V to 3.6V, maximum external capacitor = 40 pF.

Table 58-57. SPI Timings

Symbol	Parameter	Conditions	Min	Max	Unit
SPI_0	MISO Setup time before SPCK rises (master)	3.3V domain	12.4	–	ns
SPI_1	MISO Hold time after SPCK rises (master)	3.3V domain	0	–	ns
SPI_2	SPCK rising to MOSI Delay (master)	3.3V domain	-3.7	2.2	ns
SPI_3	MISO Setup time before SPCK falls (master)	3.3V domain	12.6	–	ns
SPI_4	MISO Hold time after SPCK falls (master)	3.3V domain	0	–	ns
SPI_5	SPCK falling to MOSI Delay (master)	3.3V domain	-3.6	2.0	ns
SPI_6	SPCK falling to MISO Delay (slave)	3.3V domain	3.0	11.9	ns
SPI_7	MOSI Setup time before SPCK rises (slave)	3.3V domain	1.2	–	ns
SPI_8	MOSI Hold time after SPCK rises (slave)	3.3V domain	0.6	–	ns
SPI_9	SPCK rising to MISO Delay (slave)	3.3V domain	3.0	12.0	ns
SPI_{10}	MOSI Setup time before SPCK falls (slave)	3.3V domain	1.2	–	ns
SPI_{11}	MOSI Hold time after SPCK falls (slave)	3.3V domain	0.6	–	ns
SPI_{12}	NPCS setup to SPCK rising (slave)	3.3V domain	3.9	–	ns
SPI_{13}	NPCS hold after SPCK falling (slave)	3.3V domain	0	–	ns
SPI_{14}	NPCS setup to SPCK falling (slave)	3.3V domain	4.0	–	ns
SPI_{15}	NPCS hold after SPCK falling (slave)	3.3V domain	0	–	ns

Note that in SPI master mode, the device does not sample the data (MISO) on the opposite edge where the data clocks out (MOSI), but the same edge is used. See Figure 58-19 and Figure 58-20.