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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70q20a-an

6. Package and Pinout

In the tables that follow, the column “Reset State” indicates the reset state of the line with mnemonics.

- “PIO” “/” signal

Indicates whether the PIO Line resets in I/O mode or in peripheral mode. If “PIO” is mentioned, the PIO line is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is mentioned in the “Reset State” column, the PIO line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case of pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released.

- “I” / ”O”

Indicates whether the signal is input or output state.

- “PU” / “PD”

Indicates whether pullup, pulldown, or nothing is enabled.

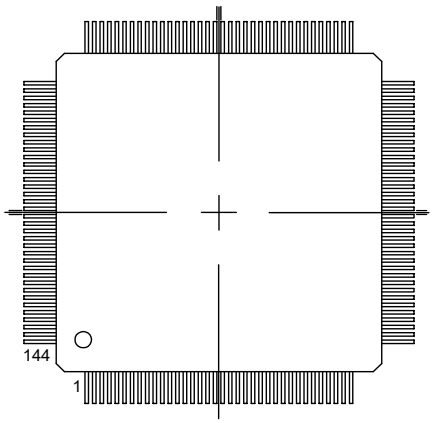
- “ST”

Indicates if Schmitt Trigger is enabled.

6.1 144-lead Packages

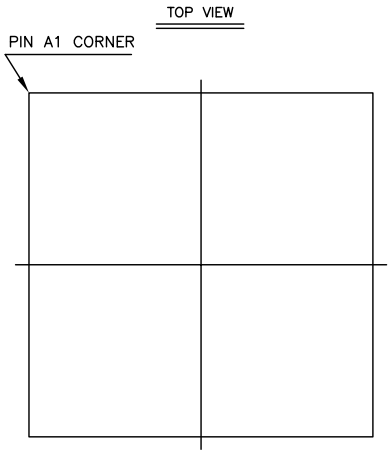
6.1.1 144-pin LQFP Package Outline

Figure 6-1. Orientation of the 144-pin LQFP Package



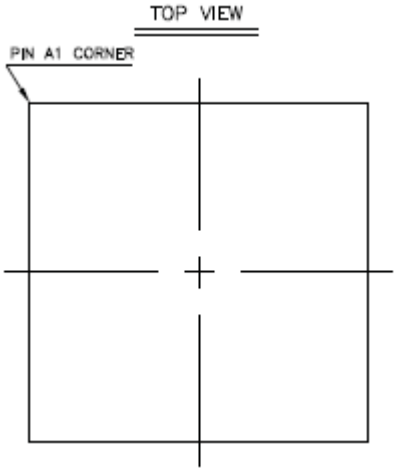
6.1.2 144-ball LFBGA/TFBGA Package Outline

Figure 6-2. Orientation of the 144-ball LFBGA/TFBGA Package



6.1.3 144-ball UFBGA Package Outline

Figure 6-3. Orientation of the 144-ball UFBGA Package



6.2 144-lead Package Pinout

Table 6-1. 144-lead Package Pinout

LQFP Pin	LFBGA/ TFBGA Ball	UFBGA Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		PIO Peripheral D		Reset State
					Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
102	C11	E11	VDDIO	GPIO_AD	PA0	I/O	WKUP0(1)	I	PWMC0_PWMH0	O	TIOA0	I/O	A17/BA1	O	I2SC0_MCK	O	PIO, I, PU, ST
99	D12	F11	VDDIO	GPIO_AD	PA1	I/O	WKUP1(1)	I	PWMC0_PWML0	O	TIOB0	I/O	A18	O	I2SC0_CK	I/O	PIO, I, PU, ST
93	E12	G12	VDDIO	GPIO	PA2	I/O	WKUP2(1)	I	PWMC0_PWMH1	O	–	–	DATRG	I	–	–	PIO, I, PU, ST
91	F12	G11	VDDIO	GPIO_AD	PA3	I/O	PIODC0(2)	I	TWD0	I/O	LONCOL1	I	PCK2	O	–	–	PIO, I, PU, ST

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Description
67	GMAC	Q2	–	GMAC Queue 2 Interrupt signal toggled on a DMA write to the first word of each DMA data buffer associated with queue 2
66	–	–	–	Reserved
67	–	–	–	Reserved
68	ARM	IXC	–	Floating Point Unit Interrupt IXC associated with FPU cumulative exception bit
69	I2SC0	X	X	Inter-IC Sound Controller
70	I2SC1	X	X	Inter-IC Sound Controller
71	GMAC	Q3	–	GMAC Queue 3 Interrupt signal toggled on a DMA write to the first word of each DMA data buffer associated with queue 3
72	GMAC	Q4	–	GMAC Queue 4 Interrupt signal toggled on a DMA write to the first word of each DMA data buffer associated with queue 4
73	GMAC	Q5	–	GMAC Queue 5 Interrupt signal toggled on a DMA write to the first word of each DMA data buffer associated with queue 5

14.2 Peripheral Signal Multiplexing on I/O Lines

The SAM E70/S70/V70/V71 features

- Two PIO controllers on 64-pin versions (PIOA and PIOB)
- Three PIO controllers on the 100-pin version (PIOA, PIOB and PIOD)
- Five PIO controllers on the 144-pin version (PIOA, PIOB, PIOC, PIOD and PIOE), that multiplex the I/O lines of the peripheral set.

The SAM E70/S70/V70/V71 PIO Controllers control up to 32 lines and each line can be assigned to one of four peripheral functions: A, B, C or D.

For more information on multiplexed signals, refer to the “Package and Pinout” chapter.

To compensate for possible temperature variations over time, this accurate clock calibration circuitry can be programmed on-the-fly and also programmed during application manufacturing, in order to correct the crystal frequency accuracy at room temperature (20–25°C). The typical clock drift range at room temperature is ±20 ppm.

In the device operating temperature range, the 32.768 kHz crystal oscillator clock inaccuracy can be up to -200 ppm.

The RTC clock calibration circuitry allows positive or negative correction in a range of 1.5 ppm to 1950 ppm.

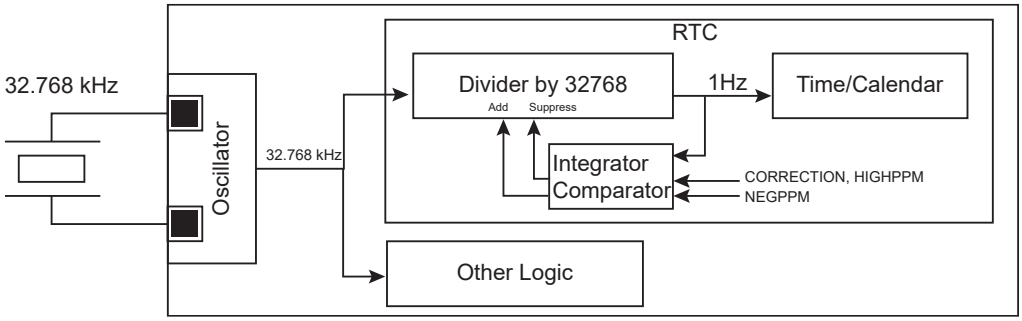
The calibration circuitry is fully digital. Thus, the configured correction is independent of temperature, voltage, process, etc., and no additional measurement is required to check that the correction is effective.

If the correction value configured in the calibration circuitry results from an accurate crystal frequency measure, the remaining accuracy is bounded by the values listed below:

- Below 1 ppm, for an initial crystal drift between 1.5 ppm up to 20 ppm, and from 30 ppm to 90 ppm
- Below 2 ppm, for an initial crystal drift between 20 ppm up to 30 ppm, and from 90 ppm to 130 ppm
- Below 5 ppm, for an initial crystal drift between 130 ppm up to 200 ppm

The calibration circuitry does not modify the 32.768 kHz crystal oscillator clock frequency but it acts by slightly modifying the 1 Hz clock period from time to time. The correction event occurs every 1 + [(20 - (19 x HIGHPPM)) x CORRECTION] seconds. When the period is modified, depending on the sign of the correction, the 1 Hz clock period increases or reduces by around 4 ms. Depending on the CORRECTION, NEGPPM and HIGHPPM values configured in RTC_MR, the period interval between two correction events differs.

Figure 27-4. Calibration Circuitry



32.6.1.49 PIO I/O Drive Register 1

Name: PIO_DRIVER1
Offset: 0x0118
Property: Read/Write

Register Reset value: 0x000000000xAAAAAAAA

Bit	31	30	29	28	27	26	25	24
	LINE31	LINE30	LINE29	LINE28	LINE27	LINE26	LINE25	LINE24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	LINE23	LINE22	LINE21	LINE20	LINE19	LINE18	LINE17	LINE16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	LINE15	LINE14	LINE13	LINE12	LINE11	LINE10	LINE9	LINE8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	LINE7	LINE6	LINE5	LINE4	LINE3	LINE2	LINE1	LINE0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – LINE Drive of PIO Line

Value	Name	Description
0	LOW_DRIVE	Lowest drive
1	HIGH_DRIVE	Highest drive

38.8.12 GMAC Interrupt Disable Register

Name: GMAC_IDR
Offset: 0x02C
Reset: –
Property: Write-only

This register is write-only and will always return zero.

The following values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
Access			W	W	R	W	W	W
Reset			–	–	–	–	–	–

Bit	23	22	21	20	19	18	17	16
	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
Access	W	W	W	W	W	W		
Reset	–	–	–	–	–	–		

Bit	15	14	13	12	11	10	9	8
	EXINT	PFTR	PTZ	PFNZ	HRESP	ROVR		
Access	W	W	W	W	W	W		
Reset	–	–	–	–	–	–		

Bit	7	6	5	4	3	2	1	0
	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bit 29 – TSUTIMCMP TSU Timer Comparison

Bit 28 – WOL Wake On LAN

Bit 27 – RXLPISBC Receive LPI indication Status Bit Change
Receive LPI indication status bit change.

Cleared on read.

Bit 26 – SRI TSU Seconds Register Increment

Bit 25 – PDRSFT PDelay Response Frame Transmitted

Bit 24 – PDRQFT PDelay Request Frame Transmitted

Bit 23 – PDRSFR PDelay Response Frame Received

Bits 15:0 – DATA[15:0] PHY Data
For a write operation, this field is written with the data to be written to the PHY.

After a read operation, this field contains the data read from the PHY.

39.6.63 Host Pipe x IN Request Register

Name: USBHS_HSTPIPINRQx
Offset: 0x0650 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								INMODE
Reset								0

Bit	7	6	5	4	3	2	1	0
Access	INRQ[7:0]							
Reset	0	0	0	0	0	0	0	0

Bit 8 – INMODE IN Request Mode

Value	Description
0	Performs a pre-defined number of IN requests. This number is the INRQ field.
1	Enables the USBHS to perform infinite IN requests when the pipe is not frozen.

Bits 7:0 – INRQ[7:0] IN Request Number before Freeze
This field contains the number of IN transactions before the USBHS freezes the pipe. The USBHS performs (INRQ+1) IN requests before freezing the pipe. This counter is automatically decreased by 1 each time an IN request has been successfully performed.

This register has no effect when INMODE = 1.

40.14.13 HSMCI Interrupt Enable Register

Name: HSMCI_IER
Offset: 0x44
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
	UNRE	OVRE	ACKRCVE	ACKRCV	XFRDONE	FIFOEMPTY		BLKOVRE
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CSTOE	DTOE	DCRCE	RTOE	RENDE	RCRCE	RDIRE	RINDE
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
			CSRCV	SDIOWAIT				SDIOIRQA
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			NOTBUSY	DTIP	BLKE	TXRDY	RXRDY	CMDRDY
Access								
Reset								

Bit 31 – UNRE Underrun Interrupt Enable

Bit 30 – OVRE Overrun Interrupt Enable

Bit 29 – ACKRCVE Boot Acknowledge Error Interrupt Enable

Bit 28 – ACKRCV Boot Acknowledge Interrupt Enable

Bit 27 – XFRDONE Transfer Done Interrupt enable

Bit 26 – FIFOEMPTY FIFO empty Interrupt enable

Bit 24 – BLKOVRE DMA Block Overrun Error Interrupt Enable

Bit 23 – CSTOE Completion Signal Timeout Error Interrupt Enable

Bit 22 – DTOE Data Time-out Error Interrupt Enable

Bit 21 – DCRCE Data CRC Error Interrupt Enable

43.7.4 TWIHS Internal Address Register

Name: TWIHS_IADR
Offset: 0x0C
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	IADR[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	IADR[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IADR[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – IADR[23:0] Internal Address
0, 1, 2 or 3 bytes depending on IADRSZ.

44.9.7 SSC Receive Holding Register

Name: SSC_RHR
Offset: 0x20
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	RDAT[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RDAT[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RDAT[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RDAT[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – RDAT[31:0] Receive Data
Right aligned regardless of the number of data bits defined by DATLEN in SSC_RFMR.

Table 46-12. SPI Bus Protocol Mode

SPI Bus Protocol Mode	CPOL	CPHA
0	0	1
1	0	0
2	1	1
3	1	0

Figure 46-37. SPI Transfer Format (CPHA = 1, 8 bits per transfer)

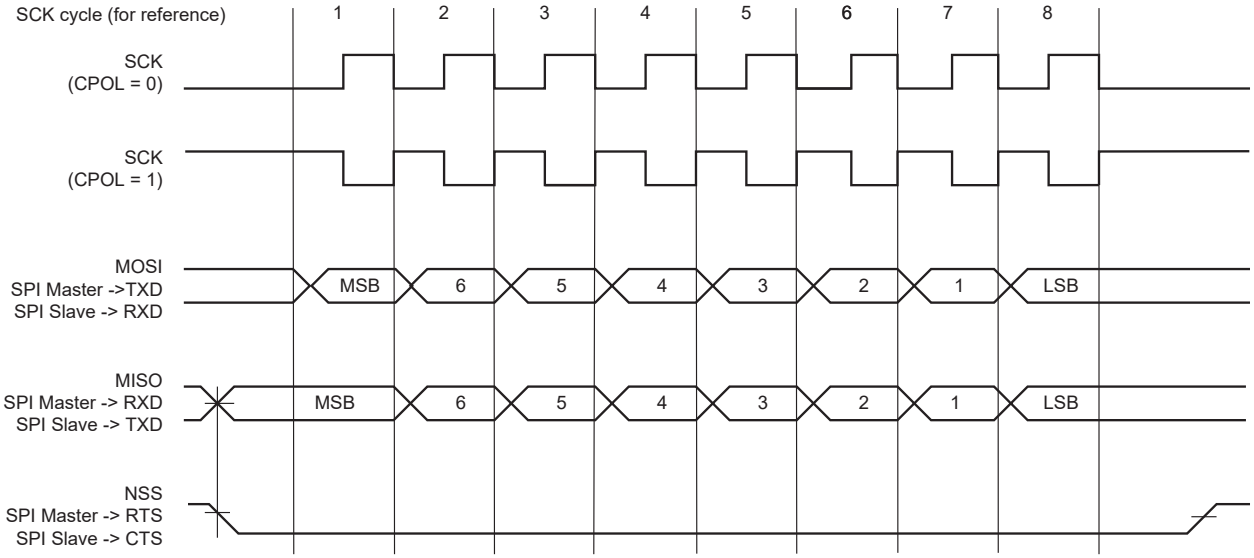
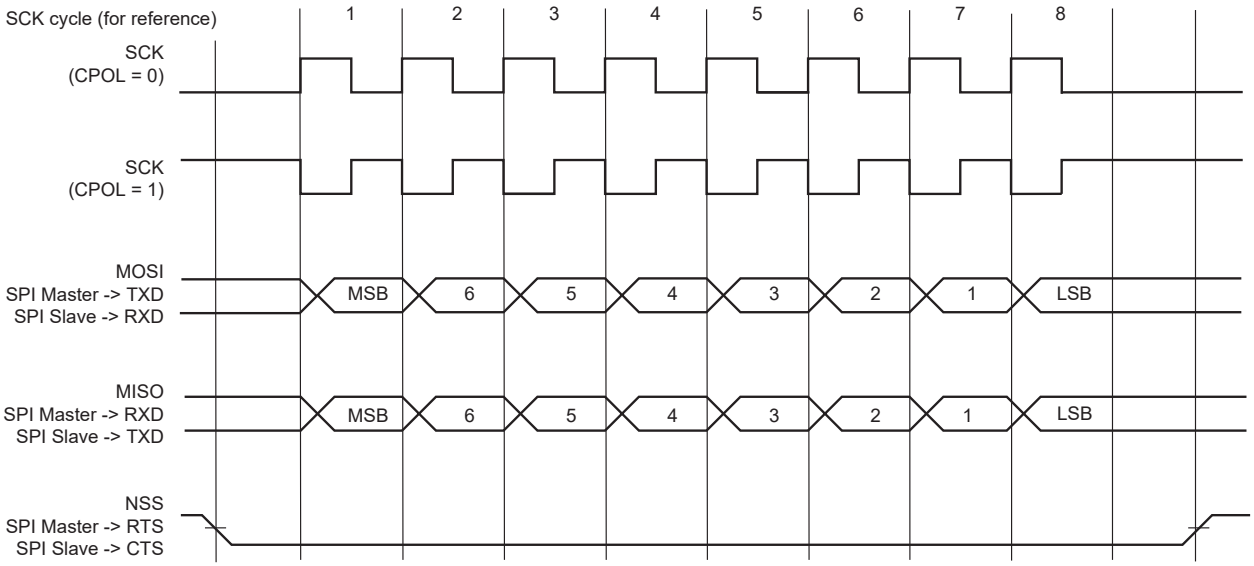


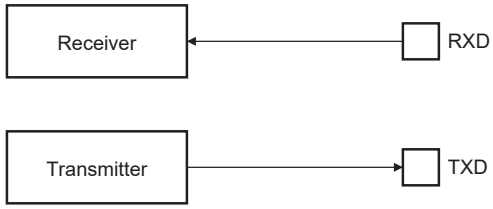
Figure 46-38. SPI Transfer Format (CPHA = 0, 8 bits per transfer)



46.6.8.4 Receiver and Transmitter Control

See “Receiver and Transmitter Control”.

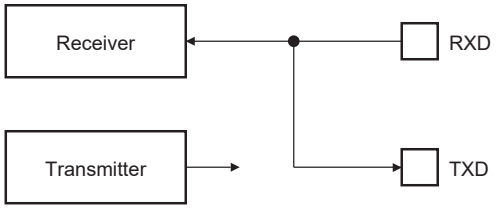
Figure 46-66. Normal Mode Configuration



46.6.11.2 Automatic Echo Mode

Automatic Echo mode allows bit-by-bit retransmission. When a bit is received on the RXD pin, it is sent to the TXD pin, as shown in the following figure. Programming the transmitter has no effect on the TXD pin. The RXD pin is still connected to the receiver input, thus the receiver remains active.

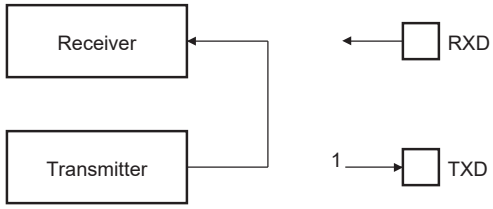
Figure 46-67. Automatic Echo Mode Configuration



46.6.11.3 Local Loopback Mode

Local Loopback mode connects the output of the transmitter directly to the input of the receiver, as shown in the following figure. The TXD and RXD pins are not used. The RXD pin has no effect on the receiver and the TXD pin is continuously driven high, as in idle state.

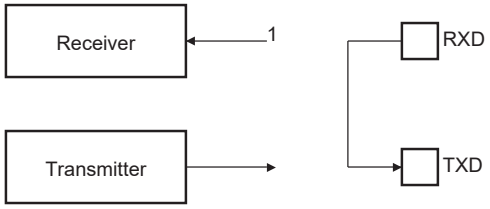
Figure 46-68. Local Loopback Mode Configuration



46.6.11.4 Remote Loopback Mode

Remote Loopback mode directly connects the RXD pin to the TXD pin, as shown in the following figure. The transmitter and the receiver are disabled and have no effect. This mode allows bit-by-bit retransmission.

Figure 46-69. Remote Loopback Mode Configuration



46.6.12 Register Write Protection

To prevent any single software error from corrupting USART behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the USART Write Protection Mode Register (US_WPMR).

Field	No. of Bits	Description	Accessibility
		1 = Enabled	
LE	1	Endianess select: 0 = Big Endian 1 = Little Endian	r,w
PG	1	Page pointer. Software initializes to zero, hardware writes thereafter. 0 = Ping buffer 1 = Pong buffer	r,w,u (1)
RDY1	1	Buffer ready bit for ping buffer page: 0 = Not ready 1 = Ready	r,w
RDY2	1	Buffer ready bit for pong buffer page: 0 = Not ready 1 = Ready	r,w
DNE1	1	Buffer done bit for ping buffer page: 0 = Not done 1 = Done	r,u (1),c0
DNE2	1	Buffer done bit for pong buffer page: 0 = Not done 1 = Done	r,u (1),c0
ERR1	1	AHB error response detected for ping buffer page: 0 = No error 1 = Error	r,u (1),c0 (2)
ERR2	1	AHB error response detected for pong buffer page: 0 = No error 1 = Error	r,u (1),c0 (2)
PS1	1	Packet start bit for ping buffer page: 0 = No packet start 1 = Packet start Reserved for synchronous and isochronous channels.	r,w,u (1) (both Tx and Rx)
PS2	1	Packet start bit for pong buffer page: 0 = No packet start 1 = Packet start	r,w,u (1) (both Tx and Rx)

Offset	Name	Bit Pos.								
		31:24								
0x8C	TC_RAB2	7:0	RAB[7:0]							
		15:8	RAB[15:8]							
		23:16	RAB[23:16]							
		31:24	RAB[31:24]							
0x90	TC_CV2	7:0	CV[7:0]							
		15:8	CV[15:8]							
		23:16	CV[23:16]							
		31:24	CV[31:24]							
0x94	TC_RA2	7:0	RA[7:0]							
		15:8	RA[15:8]							
		23:16	RA[23:16]							
		31:24	RA[31:24]							
0x98	TC_RB2	7:0	RB[7:0]							
		15:8	RB[15:8]							
		23:16	RB[23:16]							
		31:24	RB[31:24]							
0x9C	TC_RC2	7:0	RC[7:0]							
		15:8	RC[15:8]							
		23:16	RC[23:16]							
		31:24	RC[31:24]							
0xA0	TC_SR2	7:0	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
		15:8								
		23:16						MTIOB	MTIOA	CLKSTA
		31:24								
0xA4	TC_IER2	7:0	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
		15:8								
		23:16								
		31:24								
0xA8	TC_IDR2	7:0	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
		15:8								
		23:16								
		31:24								
0xAC	TC_IMR2	7:0	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
		15:8								
		23:16								
		31:24								
0xB0	TC_EMR2	7:0			TRIGSRCB[1:0]				TRIGSRCA[1:0]	
		15:8								NODIVCLK
		23:16								
		31:24								
0xB4 ... 0xBF	Reserved									
0xC0	TC_BCR	7:0								SYNC
		15:8								

50.7.20 TC QDEC Interrupt Status Register

Name: TC_QISR
Offset: 0xD4
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
								DIR
Access								R
Reset								0

Bit	7	6	5	4	3	2	1	0
					MPE	QERR	DIRCHG	IDX
Access					R	R	R	R
Reset					0	0	0	0

Bit 8 – DIR Direction
Returns an image of the current rotation direction.

Bit 3 – MPE Consecutive Missing Pulse Error

Value	Description
0	The number of consecutive missing pulses has not reached the maximum value specified in MAXCMP since the last read of TC_QISR.
1	An occurrence of MAXCMP consecutive missing pulses has been detected since the last read of TC_QISR.

Bit 2 – QERR Quadrature Error

Value	Description
0	No quadrature error since the last read of TC_QISR.
1	A quadrature error occurred since the last read of TC_QISR.

Bit 1 – DIRCHG Direction Change

Value	Description
0	No change on rotation direction since the last read of TC_QISR.
1	The rotation direction changed since the last read of TC_QISR.

52.7.19 AFEC Channel Data Register

Name: AFEC_CDR
Offset: 0x68
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – DATA[15:0] Converted Data
Returns the AFE conversion data corresponding to channel CSEL (configured in the AFEC Channel Selection Register).

At the end of a conversion, the converted data is loaded into one of the 12 internal registers (one for each channel) and remains in this internal register until a new conversion is completed on the same channel index. The AFEC_CDR together with AFEC_CSELR allows to multiplex all the internal channel data registers.

The data carried on AFEC_CDR is valid only if AFEC_CHSR.CHx bit is set (where x = AFEC_CSELR.CSEL field value).

57.5.11 AES Additional Authenticated Data Length Register

Name: AES_AADLENR
Offset: 0x70
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	AADLEN[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	AADLEN[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	AADLEN[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	AADLEN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – AADLEN[31:0] Additional Authenticated Data Length
Length in bytes of the Additional Authenticated Data (AAD) that is to be processed.

Note: The maximum byte length of the AAD portion of a message is limited to the 32-bit counter length.

Table 58-16. Typical Wakeup Time to Resume from Wait Mode

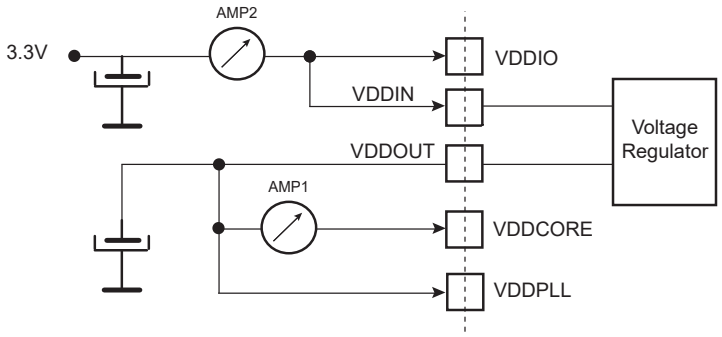
Conditions	Wake-up Time from Wait Mode	Unit
Resume from internal Flash with Cache enabled	8.1	µs
Resume from internal Flash with Cache disabled	8.5	µs
Resume from internal SRAM with Cache disabled	8	µs

58.3.4 Active Mode Power Consumption

The conditions for measurement are defined as follows:

- $V_{DDIO} = V_{DDIN} = 3.3V$
- V_{DDCORE} is provided by the Internal Voltage Regulator
- $T_A = 25°C$
- Application running from Flash memory with 128-bit access mode
- All peripheral clocks are deactivated.
- Master Clock (MCK) running at various frequencies with PLLA or the fast RC oscillator.
- Current measurement on AMP1 (VDDCORE) and total current on AMP2

Figure 58-8. Active Mode Measurement Setup



The following table gives current consumption in Active mode in typical conditions.

Table 58-17. Typical Total Active Power Consumption with VDDCORE at 1.2V Running from Embedded Memory (AMP2)

Core Clock/MCK (MHz)	Cortex-M7 Running CoreMark			Unit
	Flash		TCM	
	Cache Enable (CE) CoreMark = 4.9/MHz	Cache Disable (CD) CoreMark = 1.0/MHz	CoreMark = 5.0/MHz	
300/150	90	57	83	mA
250/125	77	48	70	
150/150	52	40	48	
96/96	35	27	33	
96/48	31	20	28	
48/48	18	15	17	
24/24	10	8	9	

Table 59-55. QSPI Timings

Symbol	Parameter	Conditions	Min	Max	Unit
$QSPI_0$	QIOx data in to QSCK rising edge (input setup time)	3.3V domain	2.5	–	ns
		1.8V domain	2.9	–	ns
$QSPI_1$	QIOx data in to QSCK rising edge (input hold time)	3.3V domain	0	–	ns
		1.8V domain	0	–	ns
$QSPI_2$	QSCK rising edge to QIOx data out valid	3.3V domain	-1.3	1.9	ns
		1.8V domain	-2.5	3.0	ns
$QSPI_3$	QIOx data in to QSCK falling edge (input setup time)	3.3V domain	2.9	–	ns
		1.8V domain	3.2	–	ns
$QSPI_4$	QIOx data in to QSCK falling edge(input hold time)	3.3V domain	0	–	ns
		1.8V domain	0	–	ns
$QSPI_5$	QSCK falling edge to QIOx data out valid	3.3V domain	-1.6	1.8	ns
		1.8V domain	-2.7	3.1	ns

Timings are given for the 3.3V domain, with VDDIO from 2.85V to 3.6V, maximum external capacitor = 40 pF.

59.13.1.6 SPI Characteristics

In the figures below, the MOSI line shifting edge is represented with a hold time equal to 0. However, it is important to note that for this device, the MISO line is sampled prior to the MOSI line shifting edge. As shown further below, the device sampling point extends the propagation delay (t_p) for slave and routing delays to more than half the SPI clock period, whereas the common sampling point allows only less than half the SPI clock period.

As an example, an SPI Slave working in Mode 0 can be safely driven if the SPI Master is configured in Mode 0.

Figure 59-19. MISO Capture in Master Mode