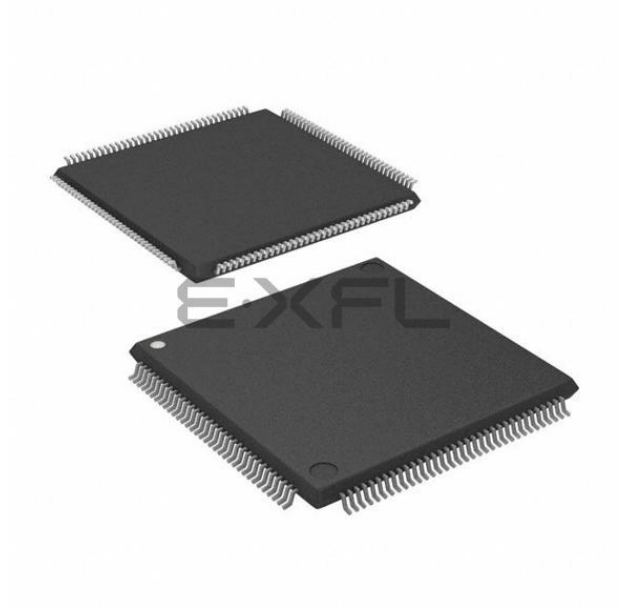

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70q20b-ant

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
URXDx	UART Receive Data	Input	–	–	PCK4 can be used to generate the baud rate
UTXDx	UART Transmit Data	Output	–	–	
PIO Controller - PIOA - PIOB - PIOC - PIOD - PIOE					
PA0–PA31	Parallel IO Controller A	I/O	–	VDDIO	–
PB0–PB9, PB12–PB13	Parallel IO Controller B	I/O	–		–
PC0– PC31	Parallel IO Controller C	I/O	–		–
PD0–PD31	Parallel IO Controller D	I/O	–	–	–
PE0–PE5	Parallel IO Controller E	I/O	–	–	–
PIO Controller - Parallel Capture Mode					
PIODC0–PIODC7	Parallel Capture Mode Data	Input	–	VDDIO	–
PIODCCLK	Parallel Capture Mode Clock	Input	–		–
PIODCEN1–PIODCEN2	Parallel Capture Mode Enable	Input	–		–
External Bus Interface					
D[15:0]	Data Bus	I/O	–	–	–
A[23:0]	Address Bus	Output	–	–	–
NWAIT	External Wait Signal	Input	Low	–	–
Static Memory Controller - SMC					
NCS0–NCS3	Chip Select Lines	Output	Low	–	–
NRD	Read Signal	Output	Low	–	–
NWE	Write Enable	Output	Low	–	–
NWR0–NWR1	Write Signal	Output	Low	–	–
NBS0–NBS1	Byte Mask Signal	Output	Low	–	Used also for SDRAMC
NAND Flash Logic					
NANDOE	NAND Flash Output Enable	Output	Low	–	–
NANDWE	NAND Flash Write Enable	Output	Low	–	–
SDR-SDRAM Controller Logic					

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Description
67	GMAC	Q2	–	GMAC Queue 2 Interrupt signal toggled on a DMA write to the first word of each DMA data buffer associated with queue 2
66	–	–	–	Reserved
67	–	–	–	Reserved
68	ARM	IXC	–	Floating Point Unit Interrupt IXC associated with FPU cumulative exception bit
69	I2SC0	X	X	Inter-IC Sound Controller
70	I2SC1	X	X	Inter-IC Sound Controller
71	GMAC	Q3	–	GMAC Queue 3 Interrupt signal toggled on a DMA write to the first word of each DMA data buffer associated with queue 3
72	GMAC	Q4	–	GMAC Queue 4 Interrupt signal toggled on a DMA write to the first word of each DMA data buffer associated with queue 4
73	GMAC	Q5	–	GMAC Queue 5 Interrupt signal toggled on a DMA write to the first word of each DMA data buffer associated with queue 5

14.2 Peripheral Signal Multiplexing on I/O Lines

The SAM E70/S70/V70/V71 features

- Two PIO controllers on 64-pin versions (PIOA and PIOB)
- Three PIO controllers on the 100-pin version (PIOA, PIOB and PIOD)
- Five PIO controllers on the 144-pin version (PIOA, PIOB, PIOC, PIOD and PIOE), that multiplex the I/O lines of the peripheral set.

The SAM E70/S70/V70/V71 PIO Controllers control up to 32 lines and each line can be assigned to one of four peripheral functions: A, B, C or D.

For more information on multiplexed signals, refer to the “Package and Pinout” chapter.

25.5.2 Reinforced Safety Watchdog Timer Mode Register

Name: RSWDT_MR
Offset: 0x04
Reset: 0x3FFFAFFF
Property: Read/Write Once

Note: The first write access prevents any further modification of the value of this register; read accesses remain possible.

Note: The WDV value must not be modified within three slow clock periods following a restart of the watchdog performed by means of a write access in the RSWDT_CR, else the watchdog may trigger an end of period earlier than expected.

Bit	31	30	29	28	27	26	25	24
			WDIDLEHLT	WDDBGHLT	ALLONES[11:8]			
Access								
Reset			1	1	1	1	1	1

Bit	23	22	21	20	19	18	17	16
	ALLONES[7:0]							
Access								
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	WDDIS		WDRSTEN	WDFIEN	WDV[11:8]			
Access								
Reset	1		1	0	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	WDV[7:0]							
Access								
Reset	1	1	1	1	1	1	1	1

Bit 29 – WDIDLEHLT Watchdog Idle Halt

Value	Description
0	The RSWDT runs when the system is in idle mode.
1	The RSWDT stops when the system is in idle state.

Bit 28 – WDDBGHLT Watchdog Debug Halt

Value	Description
0	The RSWDT runs when the processor is in debug state.
1	The RSWDT stops when the processor is in debug state.

Bits 27:16 – ALLONES[11:0] Must Always Be Written with 0xFFF

Bit 15 – WDDIS Watchdog Disable

28. Real-time Timer (RTT)

28.1 Description

The Real-time Timer (RTT) is built around a 32-bit counter used to count roll-over events of the programmable 16-bit prescaler driven from the 32-kHz slow clock source. It generates a periodic interrupt and/or triggers an alarm on a programmed value.

The RTT can also be configured to be driven by the 1Hz RTC signal, thus taking advantage of a calibrated 1Hz clock.

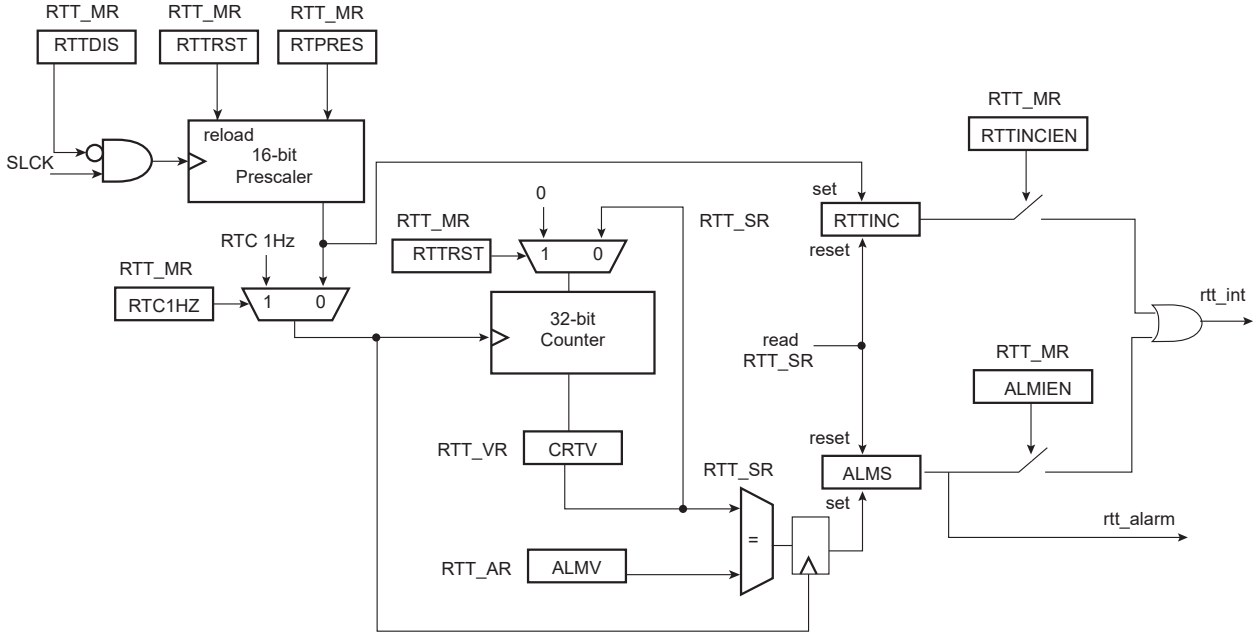
The slow clock source can be fully disabled to reduce power consumption when only an elapsed seconds count is required.

28.2 Embedded Characteristics

- 32-bit Free-running Counter on prescaled slow clock or RTC calibrated 1Hz clock
- 16-bit Configurable Prescaler
- Interrupt on Alarm or Counter Increment

28.3 Block Diagram

Figure 28-1. Real-time Timer Block Diagram



28.4 Functional Description

The programmable 16-bit prescaler value can be configured through the RTPRES field in the RTT Mode register (RTT_MR).

31.20.9 PMC Clock Generator Main Clock Frequency Register

Name: CKGR_MCFR
Offset: 0x0024
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
								CCSS
Access								
Reset								0

Bit	23	22	21	20	19	18	17	16
				RCMEAS				MAINFRDY
Access								
Reset				0				0

Bit	15	14	13	12	11	10	9	8
	MAINF[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MAINF[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit 24 – CCSS Counter Clock Source Selection

Value	Description
0	The measured clock of the MAINF counter is the Main RC oscillator.
1	The measured clock of the MAINF counter is the Main crystal oscillator.

Bit 20 – RCMEAS RC Oscillator Frequency Measure (write-only)
The measurement is performed on the main frequency (i.e., not limited to the Main RC oscillator only). If the source of MAINCK is the Main crystal oscillator, the restart of measurement may not be required because of the stability of crystal oscillators.

Value	Description
0	No effect.
1	Restarts measuring of the frequency of MAINCK. MAINF carries the new frequency as soon as a low-to-high transition occurs on the MAINFRDY flag.

Bit 16 – MAINFRDY Main Clock Frequency Measure Ready

32.6.1.21 PIO Pull-Up Disable Register

Name: PIO_PUDR
Offset: 0x0060
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

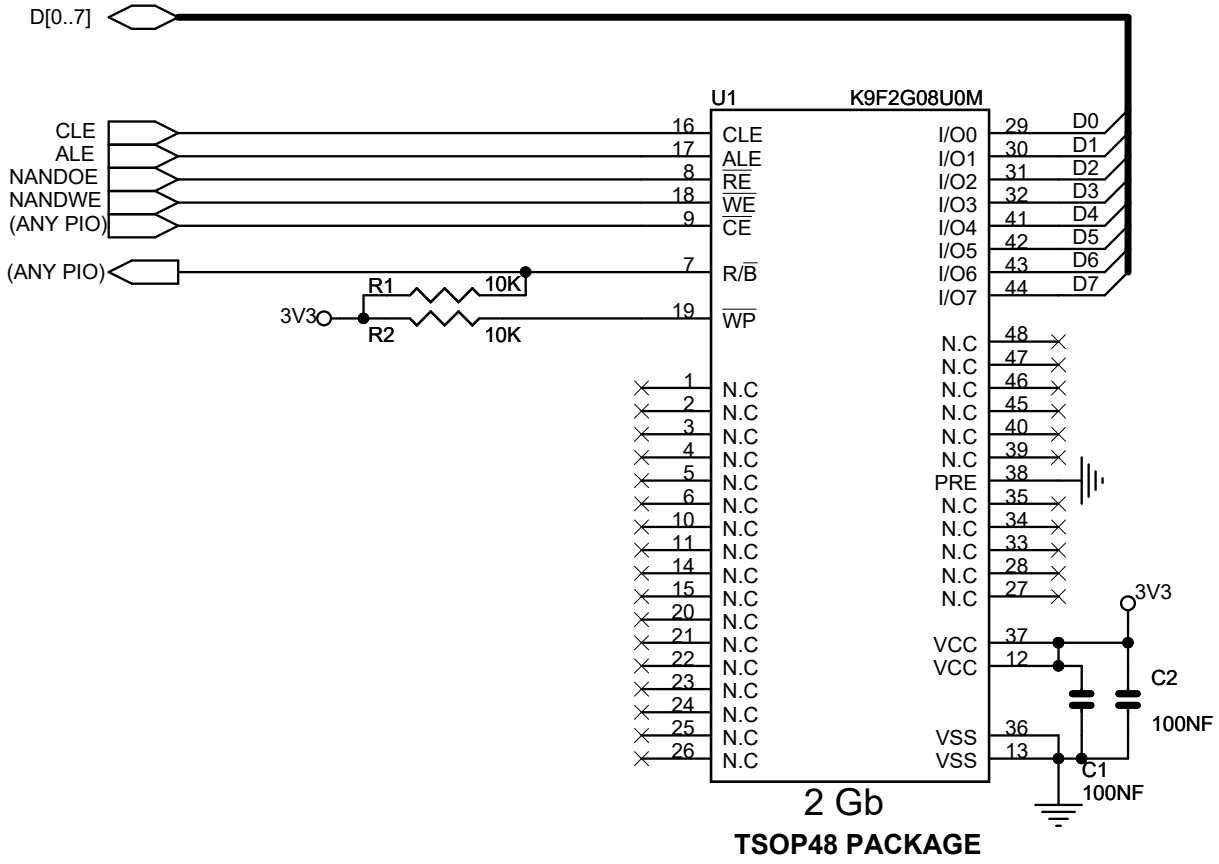
Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Pull-Up Disable

Value	Description
0	No effect.
1	Disables the pullup resistor on the I/O line.

35.8.1.1 8-bit NAND Flash

Hardware Configuration

Figure 35-7. 8-bit NAND Flash



Software Configuration
Perform the following configuration:

1. Select the chip select used to drive the NAND Flash by setting the bit CCFG_SMCNFCS.SMC_NFCSx.
2. Reserve A21 / A22 for ALE / CLE functions. Address and Command Latches are controlled by setting the address bits A21 and A22, respectively, during accesses.
3. NANDOE and NANDWE signals are multiplexed with PIO lines. Thus, the dedicated PIOs must be programmed in Peripheral mode in the PIO controller.
4. Configure a PIO line as an input to manage the Ready/Busy signal.
5. Configure SMC CS3 Setup, Pulse, Cycle and Mode according to NAND Flash timings, the data bus width and the system bus frequency.

In this example, the NAND Flash is not addressed as a “CE don’t care”. To address it as a “CE don’t care”, connect NCS3 (if SMC_NFCS3 is set) to the NAND Flash CE.

Offset	Name	Bit Pos.								
		31:24								
0xC4	XDMAC_CDUS1	7:0	DUBS[7:0]							
		15:8	DUBS[15:8]							
		23:16	DUBS[23:16]							
		31:24								
0xC8 ... 0xCF	Reserved									
0xD0	XDMAC_CIE2	7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
		15:8								
		23:16								
		31:24								
0xD4	XDMAC_CID2	7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
		15:8								
		23:16								
		31:24								
0xD8	XDMAC_CIM2	7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
		15:8								
		23:16								
		31:24								
0xDC	XDMAC_CIS2	7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
		15:8								
		23:16								
		31:24								
0xE0	XDMAC_CSA2	7:0	SA[7:0]							
		15:8	SA[15:8]							
		23:16	SA[23:16]							
		31:24	SA[31:24]							
0xE4	XDMAC_CDA2	7:0	DA[7:0]							
		15:8	DA[15:8]							
		23:16	DA[23:16]							
		31:24	DA[31:24]							
0xE8	XDMAC_CNDA2	7:0	NDA[5:0]							NDAIF
		15:8	NDA[13:6]							
		23:16	NDA[21:14]							
		31:24	NDA[29:22]							
0xEC	XDMAC_CNDC2	7:0				NDVIEW[1:0]		NDDUP	NDSUP	NDE
		15:8								
		23:16								
		31:24								
0xF0	XDMAC_CUBC2	7:0	UBLEN[7:0]							
		15:8	UBLEN[15:8]							
		23:16	UBLEN[23:16]							
		31:24								
0xF4	XDMAC_CBC2	7:0	BLEN[7:0]							
		15:8					BLEN[11:8]			

Value	Description
0	Indicates that the request is not completed (if a request was issued).
1	Disable request has completed. This flag is reset after a read operation.

Bit 0 – ENABLE Module Enable

Value	Description
0	Module is disabled.
1	Module is enabled.

Value	Name	Description
		• for OUT endpoint, USBHS_DEVEPTIMRx.NBUSYBKE = 1 and all the banks are busy.

Bits 9:8 – DTSEQ[1:0] Data Toggle Sequence
This field is set to indicate the PID of the current bank:

For IN transfers, it indicates the data toggle sequence that should be used for the next packet to be sent. This is not relative to the current bank.

For OUT transfers, this value indicates the last data toggle sequence received on the current bank.

By default, DTSEQ is 0b01, as if the last data toggle sequence was Data1, so the next sent or expected data toggle sequence should be Data0.

Value	Name	Description
0	DATA0	Data0 toggle sequence
1	DATA1	Data1 toggle sequence
2	DATA2	Reserved for high-bandwidth isochronous endpoint
3	MDATA	Reserved for high-bandwidth isochronous endpoint

Bit 7 – SHORTPACKET Short Packet Interrupt

Value	Description
0	Cleared when SHORTPACKETC = 1. This acknowledges the interrupt.
1	Set for non-control OUT endpoints, when a short packet has been received. This triggers a PEP_x interrupt if USBHS_DEVEPTIMRx.SHORTPACKETE = 1.

Bit 6 – STALLEDI STALLed Interrupt

Value	Description
0	Cleared when STALLEDIC = 1. This acknowledges the interrupt.
1	Set to signal that a STALL handshake has been sent. To do that, the software has to set the STALLRQ bit (by writing a one to the STALLRQS bit). This triggers a PEP_x interrupt if STALLEDE = 1.

Bit 5 – OVERFI Overflow Interrupt
For all endpoint types, an overflow can occur during the OUT stage if the host attempts to write into a bank that is too small for the packet. The packet is acknowledged and the USBHS_DEVEPTISRx.RXOUTI bit is set as if no overflow had occurred. The bank is filled with all the first bytes of the packet that fit in.

Value	Description
0	Cleared when the OVERFIC bit is written to one. This acknowledges the interrupt.
1	Set when an overflow error occurs. This triggers a PEP_x interrupt if OVERFE = 1.

Bit 4 – NAKINI NAKed IN Interrupt

Value	Description
0	Cleared when NAKINIC = 1. This acknowledges the interrupt.
1	Set when a NAK handshake has been sent in response to an IN request from the host. This triggers a PEP_x interrupt if NAKINE = 1.

39.6.17 Device Endpoint Interrupt Clear Register (Control, Bulk, Interrupt Endpoints)

Name: USBHS_DEVEPTICRx
Offset: 0x0160 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

This register view is relevant only if EPTYPE = 0x0, 0x2, or 0x3 in the "Device Endpoint x Configuration Register".

For additional information, see "Device Endpoint x Status Register (Control, Bulk, Interrupt Endpoints)".

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Clears the corresponding bit in USBHS_DEVEPTISRx.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	SHORTPACKETC	STALLEDIC	OVERFIC	NAKINIC	NAKOUTIC	RXSTPIC	RXOUTIC	TXINIC
Access								
Reset	0	0	0	0	0	0	0	0

Bit 7 – SHORTPACKETC Short Packet Interrupt Clear

Bit 6 – STALLEDIC STALLed Interrupt Clear

Bit 5 – OVERFIC Overflow Interrupt Clear

Bit 4 – NAKINIC NAKed IN Interrupt Clear

Bit 3 – NAKOUTIC NAKed OUT Interrupt Clear

Bit 2 – RXSTPIC Received SETUP Interrupt Clear

40.14.15 HSMCI Interrupt Mask Register

Name: HSMCI_IMR
Offset: 0x4C
Reset: 0x0
Property: Read-only

The following configuration values are valid for all listed bit names of this register:

0: The corresponding interrupt is not enabled.

1: The corresponding interrupt is enabled.

Bit	31	30	29	28	27	26	25	24
	UNRE	OVRE	ACKRCVE	ACKRCV	XFRDONE	FIFOEMPTY		BLKOVRE
Access								
Reset	0	0	0	0	0	0		0

Bit	23	22	21	20	19	18	17	16
	CSTOE	DTOE	DCRCE	RTOE	RENDE	RCRCE	RDIRE	RINDE
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
			CSRCV	SDIOWAIT				SDIOIRQA
Access								
Reset			0	0				0

Bit	7	6	5	4	3	2	1	0
			NOTBUSY	DTIP	BLKE	TXRDY	RXRDY	CMDRDY
Access								
Reset			0	0	0	0	0	0

Bit 31 – UNRE Underrun Interrupt Mask

Bit 30 – OVRE Overrun Interrupt Mask

Bit 29 – ACKRCVE Boot Operation Acknowledge Error Interrupt Mask

Bit 28 – ACKRCV Boot Operation Acknowledge Received Interrupt Mask

Bit 27 – XFRDONE Transfer Done Interrupt Mask

Bit 26 – FIFOEMPTY FIFO Empty Interrupt Mask

Bit 24 – BLKOVRE DMA Block Overrun Error Interrupt Mask

Bit 23 – CSTOE Completion Signal Time-out Error Interrupt Mask

Bit 22 – DTOE Data Time-out Error Interrupt Mask

43.7.10 TWIHS Interrupt Disable Register

Name: TWIHS_IDR
Offset: 0x28
Reset: –
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			SMBHHM	SMBDAM	PECERR	TOUT		MCACK
Access			W	W	W	W		W
Reset			–	–	–	–		–

Bit	15	14	13	12	11	10	9	8
					EOSACC	SCL_WS	ARBLST	NACK
Access					W	W	W	W
Reset					–	–	–	–

Bit	7	6	5	4	3	2	1	0
	UNRE	OVRE	GACC	SVACC		TXRDY	RXRDY	TXCOMP
Access	W	W	W	W		W	W	W
Reset	–	–	–	–		–	–	–

Bit 21 – SMBHHM SMBus Host Header Address Match Interrupt Disable

Bit 20 – SMBDAM SMBus Default Address Match Interrupt Disable

Bit 19 – PECERR PEC Error Interrupt Disable

Bit 18 – TOUT Timeout Error Interrupt Disable

Bit 16 – MCACK Master Code Acknowledge Interrupt Disable

Bit 11 – EOSACC End Of Slave Access Interrupt Disable

Bit 10 – SCL_WS Clock Wait State Interrupt Disable

Bit 9 – ARBLST Arbitration Lost Interrupt Disable

Bit 8 – NACK Not Acknowledge Interrupt Disable

- LIN Mode
  - Compliant with LIN 1.3 and LIN 2.0 SPECIFICATIONS
  - Master or Slave
  - Processing of Frames with Up to 256 Data Bytes
  - Response Data Length can be Configurable or Defined Automatically by the Identifier
  - Self-synchronization in Slave Node Configuration
  - Automatic Processing and Verification of the “Synch Break” and the “Synch Field”
  - “Synch Break” Detection Even When Partially Superimposed with a Data Byte
  - Automatic Identifier Parity Calculation/Sending and Verification
  - Parity Sending and Verification Can be Disabled
  - Automatic Checksum Calculation/sending and Verification
  - Checksum Sending and Verification Can be Disabled
  - Support Both “Classic” and “Enhanced” Checksum Types
  - Full LIN Error Checking and Reporting
  - Frame Slot Mode: Master Allocates Slots to the Scheduled Frames Automatically
  - Generation of the Wakeup Signal
- LON Mode
  - Compliant with CEA-709 Specification
  - Full-layer 2 Implementation
  - Differential Manchester Encoding/Decoding (CDP)
  - Preamble Generation Including Bit- and Byte-sync Fields
  - LON Timings Handling (beta1, beta2, IDT, etc.)
  - CRC Generation and Checking
  - Automated Random Number Generation
  - Backlog Calculation and Update
  - Collision Detection Support
  - Supports Both comm_type=1 and comm_type=2 Modes
  - Clock Drift Tolerance Up to 16%
  - Optimal for Node-to-Node Communication (no embedded digital line filter)
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo
- Supports Connection of:
  - Two DMA Controller Channels (DMAC)
- Offers Buffer Transfer without Processor Intervention
- Register Write Protection

Note: All reserved Channel Descriptor bits must be written to ‘0’ by software when initialized.

Synchronous Channel Operation

The MLB provides two modes of operation (Standard and Multi-Frame per Sub- buffer) to provide flexibility for implementing synchronous channels.

Channels set up for Standard mode require less buffer space, but have higher interrupt rates and more stringent latency requirements. For channels configured for Standard mode, the Host Controller must transfer one full frame of streaming data in/out of each streaming channel's data buffer for each frame period.

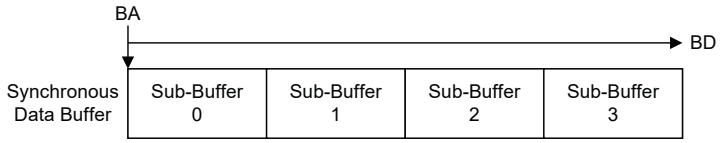
Channels set up for Multi-Frame per Sub-buffer mode require more buffer space, but have lower interrupt rates and less stringent latency requirements. For channels configured for Multi-Frame per Sub-buffer mode, the Host Controller must transfer N full frames of streaming data in/out of each streaming channel's data buffer for each frame period.

To set up a channel in Multi-Frame per Sub-buffer mode:

- Program MLB_MLBC0.FCNT[2:0] to select the number of frames per sub-buffer
- Program the CAT to enable multi-frame sub-buffering (MFE = 1) for each particular channel
- Set the buffer depth in the CDT: BD = 4 × m × bpf - 1,
  where m = frames per sub- buffer, bpf = bytes per frame
- Repeat for additional synchronous channels

A sample synchronous data buffer is shown in the following figure. Each data buffer contains four sub-buffers and each sub-buffer contains space for 1 to 64 frames of data, determined by MLB_MLBC0.FCNT[2:0].

Figure 48-17. Synchronous Data Buffer Structure



Synchronous Channel Descriptors

The format and field definitions for a synchronous CDT entry are shown in Table 48-14 and Table 48-14, respectively.

Table 48-14. Synchronous CDT Entry Format

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	WSBC		Reserved													
16	RSBC		Reserved													
32	Reserved															
48	Reserved															
64	WSTS[3:0]				WPTR[11:0]											
80	RSTS[3:0]				RPTR[11:0]											
96	Reserved				BD[11:0]											
112	Reserved		BA[13:0]													

4. Program the CAT for the inbound DMA
    4.1. For Tx channels (to MediaLB) HBI is the inbound DMA
    4.2. For Rx channels (from MediaLB) MediaLB is the inbound DMA
    4.3. Set the channel direction: RNW = 0
    4.4. Set the channel type:
    CT[2:0] = 010 (asynchronous), 001 (control), 011 (isochronous), or 000 (synchronous)
    4.5. Set the connection label: CL[5:0] = N
    4.6. If CT[2:0] = 000 (synchronous), set the mute bit (MT = 1)
    4.7. Set the channel enable: CE = 1
    4.8. Set all other bits of the CAT to ‘0’
5. Program the CAT for the outbound DMA
    5.1. For Tx channels (to MediaLB) MediaLB is the outbound DMA
    5.2. For Rx channels (from MediaLB) HBI is the outbound DMA
    5.3. Set the channel direction: RNW = 1
    5.4. Set the channel type: CT[2:0] = 010 (asynchronous), 001 (control), 011 (isochronous), or 000 (synchronous)
    5.5. Set the channel label: CL[5:0] = N
    5.6. If CT[2:0] = 000 (synchronous), set the mute bit (MT = 1)
    5.7. Set the channel enable: CE = 1
    5.8. Set all other bits of the CAT to ‘0’
6. Repeat steps 2–5 to initialize all logical channels

Program the AHB Block DMAs

The ADT resides in the external CTR and is programmed indirectly via APB reads and writes to the MIF.

1. Initialize all bits of the ADT to ‘0’
2. Select a logical channel: N = 0–63
3. Program the AHB block ping page for channel N
    3.1. Set the 32-bit base address (BA1)
    3.2. Set the 11-bit buffer depth (BD1): BD1 = buffer depth in bytes - 1
        3.2.1. For synchronous channels: (BD1 + 1) = n x frames per sub-buffer (m) x bytes-per-frame (bpf)
        3.2.2. For isochronous channels: (BD1 + 1) mod (BS + 1) = 0
        3.2.3. For asynchronous channels: 5 ≤ (BD1 + 1) ≤ 4096 (max packet length)
        3.2.4. For control channels: 5 ≤ (BD1 + 1) ≤ 4096 (max packet length)
    3.3. For asynchronous and control Tx channels set the packet start bit (PS1) iff the page contains the start of the packet
    3.4. Clear the page done bit (DNE1)
    3.5. Clear the error bit (ERR1)
    3.6. Set the page ready bit (RDY1)
4. Program the AHB block pong page for channel N
    4.1. Set the 32-bit base address (BA2)
    4.2. Set the 11-bit buffer depth (BD2): BD2 = buffer depth in bytes - 1
        4.2.1. For synchronous channels: (BD2 +1) = n x frames per sub-buffer (m) x bytes-per-frame (bpf)

49.6.31 MCAN Receive FIFO 1 Configuration

Name: MCAN_RXF1C
Offset: 0xB0
Reset: 0x00000000
Property: Read/Write

This register can only be written if the bits CCE and INIT are set in MCAN CC Control Register.

Bit	31	30	29	28	27	26	25	24
	F1OM	F1WM[6:0]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
		F1S[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	F1SA[13:6]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	F1SA[5:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit 31 – F1OM FIFO 1 Operation Mode
FIFO 1 can be operated in Blocking or in Overwrite mode (see Rx FIFOs).

Value	Description
0	FIFO 1 Blocking mode.
1	FIFO 1 Overwrite mode.

Bits 30:24 – F1WM[6:0] Receive FIFO 1 Watermark

Value	Description
0	Watermark interrupt disabled
1-64	Level for Receive FIFO 1 watermark interrupt (MCAN_IR.RF1W).
>64	Watermark interrupt disabled.

Bits 22:16 – F1S[6:0] Receive FIFO 1 Size
The elements in Receive FIFO 1 are indexed from 0 to F1S - 1.

Value	Description
0	No Receive FIFO 1
1-64	Number of elements in Receive FIFO 1.
>64	Values greater than 64 are interpreted as 64.

53.7.11 DACC Interrupt Status Register

Name: DACC_ISR
Offset: 0x30
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			EOC1	EOC0			TXRDY1	TXRDY0
Access			R	R			R	R
Reset			0	0			0	0

Bits 4, 5 – EOCx End of Conversion Interrupt Flag of channel x

Value	Description
0	No conversion has been performed since the last read of DACC_ISR.
1	At least one conversion has been performed since the last read of DACC_ISR.

Bits 0, 1 – TXRDYx Transmit Ready Interrupt Flag of channel x

Value	Description
0	DACC is not ready to accept new conversion requests.
1	DACC is ready to accept new conversion requests.

53.7.13 DACC Write Protection Mode Register

Name: DACC_WPMR
Offset: 0xE4
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	WPKEY[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	WPKEY[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	WPKEY[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–
Bit	7	6	5	4	3	2	1	0
								WPEN
Access								R/W
Reset								0

Bits 31:8 – WPKEY[23:0] Write Protect Key

Value	Name	Description
0x444143	PASSWD	Writing any other value in this field aborts the write operation of bit WPEN. Always reads as 0.

Bit 0 – WPEN Write Protection Enable
See Register Write Protection for list of write-protected registers.

Value	Description
0	Disables the write protection if WPKEY corresponds to 0x444143 (“DAC” in ASCII).
1	Enables the write protection if WPKEY corresponds to 0x444143 (“DAC” in ASCII).

Date	Changes
	Section 46. ”Universal Synchronous Asynchronous Receiver Transceiver (USART)” Section 46.4 ”I/O Lines Description”: removed mention of USART3 as fully equipped with modem signals. Updated Figure 46-27 “RTS Line Software Control when US_MR.USART_MODE = 2” Section 46.7.17 ”USART Channel Status Register”: updated RTSDIS description.
	Section 49. ”Controller Area Network (MCAN)” Section 49.1 ”Description”: updated information on compliance. Updated Table 49-2 “Peripheral IDs” .
	Section 50. ”Timer Counter (TC)” Section 50.6.16.2 ”Input Preprocessing”: removed unit following equation in 3rd paragraph. Added limitation on maximum pulse duration. Section 50.6.16.4 ”Position and Rotation Measurement”: in 3rd paragraph, added “The process must be started by configuring TC_CCR.CLKEN and TC_CCR.SWTRG.” “Detecting a Missing Index Pulse” now Section 50.6.16.6 (was Section 50.6.17). Corrected value of TC_RC0.RC in example in 2nd paragraph. Added Section 50.6.16.7 ”Detecting Contamination/Dust at Rotary Encoder Low Speed”. Section 50.7.16 ”TC Block Mode Register”: added AUTOC at index 18 and bit description. Added MAXCMP at index [29:26] and field description. Updated MAXFILT field description. Section 50.7.17 ”TC QDEC Interrupt Enable Register”, Section 50.7.17 ”TC QDEC Interrupt Enable Register”, Section 50.7.17 ”TC QDEC Interrupt Enable Register” and Section 50.7.17 ”TC QDEC Interrupt Enable Register”: added bit MPE at index 3 and bit description
	Section 51. ”Pulse Width Modulation Controller (PWM)” Throughout, “PWMTRG” and “EXTTRG” renamed to “PWMEXTRG”. Updated Figure 51-1 “Pulse Width Modulation Controller Block Diagram”. Updated section “Recoverable Fault”. Updated Figure 51-16 “Fault Protection”. Section 51.6.7 ”Register Write Protection”: added PWM_IER1, PWM_IDR1, PWM_IER2 and PWM_IDR2 to list of write-protected registers in Register group 1. Section 51-8 ”Register Mapping”: modified offsets for “PWM External Trigger Register 1”, “PWM Leading-Edge Blanking Register 1”, “PWM External Trigger Register 2” and “PWM Leading-Edge Blanking Register 2”. Section 51.7.5 ”PWM Interrupt Enable Register 1”, Section 51.7.6 ”PWM Interrupt Disable Register 1”, Section 51.7.14 ”PWM Interrupt Enable Register 2”, Section 51.7.15 ”PWM Interrupt Disable Register 2”: below each register table, added “This register can only be written if bits WPSWS1 and WPHWS1 are cleared in the PWM Write Protection Status Register.”
12-Oct-16	Section 52. ”Analog Front-End Controller (AFEC)” Section 52.5.7 ”Fault Output”: updated section with details on AFEC_TEMPMR and