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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70q20b-cfnt

2. PIODCEN1/PIODCx has priority over WKUPx. Refer to the 32.5.14 Parallel Capture Mode section in the PIO chapter.
3. Refer to the 23.4.2 Slow Clock Generator section in the Supply Controller (SUPC) chapter.
4. To select this extra function, refer to the 33.5.2.1 I/O Lines section in the External Bus Interface (EBI) chapter. This selection is independent of the PIO line configuration. PIO lines must be configured according to required settings (PU or PD).
5. Analog input has priority over WKUPx pin. To select the analog input, refer to the 33.5.2.1 I/O Lines section in the EBI chapter. WKUPx can be used if the PIO controller defines the I/O line as “input”.
6. Analog input has priority over RTCOUTx pin. To select the analog input, refer to the 33.5.2.1 I/O Lines section in the EBI chapter. Refer to the 27.5.8 Waveform Generation section in the Real-Time Clock (RTC) chapter to select RTCOUTx.
7. Analog input has priority over WKUPx pin. To select the analog input, refer to the 33.5.2.1 I/O Lines section in the EBI chapter. To select PIODCEN2, refer to the 32.5.14 Parallel Capture Mode in the PIO chapter.
8. Refer to the System I/O Configuration Register (19.4.7 CCFG_SYSIO) in the Bus Matrix (MATRIX) chapter.
9. Refer to the 30.5.3 Main Crystal Oscillator section in the Clock Generator chapter. This selection is independent of the PIO line configuration. PIO lines must be configured according to XINxx (I) and XOUTxx (O).
10. DAC0 is selected when DACC_CHER.CH0 is set. DAC1 is selected when DACC_CHER.CH1 is set. Refer to the DACC Channel Enable Register in the Digital-to-Analog Converter Controller (DACC) chapter.
11. The exposed pad of the QFN64 package MUST be connected to ground.

Mode	SUPC, 32 kHz Oscillator, RTC, RTT Backup SRAM (BRAM), Backup Registers (GPBR), POR (Backup Area)	Regulator	Core Memory Peripherals	Mode Entry Configuration	Potential Wakeup Sources	Core at Wakeup	PIO State while in Low-Power Mode	PIO State at Wakeup	Wakeup Time (see Note 2)
					RTC alarm RTT alarm			inputs with pullups	
Wait Mode w/Flash in Deep Power-down Mode	ON	ON	Powered (Not clocked)	PMC_MCKR.MDIV = 0 , CKGR_MOR.WAITMODE =1 , SLEEPDEEP = 0 , PMC_FSMR.LPM = 1 , PMC_FSMR.FLPM = 1 (see **Note 1)**	WKUP0–13 pins RTC RTT USBHS Processor debug (see **Note 6**) GMAC Wake on LAN event Wakeup from CAN (see **Note 7**)	Clocked back (see **Note 3**)	Previous state maintained	Unchanged	< 10 µs
Wait Mode w/Flash in Standby Mode	ON	ON	Powered (Not clocked)	PMC_MCKR.MDIV = 0 , CKGR_MOR.WAITMODE =1 , SLEEPDEEP = 0 , PMC_FSMR.LPM = 1 , PMC_FSMR.FLPM = 0 (see **Note 1**)	WKUP0–13 pins RTC RTT USBHS Processor debug (see **Note 6)** GMAC Wake on LAN Wakeup from CAN (see **Note 7**)	Clocked back (see **Note 3**)	Previous state maintained	Unchanged	< 10 µs
Sleep Mode	ON	ON	Powered (Not clocked) (see **Note 4**)	WFI SLEEPDEEP = 0 PMC_FSMR.LPM = 0 (see **Note 1**)	Any enabled Interrupt	Clocked back	Previous state maintained	Unchanged	(see **Note 5**)

Note:

1. The bit SLEEPDEEP is in the Cortex-M7 System Control Register.
2. When considering wakeup time, the time required to start the PLL is not taken into account. Once started, the device works with the Main RC oscillator. The user has to add the PLL startup time if it is needed in the system. The wakeup time is defined as the time taken for wakeup until the first instruction is fetched.
3. HCLK = MCK. The user may need to revert back to the previous clock configuration.
4. Depends on MCK frequency.
5. In this mode, the core is supplied and not clocked. Some peripherals can be clocked.
6. Resume from Wait mode if a debug request occurs (CDBGPWRUPREQ is set in the processor).
7. CAN wake-up requires the use of any WKUP0–13 pin.

7.7 Wakeup Sources

Wakeup events allow the device to exit Backup mode. When a wakeup event is detected, the Supply Controller performs a sequence which automatically reenables the core power supply and the SRAM power supply, if they are not already enabled.

21.3.2 Chip ID Extension Register

Name: CHIPID_EXID
Offset: 0x4
Reset: -
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	EXID[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	EXID[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	EXID[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	EXID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 31:0 – EXID[31:0] Chip ID Extension
This field is cleared if CHIPID_CIDR.EXT = 0.

Value	Name	Description
0xX	Reserved	Reserved

32.6.1.2 PIO Disable Register

Name: PIO_PDR
Offset: 0x0004
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Disable

Value	Description
0	No effect.
1	Disables the PIO from controlling the corresponding pin (enables peripheral control of the pin).

35.16.1.3 SMC Cycle Register

Name: SMC_CYCLE[0..3]
Offset: 0x00
Reset: 0
Property: R/W

This register can only be written if the WPEN bit is cleared in the “SMC Write Protection Mode Register” .

Bit	31	30	29	28	27	26	25	24
								NRD_CYCLE[8:8]
Access								
Reset								0

Bit	23	22	21	20	19	18	17	16
	NRD_CYCLE[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
								NWE_CYCLE[8:8]
Access								
Reset								0

Bit	7	6	5	4	3	2	1	0
	NWE_CYCLE[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 24:16 – NRD_CYCLE[8:0] Total Read Cycle Length
The total read cycle length is the total duration in clock cycles of the read cycle. It is equal to the sum of the setup, pulse and hold steps of the NRD and NCS signals. It is defined as:

Read cycle length = (NRD_CYCLE[8:7]*256 + NRD_CYCLE[6:0]) clock cycles

Bits 8:0 – NWE_CYCLE[8:0] Total Write Cycle Length
The total write cycle length is the total duration in clock cycles of the write cycle. It is equal to the sum of the setup, pulse and hold steps of the NWE and NCS signals. It is defined as:

Write cycle length = (NWE_CYCLE[8:7]*256 + NWE_CYCLE[6:0]) clock cycles

Offset	Name	Bit Pos.								
		31:24								
0x0570	XDMAC_CUBC20	7:0	UBLEN[7:0]							
		15:8	UBLEN[15:8]							
		23:16	UBLEN[23:16]							
		31:24								
0x0574	XDMAC_CBC20	7:0	BLEN[7:0]							
		15:8					BLEN[11:8]			
		23:16								
		31:24								
0x0578	XDMAC_CC20	7:0	MEMSET	SWREQ		DSYNC		MBSIZE[1:0]		TYPE
		15:8		DIF	SIF	DWIDTH[1:0]		CSIZE[2:0]		
		23:16	WRIP	RDIP	INITD		DAM[1:0]		SAM[1:0]	
		31:24		PERID[6:0]						
0x057C	XDMAC_CDS_MSP20	7:0	SDS_MSP[7:0]							
		15:8	SDS_MSP[15:8]							
		23:16	DDS_MSP[7:0]							
		31:24	DDS_MSP[15:8]							
0x0580	XDMAC_CSUS20	7:0	SUBS[7:0]							
		15:8	SUBS[15:8]							
		23:16	SUBS[23:16]							
		31:24								
0x0584	XDMAC_CDUS20	7:0	DUBS[7:0]							
		15:8	DUBS[15:8]							
		23:16	DUBS[23:16]							
		31:24								
0x0588 ... 0x058F	Reserved									
0x0590	XDMAC_CIE21	7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
		15:8								
		23:16								
		31:24								
0x0594	XDMAC_CID21	7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
		15:8								
		23:16								
		31:24								
0x0598	XDMAC_CIM21	7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
		15:8								
		23:16								
		31:24								
0x059C	XDMAC_CIS21	7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
		15:8								
		23:16								
		31:24								
0x05A0	XDMAC_CSA21	7:0	SA[7:0]							
		15:8	SA[15:8]							

36.9.15 XDMAC Global Channel Software Request Register

Name: XDMAC_GSWR
Offset: 0x38
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	SWREQ23	SWREQ22	SWREQ21	SWREQ20	SWREQ19	SWREQ18	SWREQ17	SWREQ16
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bit	15	14	13	12	11	10	9	8
	SWREQ15	SWREQ14	SWREQ13	SWREQ12	SWREQ11	SWREQ10	SWREQ9	SWREQ8
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

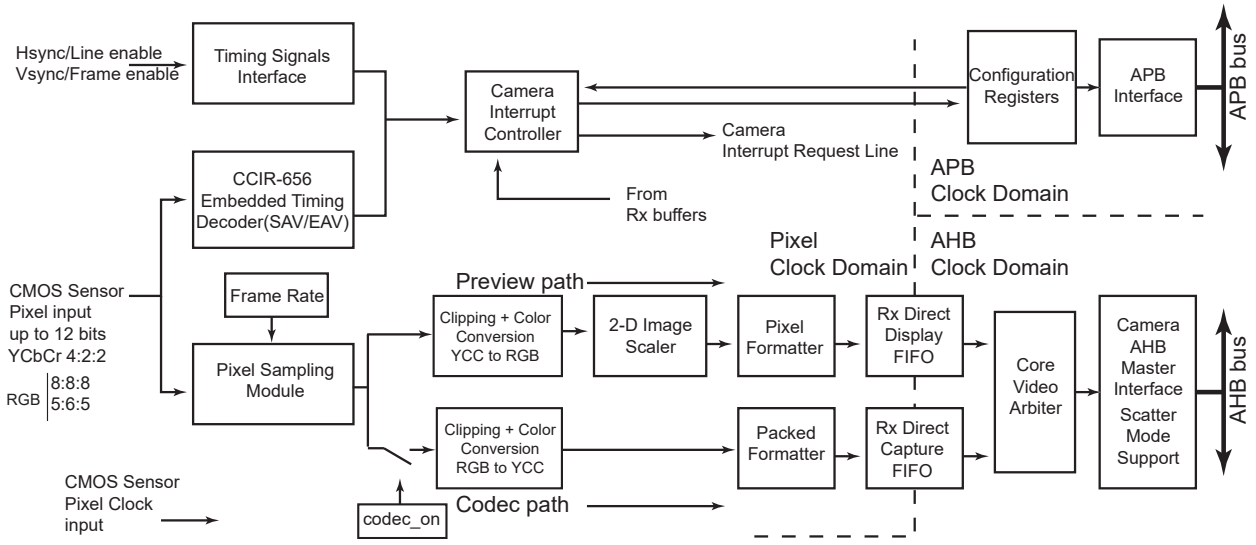
Bit	7	6	5	4	3	2	1	0
	SWREQ7	SWREQ6	SWREQ5	SWREQ4	SWREQ3	SWREQ2	SWREQ1	SWREQ0
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 – SWREQ XDMAC Channel x Software Request

Value	Description
0	No effect.
1	Requests a DMA transfer for channel x.

37.3 Block Diagram

Figure 37-2. ISI Block Diagram



37.4 Product Dependencies

37.4.1 I/O Lines

The pins used for interfacing the compliant external devices can be multiplexed with PIO lines. The programmer must first program the PIO controllers to assign the ISI pins to their peripheral functions.

37.4.2 Power Management

The ISI can be clocked through the Power Management Controller (PMC), thus the programmer must first configure the PMC to enable the ISI clock.

37.4.3 Interrupt Sources

The ISI interface has an interrupt line connected to the interrupt controller. Handling the ISI interrupt requires programming the interrupt controller before configuring the ISI.

37.5 Functional Description

The Image Sensor Interface (ISI) supports direct connection to the ITU-R BT. 601/656 8-bit mode compliant sensors and up to 12-bit grayscale sensors. It receives the image data stream from the image sensor on the 12-bit data bus.

This module receives up to 12 bits for data, the horizontal and vertical synchronizations and the pixel clock. The reduced pin count alternative for synchronization is supported for sensors that embed SAV (start of active video) and EAV (end of active video) delimiters in the data stream.

The Image Sensor Interface interrupt line is connected to the Advanced Interrupt Controller and can trigger an interrupt at the beginning of each frame and at the end of a DMA frame transfer. If the SAV/EAV synchronization is used, an interrupt can be triggered on each delimiter event.

For 8-bit color sensors, the data stream received can be in several possible formats: YCbCr 4:2:2, RGB 8:8:8, RGB 5:6:5 and may be processed before the storage in memory. When the preview DMA channel

Table 38-12. Example of Sync Frame in 1588 Version 2 (Ethernet Multicast) Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	011B19000000
SA (Octets 6–11)	—
Type (Octets 12–13)	88F7
Message type (Octet 14)	00
Version PTP (Octet 15)	02

Pdelay request frames need a special multicast address so they can pass through ports blocked by the spanning tree protocol. For the multicast address 0180C200000E sync, Pdelay_Req and Pdelay_Resp frames are recognized depending on the message type field, 00 for sync, 02 for pdelay request and 03 for pdelay response.

Table 38-13. Example of Pdelay_Req Frame in 1588 Version 2 (Ethernet Multicast) Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	0180C200000E
SA (Octets 6–11)	—
Type (Octets 12–13)	88F7
Message type (Octet 14)	00
Version PTP (Octet 15)	02

38.6.15 Time Stamp Unit

Overview

The TSU consists of a timer and registers to capture the time at which PTP event frames cross the message timestamp point. An interrupt is issued when a capture register is updated.

The 1588 time stamp unit (TSU) is implemented as a 94-bit timer.

- The 48 upper bits [93:46] of the timer count seconds and are accessible in the GMAC 1588 Timer Seconds High Register” (GMAC_TSH) and GMAC 1588 Timer Seconds Low Register (GMAC_TSL).
- The 30 lower bits [45:16] of the timer count nanoseconds and are accessible in the GMAC 1588 Timer Nanoseconds Register (GMAC_TN).
- The lowest 16 bits [15:0] of the timer count sub-nanoseconds.

The 46 lower bits roll over when they have counted to 1s. An interrupt is generated when the seconds increment. The timer increments by a programmable period (to approximately 15.2fs resolution) with each MCK period. The timer value can be read, written and adjusted with 1ns resolution (incremented or decremented) through the APB interface.

38.8.76 GMAC Receive Symbol Errors Register

Name: GMAC_RSE
Offset: 0x198
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							RXSE[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	RXSE[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – RXSE[9:0] Receive Symbol Errors
This bit field counts the number of frames that had GRXER asserted during reception. For 10/100 mode symbol errors are counted regardless of frame length checks. Receive symbol errors will also be counted as an FCS or alignment error if the frame is between 64 and 1518 Bytes (1536 Bytes if GMAC_NCFGR.MAXFS=1). If the frame is larger it will be recorded as a jabber error.

Value	Description
0	Cleared when USBHS_HSTPIPICR.RXINIC = 1.
1	Set when a new USB message is stored in the current bank of the pipe. This triggers an interrupt if USBHS_HSTPIPIMR.RXINE = 1.

39.6.66 Host DMA Channel x Address Register

Name: USBHS_HSTDMAADDRESSx
Offset: 0x0704 + x*0x10 [x=0..6]
Reset: 0
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	BUFF_ADD[31:24]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	BUFF_ADD[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	BUFF_ADD[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	BUFF_ADD[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – BUFF_ADD[31:0] Buffer Address
This field determines the AHB bus starting address of a DMA channel transfer.

Channel start and end addresses may be aligned on any byte boundary.

The firmware can write this field only when the USBHS_HSTDMASTATUS.CHANN_ENB bit is cleared.

This field is updated at the end of the address phase of the current access to the AHB bus. It is incremented by the access byte width. The access width is 4 bytes (or less) at packet start or end, if the start or end address is not aligned on a word boundary.

The packet start address is either the channel start address or the next channel address to be accessed in the channel buffer.

The packet end address is either the channel end address or the latest channel address accessed in the channel buffer.

The channel start address is written by software or loaded from the descriptor. The channel end address is either determined by the end of buffer or the USB device, or by the USB end of transfer if the USBHS_HSTDMACONTROLx.END_TR_EN bit is set.

42.7.6 QSPI Interrupt Enable Register

Name: QSPI_IER
Offset: 0x14
Reset: –
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
						INSTRE	CSS	CSR
Access						W	W	W
Reset						–	–	–

Bit	7	6	5	4	3	2	1	0
					OVRES	TXEMPTY	TDRE	RDRF
Access					W	W	W	W
Reset					–	–	–	–

Bit 10 – INSTRE Instruction End Interrupt Enable

Bit 9 – CSS Chip Select Status Interrupt Enable

Bit 8 – CSR Chip Select Rise Interrupt Enable

Bit 3 – OVRES Overrun Error Interrupt Enable

Bit 2 – TXEMPTY Transmission Registers Empty Enable

Bit 1 – TDRE Transmit Data Register Empty Interrupt Enable

Bit 0 – RDRF Receive Data Register Full Interrupt Enable

- MLB_MADR.WNR = 1
- MLB_MADR.TB = 1
- MLB_MADR.ADDR[13:0] = 14-bit Target Address

The MIF block sets MLB_MCTL.XCMP = 1 to inform the HC when the write is complete.

Direct DBR Reads

For a direct read of the DBR, the HC initiates a read cycle by writing the address and control information to MLB_MADR as follows:

- MLB_MADR.WNR = 0
- MLB_MADR.TB = 1
- MLB_MADR.ADDR[13:0] = 14-bit target address

The MIF block sets MLB_MCTL.XCMP = 1 to inform the HC when the read is complete. The HC can then read the 8-bit data entry from the MLB_MDAT0 register at bits[7:0].

48.6.3.5 Interrupt Interface Block

The Interrupt Interface (INTIF) block performs a low-priority polling algorithm of each of the HBI channel descriptors.

The INTIF alerts the HBI block when specific changes to HBI Channel Descriptors occur.

- For asynchronous and control read/write channels:
  - a packet is available to read in the channel buffer, or
  - sufficient empty space is available in the channel buffer to accept a requested packet write.
- For isochronous read/write channels:
  - the number of valid bytes in the channel buffer exceeds the block size, or
  - the number of empty bytes in the channel buffer exceeds the block size.

48.6.3.6 AHB Block

The AHB block manages data exchange between local channel data buffers within the MLB and the system memory buffer.

To support system memory buffering, a ping-pong memory structure is implemented on a per-channel basis using 128-bit descriptors for AHB Descriptor Table (ADT) entries.

Note: The 64 ADT entries are directly mapped to the 64 HBI physical channels.

Each logical channel is assigned a separate 128-bit descriptor, defining the data buffers in the system memory used by the DMA interface for that channel. The descriptors are stored at fixed addresses in the external CTR.

AHB Descriptor Table

The following table provides an overview of field definitions for ADT entries.

Table 48-20. ADT Field Definitions

Field	No. of Bits	Description	Accessibility
CE	1	Channel enable: 0 = Disabled	r,w,u (1)

Value	Description
0	An asynchronous packet that is flagged with a Break or ProtocolError by the receiver is skipped.
1	An asynchronous packet that is flagged with a Break or ProtocolError by the receiver is retransmitted.

Bit 7 – MLBLK MediaLB Lock Status (read-only)

Value	Description
1	indicates that the MediaLB block is synchronized to the incoming MediaLB frame. If MLBLK is cleared (unlocked), MLBLK is set after FRAMESYNC is detected at the same position for three consecutive frames. If MLBLK is set (locked), MLBLK is cleared after not receiving FRAMESYNC at the expected time for two consecutive frames. While MLBLK is set, FRAMESYNC patterns occurring at locations other than the expected one are ignored.

Bit 5 – ZERO Must be Written to 0

Bits 4:2 – MLBCLK[2:0] MLBCLK (MediaLB clock) Speed Select

Value	Name	Description
0	256_FS	256xFs (for MLBPEN = 0)
1	512_FS	512xFs (for MLBPEN = 0)
2	1024_FS	1024xFs (for MLBPEN = 0)
3	2048_FS	2048xFs (for MLBPEN = 0)
4	3072_FS	3072xFs (for MLBPEN = 0)
5	4096_FS	4096xFs (for MLBPEN = 0)
6	6144_FS	6144xFs (for MLBPEN = 0)

Bit 0 – MLBEN MediaLB Enable

Value	Description
1	MLBCLK (MediaLB clock), MLBSIG (signal), and MLBDATA (data) are received and transmitted on the appropriate MediaLB pins.

49.6.43 MCAN Transmit Buffer Transmission Interrupt Enable

Name: MCAN_TXBTIE
Offset: 0xE0
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	TIE31	TIE30	TIE29	TIE28	TIE27	TIE26	TIE25	TIE24
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TIE23	TIE22	TIE21	TIE20	TIE19	TIE18	TIE17	TIE16
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TIE15	TIE14	TIE13	TIE12	TIE11	TIE10	TIE9	TIE8
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TIE7	TIE6	TIE5	TIE4	TIE3	TIE2	TIE1	TIE0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – TIEx Transmission Interrupt Enable for Buffer x
Each Transmit Buffer has its own Transmission Interrupt Enable bit.

Value	Description
0	Transmission interrupt disabled
1	Transmission interrupt enable

50.7.16 TC Block Mode Register

Name: TC_BMR
Offset: 0xC4
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the TC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
			MAXCMP[3:0]				MAXFILT[5:4]	
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	MAXFILT[3:0]					AUTOC	IDXPHB	SWAP
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	15	14	13	12	11	10	9	8
	INVIDX	INVB	INVA	EDGPHA	QDTRANS	SPEEDEN	POSEN	QDEN
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			TC2XC2S[1:0]		TC1XC1S[1:0]		TC0XC0S[1:0]	
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 29:26 – MAXCMP[3:0] Maximum Consecutive Missing Pulses

Value	Description
0	The flag MPE in TC_QISR never rises.
1–15	Defines the number of consecutive missing pulses before a flag report.

Bits 25:20 – MAXFILT[5:0] Maximum Filter
Pulses with a period shorter than MAXFILT+1 peripheral clock cycles are discarded. For more details on MAXFILT constraints, see "Input Preprocessing"

Value	Description
1–63	Defines the filtering capabilities.

Bit 18 – AUTOC AutoCorrection of missing pulses
0 (DISABLED): The detection and autocorrection function is disabled.

1 (ENABLED): The detection and autocorrection function is enabled.

Bit 17 – IDXPHB Index Pin is PHB Pin

51.6.2.7.1 Recoverable Fault

The PWM provides a Recoverable Fault mode on fault 1 and 2 (see figure *Fault Protection*).

The recoverable fault signal is an internal signal generated as soon as an external trigger event occurs (see PWM External Trigger Mode).

When the fault 1 or 2 is defined as a recoverable fault, the corresponding fault input pin is ignored and bits FFIL1/2, FMOD1/2 and FFIL1/2 are not taken into account.

The fault 1 is managed as a recoverable fault by the PWMEXTRG1 input trigger when PWM_ETRG1.RFEN = 1, PWM_ENA.CHID1 = 1, and PWM_ETRG1.TRGMODE ≠ 0.

The fault 2 is managed as a recoverable fault by the PWMEXTRG2 input trigger when PWM_ETRG2.RFEN = 1, PWM_ENA.CHID2 = 1, and PWM_ETRG2.TRGMODE ≠ 0.

Recoverable fault 1 and 2 can be taken into account by all channels by enabling the bit FPEx[1/2] in the PWM Fault Protection Enable registers (PWM_FPEx). However the synchronous channels (see Synchronous Channels) do not use their own fault enable bits, but those of the channel 0 (bits FPE0[1/2]).

When a recoverable fault is triggered (according to the PWM_ETRGx.TRGMODE setting), the PWM counter of the affected channels is not cleared (unlike in the classic fault protection mechanism) but the channel outputs are forced to the values defined by the fields FPVHx and FPVLx in the PWM Fault Protection Value Register 1 (PWM_FPV), as per table *Forcing Values of PWM Outputs by Fault Protection*. The output forcing is made asynchronously to the channel counter and lasts from the recoverable fault occurrence to the end of the next PWM cycle (if the recoverable fault is no longer present) (see the figure below).

The recoverable fault does not trigger an interrupt. The Fault Status FSy (with y = 1 or 2) is not reported in the PWM Fault Status Register when the fault y is a recoverable fault.

53.7.7 DACC Conversion Data Register

Name: DACC_CDRx
Offset: 0x1C + x*0x04 [x=0..1]
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
	DATA1[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DATA1[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bit	15	14	13	12	11	10	9	8
	DATA0[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA0[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bits 31:16 – DATA1[15:0] Data to Convert for channel x
If DACC_MR.WORD is set, DATA1 is written to the FIFO of channel x after DATA0.

Bits 15:0 – DATA0[15:0] Data to Convert for channel x
DATA0 is written to the FIFO of channel x.

Date	Changes
	Figure 50-7 “Analog Full Scale Ranges in Single-Ended/Differential Applications Versus Gain”: replaced all occurrences of VADVREF with VVREFP; replaced min ‘0’ value with VVREFN=0. Section 50.7.2 “AFEC Mode Register”: modified PRESCAL description.
24-Feb-15	Section 51. “Digital-to-Analog Converter (DACC)” Section 51.1 “Description”: removed information on refresh feature. Figure 51-1 “Block Diagram”: added VDDANA, VREFP and VREFN. Table 51-1 “DACC Signal Description”: added VREFP and VREFN to table. Section 51.2 “Embedded Characteristics”: removed bullet on refresh period. Added Section 51.5.1 “I/O Lines”. Section 51.6.3 “Analog Output Mode Selection”: corrected bit name for output modeselection to ‘DIFF’ from ‘ANA_MODE_SEL’ . Section 51.6.4 “Conversion Modes”: added details on enabling conversion modes. Removed bullet “Interpolated Mode”. Removed section 51.6.5 “Refresh Mode”. Updated Section 51.6.4.4 “Interpolation Mode”. Section 51.7.2 “DACC Mode Register”: removed field REFRESH and description. Bits 15:8 now reserved. Section 51.7.6 “DACC Channel Status Register”: modified DACRDYx bit descriptions. Section 51.7.11 “DACC Interrupt Status Register”: ENDTXx, TXBUFEx descriptions: corrected register name to ‘DACC_CDRx’ from ‘DACC _TCR or DACC_TNCR’.
	Section 52. “Analog Comparator Controller (ACC)” In text and in tables throughout this section, changed all occurrences of ADVREF to VREFP. Section 52.2 “Embedded Characteristics”: In bullet: “Four Voltage References...”, changed ADVREF to ‘External Voltage Reference’ Renamed Section 5. to “Signal Description” Removed Table 52-1 “List of External Analog Data Inputs” and note referring to this table.
	Section 53. “Integrity Check Monitor (ICM)” Section 53.1 “Description”: updated content. Renamed section “ICM SHA Engine” to “Using ICM as SHA Engine” and updated content. Added Section 53.5.4.1 “Settings for Simple SHA Calculation”. Section 53.5.2.2 “ICM Region Configuration Structure Member”: updated descriptions for RHIEN, DMIEN, BEIEN, WCIEN, ECIEN, SUIEN and MPROT. Section 53.6.1 “ICM Configuration Register”: updated descriptions for DAPROT and HAPROT. Section 53.6.3 “ICM Status Register”: updated descriptions for RAWRMDIS and RMDIS.