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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70q20b-cn

9. Interconnect

The system architecture is based on the ARM Cortex-M7 processor connected to the main AHB Bus Matrix, the embedded Flash, the multi-port SRAM and the ROM.

The 32-bit AHBP interface is a single 32-bit wide interface that accesses the peripherals connected on the main Bus Matrix. It is used only for data access. Instruction fetches are never performed on the AHBP interface. The bus, AHBP or AXIM, accessing the peripheral memory area [0x40000000 to 0x60000000] is selected in the AHBP control register.

The 32-bit AHBS interface provides system access to the ITCM, D1TCM, and D0TCM. It is connected on the main Bus Matrix and allows the XDMA to transfer from memory or peripherals to the instruction or data TCMs.

The 64-bit AXIM interface is a single 64-bit wide interface connected through two ports of the AXI Bridge to the main AHB Bus Matrix and to two ports of the multi-port SRAM. The AXIM interface allows:

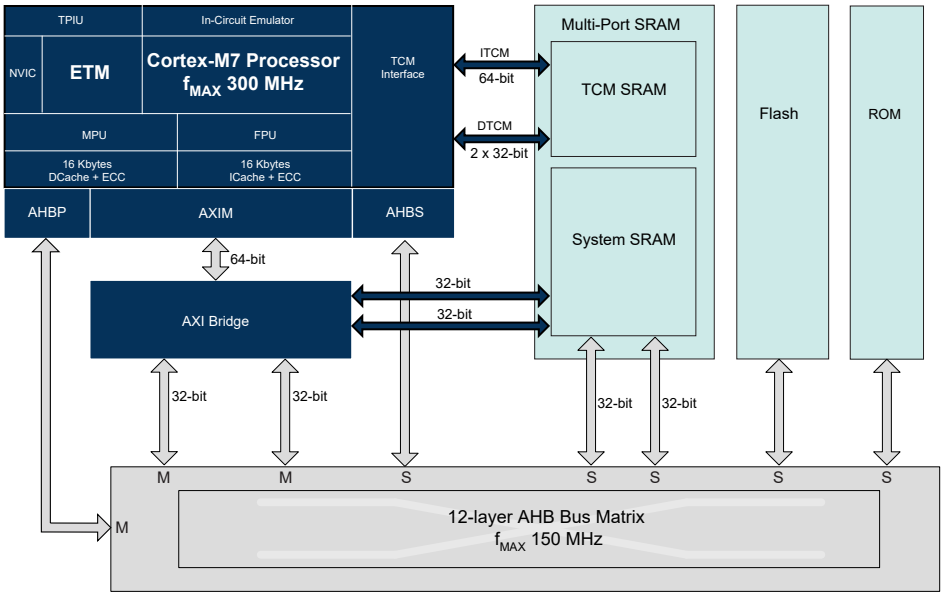
- Instruction fetches
- Data cache linefills and evictions
- Non-cacheable normal-type memory data accesses
- Device and strongly-ordered type data accesses, generally to peripherals

The interleaved multi-port SRAM optimizes the Cortex-M7 accesses to the internal SRAM.

The interconnect of the other masters and slaves is described in 19. Bus Matrix (MATRIX).

The figure below shows the connections of the different Cortex-M7 ports.

Figure 9-1. Interconnect Block Diagram



23.4 Functional Description

23.4.1 Overview

The device is divided into two power supply areas:

- VDDIO power supply: includes the Supply Controller, part of the Reset Controller, the slow clock switch, the general-purpose backup registers, the supply monitor and the clock which includes the Real-time Timer and the Real-time Clock.
- Core power supply: includes part of the Reset Controller, the Brownout Detector, the processor, the SRAM memory, the Flash memory and the peripherals.

The Supply Controller (SUPC) controls the supply voltage of the core power supply. The SUPC intervenes when the VDDIO power supply rises (when the system is starting) or when Backup mode is entered.

The SUPC also integrates the slow clock generator, which is based on a 32.768 kHz crystal oscillator, and a slow RC oscillator. The slow clock defaults to the slow RC oscillator, but the software can enable the 32.768 kHz crystal oscillator and select it as the slow clock source.

The SUPC and the VDDIO power supply have a reset circuitry based on a zero-power power-on reset cell. The zero-power power-on reset allows the SUPC to start correctly as soon as the VDDIO voltage becomes valid.

At startup of the system, once the backup voltage VDDIO is valid and the slow RC oscillator is stabilized, the SUPC starts up the core by sequentially enabling the internal voltage regulator. The SUPC waits until the core voltage VDDCORE is valid, then releases the reset signal of the core vddcore_nreset signal.

Once the system has started, the user can program a supply monitor and/or a brownout detector. If the supply monitor detects a voltage level on VDDIO that is too low, the SUPC asserts the reset signal of the core vddcore_nreset signal until VDDIO is valid. Likewise, if the brownout detector detects a core voltage level VDDCORE that is too low, the SUPC asserts the reset signal vddcore_nreset until VDDCORE is valid.

When Backup mode is entered, the SUPC sequentially asserts the reset signal of the core power supply vddcore_nreset and disables the voltage regulator, in order to supply only the VDDIO power supply. Current consumption is reduced to a few microamps for the backup part retention. Exit from this mode is possible on multiple wakeup sources including an event on WKUP pins, or a clock alarm. To exit this mode, the SUPC operates in the same way as system startup.

23.4.2 Slow Clock Generator

The SUPC embeds a slow clock generator that is supplied with the VDDIO power supply. As soon as the VDDIO is supplied, both the 32.768 kHz crystal oscillator and the slow RC oscillator are powered up, but only the slow RC oscillator is enabled. When the slow RC oscillator is selected as the slow clock source, the slow clock stabilizes more quickly than when the 32.768 kHz crystal oscillator is selected.

The user can select the 32.768 kHz crystal oscillator to be the source of the slow clock, as it provides a more accurate frequency than the slow RC oscillator. The 32.768 kHz crystal oscillator is selected by setting the XTALSEL bit in the SUPC Control register (SUPC_CR). The following sequence must be used to switch from the slow RC oscillator to the 32.768 kHz crystal oscillator:

1. The PIO lines multiplexed with XIN32 and XOUT32 are configured to be driven by the oscillator.
2. The 32.768 kHz crystal oscillator is enabled.

26.4.5.3 RSTC Mode Register

Name: RSTC_MR
Offset: 0x08
Reset: 0x00000001
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the System Controller Write Protection Mode Register (SYSC_WPMR).

Bit	31	30	29	28	27	26	25	24
	KEY[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					ERSTL[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
				URSTIEN				URSTEN
Access				R/W				R/W
Reset				0				1

Bits 31:24 – KEY[7:0] Write Access Password

Value	Name	Description
0xA5	PASSWD	Writing any other value in this field aborts the write operation. Always reads as 0.

Bits 11:8 – ERSTL[3:0] External Reset Length
This field defines the external reset length. The external reset is asserted during a time of $2^{(ERSTL+1)}$ SLCK cycles. This allows assertion duration to be programmed between 60 µs and 2 seconds. Note that synchronization cycles must also be considered when calculating the actual reset length as previously described.

Bit 4 – URSTIEN User Reset Interrupt Enable

Value	Description
0	RSTC_SR.USRTS at ‘1’ has no effect on the RSTC interrupt line.
1	RSTC_SR.USRTS at ‘1’ asserts the RSTC interrupt line if URSTEN = 0.

Bit 0 – URSTEN User Reset Enable

30. Clock Generator

30.1 Description

The Clock Generator user interface is embedded within the Power Management Controller and is described in Power Management Controller (PMC) User Interface. However, the Clock Generator registers are named CKGR_.

30.2 Embedded Characteristics

The Clock Generator is comprised of the following:

- A low-power 32.768 kHz crystal oscillator with Bypass mode
- A low-power Slow RC oscillator (32 kHz typical)
- A 3 to 20 MHz Main crystal oscillator with Bypass mode
- A Main RC oscillator. Three output frequencies can be selected: 4/8/12 MHz. By default 12 MHz is selected. 8 MHz and 12 MHz are factory-trimmed.
- A 480 MHz UTMI PLL, providing a clock for the USB high-speed controller
- A 160 to 500 MHz programmable PLL (input from 8 to 32 MHz)

It provides the following clocks:

- SLCK — Slow clock. The only permanent clock within the system
- MAINCK — output of the Main clock oscillator selection: either the Main crystal oscillator or Main RC oscillator
- PLLACK — output of the divider and 160 to 500 MHz programmable PLL (PLLA)
- UPLLCK — output of the 480 MHz UTMI PLL (UPLL)

31.20.7 PMC UTMI Clock Configuration Register

Name: CKGR_UCKR
Offset: 0x001C
Reset: 0x10200800
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access	UPLLCOUNT[3:0]							UPLLEN
Reset	0	0	1	0				0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bits 23:20 – UPLLCOUNT[3:0] UTMI PLL Startup Time
Specifies the number of SLCK cycles multiplied by 8 for the UTMI PLL startup time.

Bit 16 – UPLLEN UTMI PLL Enable
When UPLLEN is set, the LOCKU flag is set once the UTMI PLL startup time is achieved.

Value	Description
0	The UTMI PLL is disabled.
1	The UTMI PLL is enabled.

31.20.9 PMC Clock Generator Main Clock Frequency Register

Name: CKGR_MCFR
Offset: 0x0024
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
								CCSS
Access								
Reset								0

Bit	23	22	21	20	19	18	17	16
				RCMEAS				MAINFRDY
Access								
Reset				0				0

Bit	15	14	13	12	11	10	9	8
	MAINF[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MAINF[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit 24 – CCSS Counter Clock Source Selection

Value	Description
0	The measured clock of the MAINF counter is the Main RC oscillator.
1	The measured clock of the MAINF counter is the Main crystal oscillator.

Bit 20 – RCMEAS RC Oscillator Frequency Measure (write-only)
The measurement is performed on the main frequency (i.e., not limited to the Main RC oscillator only). If the source of MAINCK is the Main crystal oscillator, the restart of measurement may not be required because of the stability of crystal oscillators.

Value	Description
0	No effect.
1	Restarts measuring of the frequency of MAINCK. MAINF carries the new frequency as soon as a low-to-high transition occurs on the MAINFRDY flag.

Bit 16 – MAINFRDY Main Clock Frequency Measure Ready

32.6.1.53 PIO Parallel Capture Interrupt Mask Register

Name: PIO_PCIMR
Offset: 0x015C
Reset: 0x00000000
Property: Read-only

The following configuration values are valid for all listed bit names of this register:

0: Corresponding interrupt is not enabled.

1: Corresponding interrupt is enabled.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
					RXBUFF	ENDRX	OVRE	DRDY
Access								
Reset					0	0	0	0

Bit 3 – RXBUFF Reception Buffer Full Interrupt Mask

Bit 2 – ENDRX End of Reception Transfer Interrupt Mask

Bit 1 – OVRE Parallel Capture Mode Overrun Error Interrupt Mask

Bit 0 – DRDY Parallel Capture Mode Data Ready Interrupt Mask

Bits 9:8 – TCSR[1:0] Temperature Compensated Self-Refresh (only for low-power SDRAM)
TCSR is transmitted to the SDRAM during initialization to set the refresh interval during Self-refresh mode depending on the temperature of the low-power SDRAM. This parameter must be set according to the SDRAM device specification.

After initialization, as soon as the TCSR field is modified and Self-refresh mode is activated, the Extended Mode Register is accessed automatically and TCSR bits are updated before entry in Self-refresh mode. This feature is not supported when SDRAMC shares an external bus with another controller.

Bits 6:4 – PASR[2:0] Partial Array Self-refresh (only for low-power SDRAM)
PASR is transmitted to the SDRAM during initialization to specify whether only one quarter, one half or all banks of the SDRAM array are enabled. Disabled banks are not refreshed in Self-refresh mode. This parameter must be set according to the SDRAM device specification.

After initialization, as soon as the PASR field is modified and Self-refresh mode is activated, the Extended Mode Register is accessed automatically and PASR bits are updated before entry in Self-refresh mode. This feature is not supported when SDRAMC shares an external bus with another controller.

Bits 1:0 – LPCB[1:0] Low-power Configuration Bits

Value	Name	Description
0	DISABLED	The low-power feature is inhibited: no Powerdown, Self-refresh or Deep Powerdown command is issued to the SDRAM device.
1	SELF_REFRESH	The SDRAMC issues a Self-refresh command to the SDRAM device, the SDCK clock is deactivated and the SDCKE signal is set low. The SDRAM device leaves the Self-refresh mode when accessed and enters it after the access.
2	POWER_DOWN	The SDRAMC issues a Powerdown Command to the SDRAM device after each access, the SDCKE signal is set to low. The SDRAM device leaves the Powerdown mode when accessed and enters it after the access.
3	DEEP_POWER_DOWN	The SDRAMC issues a Deep Powerdown command to the SDRAM device. This mode is unique to low-power SDRAM.

2. Allocate an area 8N bytes for the transmit buffer descriptor list in system memory and create N entries in this list. Mark all entries in this list as owned by GMAC, i.e., bit 31 of word 1 set to 0.
3. Mark the last descriptor in the queue with the wrap bit (bit 30 in word 1 set to 1).
4. Write address of transmit buffer descriptor list and control information to GMAC register transmit buffer queue pointer.
5. The transmit circuits can then be enabled by writing to the Network Control register.

Note: The queue pointers must be initialized and point to USED descriptors for all queues including those not intended for use.

38.7.1.4 Address Matching

The GMAC Hash register pair and the four Specific Address register pairs must be written with the required values. Each register pair comprises of a bottom register and top register, with the bottom register being written first. The address matching is disabled for a particular register pair after the bottom register has been written and re-enabled when the top register is written. Each register pair may be written at any time, regardless of whether the receive circuits are enabled or disabled.

As an example, to set Specific Address register 1 to recognize destination address 21:43:65:87:A9:CB, the following values are written to Specific Address register 1 bottom and Specific Address register 1 top:

- Specific Address register 1 bottom bits 31:0 (0x98): 0x8765_4321.
- Specific Address register 1 top bits 31:0 (0x9C): 0x0000_CBA9.
  Note: The address matching is the first level of filtering. If there is a match, the screeners are the next level of filtering for routing the data to the appropriate queue. See Priority Queueing in the DMA for more details.

38.7.1.5 PHY Maintenance

The PHY Maintenance register is implemented as a shift register. Writing to the register starts a shift operation which is signalled as complete when bit two is set in the Network Status register (about 2000 MCK cycles later when bits 18:16 are set to 010 in the Network Configuration register). An interrupt is generated as this bit is set.

During this time, the MSB of the register is output on the MDIO pin and the LSB updated from the MDIO pin with each Management Data Clock (MDC) cycle. This causes the transmission of a PHY management frame on MDIO. See section 22.2.4.5 of the IEEE 802.3 standard.

Reading during the shift operation will return the current contents of the shift register. At the end of the management operation the bits will have shifted back to their original locations. For a read operation the data bits are updated with data read from the PHY. It is important to write the correct values to the register to ensure a valid PHY management frame is produced.

The Management Data Clock (MDC) should not toggle faster than 2.5 MHz (minimum period of 400 ns), as defined by the IEEE 802.3 standard. MDC is generated by dividing down MCK. Three bits in the Network Configuration register determine by how much MCK should be divided to produce MDC.

38.7.1.6 Interrupts

There are 18 interrupt conditions that are detected within the GMAC. The conditions are ORed to make multiple interrupts. Depending on the overall system design this may be passed through a further level of interrupt collection (interrupt controller). On receipt of the interrupt signal, the CPU enters the interrupt handler. Refer to the device interrupt controller documentation to identify that it is the GMAC that is generating the interrupt. To ascertain which interrupt, read the Interrupt Status register. Note that in the default configuration this register will clear itself after being read, though this may be configured to be write-one-to-clear if desired.

Offset	Name	Bit Pos.								
0x04BC	GMAC_CBSCR	7:0							QAE	QBE
		15:8								
		23:16								
		31:24								
0x04C0	GMAC_CBSISQA	7:0	IS[7:0]							
		15:8	IS[15:8]							
		23:16	IS[23:16]							
		31:24	IS[31:24]							
0x04C4	GMAC_CBSISQB	7:0	IS[7:0]							
		15:8	IS[15:8]							
		23:16	IS[23:16]							
		31:24	IS[31:24]							
0x04C8 ... 0x04FF	Reserved									
0x0500	GMAC_ST1RPQ0	7:0	DSTCM[3:0]					QNB[2:0]		
		15:8	UDPM[3:0]				DSTCM[7:4]			
		23:16	UDPM[11:4]							
		31:24			UDPE	DSTCE	UDPM[15:12]			
0x0504	GMAC_ST1RPQ1	7:0	DSTCM[3:0]					QNB[2:0]		
		15:8	UDPM[3:0]				DSTCM[7:4]			
		23:16	UDPM[11:4]							
		31:24			UDPE	DSTCE	UDPM[15:12]			
0x0508	GMAC_ST1RPQ2	7:0	DSTCM[3:0]					QNB[2:0]		
		15:8	UDPM[3:0]				DSTCM[7:4]			
		23:16	UDPM[11:4]							
		31:24			UDPE	DSTCE	UDPM[15:12]			
0x050C	GMAC_ST1RPQ3	7:0	DSTCM[3:0]					QNB[2:0]		
		15:8	UDPM[3:0]				DSTCM[7:4]			
		23:16	UDPM[11:4]							
		31:24			UDPE	DSTCE	UDPM[15:12]			
0x0510 ... 0x053F	Reserved									
0x0540	GMAC_ST2RPQ0	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x0544	GMAC_ST2RPQ1	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x0548	GMAC_ST2RPQ2	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE

38.8.57 GMAC Carrier Sense Errors Register

Name: GMAC_CSE
Offset: 0x14C
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							CSR[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	CSR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – CSR[9:0] Carrier Sense Error
This register counts the number of frames transmitted with carrier sense was not seen during transmission or where carrier sense was de-asserted after being asserted in a transmit frame without collision (no underrun). Only incremented in half duplex mode. The only effect of a carrier sense error is to increment this register. The behavior of the other statistics registers is unaffected by the detection of a carrier sense error.

38.8.74 GMAC Frame Check Sequence Errors Register

Name: GMAC_FCSE
Offset: 0x190
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							FCKR[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	FCKR[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – FCKR[9:0] Frame Check Sequence Errors
The register counts frames that are an integral number of bytes, have bad CRC and are between 64 and 1518 bytes in length (1536 Bytes if GMAC_NCFGR.MAXFS is written to '1'). This register is also incremented if a symbol error is detected and the frame is of valid length and has an integral number of bytes.
This register is incremented for a frame with bad FCS, regardless of whether it is copied to memory due to ignore FCS mode (enabled by writing GMAC_NCFGR.IRXFCS=1).

Offset	Name	Bit Pos.								
		31:24								
0x0564	USBHS_HSTPIPICR1 (INTPIPES)	7:0	SHORTPACKETIC	RXSTALLDIC	OVERFIC	NAKEDIC		UNDERFIC	TXOUTIC	RXINIC
		15:8								
		23:16								
		31:24								
0x0564	USBHS_HSTPIPICR1 (ISOPIPES)	7:0	SHORTPACKETIC	CRCERRIC	OVERFIC	NAKEDIC		UNDERFIC	TXOUTIC	RXINIC
		15:8								
		23:16								
		31:24								
0x0568	USBHS_HSTPIPICR2	7:0	SHORTPACKETIC	RXSTALLDIC	OVERFIC	NAKEDIC		TXSTPIC	TXOUTIC	RXINIC
		15:8								
		23:16								
		31:24								
0x0568	USBHS_HSTPIPICR2 (INTPIPES)	7:0	SHORTPACKETIC	RXSTALLDIC	OVERFIC	NAKEDIC		UNDERFIC	TXOUTIC	RXINIC
		15:8								
		23:16								
		31:24								
0x0568	USBHS_HSTPIPICR2 (ISOPIPES)	7:0	SHORTPACKETIC	CRCERRIC	OVERFIC	NAKEDIC		UNDERFIC	TXOUTIC	RXINIC
		15:8								
		23:16								
		31:24								
0x056C	USBHS_HSTPIPICR3	7:0	SHORTPACKETIC	RXSTALLDIC	OVERFIC	NAKEDIC		TXSTPIC	TXOUTIC	RXINIC
		15:8								
		23:16								
		31:24								
0x056C	USBHS_HSTPIPICR3 (INTPIPES)	7:0	SHORTPACKETIC	RXSTALLDIC	OVERFIC	NAKEDIC		UNDERFIC	TXOUTIC	RXINIC
		15:8								
		23:16								
		31:24								
0x056C	USBHS_HSTPIPICR3 (ISOPIPES)	7:0	SHORTPACKETIC	CRCERRIC	OVERFIC	NAKEDIC		UNDERFIC	TXOUTIC	RXINIC
		15:8								
		23:16								
		31:24								
0x0570	USBHS_HSTPIPICR4	7:0	SHORTPACKETIC	RXSTALLDIC	OVERFIC	NAKEDIC		TXSTPIC	TXOUTIC	RXINIC
		15:8								
		23:16								
		31:24								

Value	Description
	• (INRQ+1) in requests have been processed. • A Pipe Reset (USBHS_HSTPIP.PRSTx rising) has occurred. • A Pipe Enable (USBHS_HSTPIP.PEN rising) has occurred.

Bit 16 – PDISHDMA Pipe Interrupts Disable HDMA Request Enable
See the USBHS_DEVEPTIMR.EPDISHDMA bit description.

Bit 14 – FIFOCON FIFO Control
For OUT and SETUP pipes:

0: Cleared when USBHS_HSTPIPIDR.FIFOCONC = 1. This sends the FIFO data and switches the bank.

1: Set when the current bank is free, at the same time as USBHS_HSTPIPISR.TXOUTI or TXSTPI.

For IN pipes:

0: Cleared when USBHS_HSTPIPIDR.FIFOCONC = 1. This frees the current bank and switches to the next bank.

1: Set when a new IN message is stored in the current bank, at the same time as USBHS_HSTPIPISR.RXINI.

Bit 12 – NBUSYBKE Number of Busy Banks Interrupt Enable

Value	Description
0	Cleared when USBHS_HSTPIPIDR.NBUSYBKEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.NBUSYBKE).
1	Set when USBHS_HSTPIPIER.NBUSYBKES = 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.NBUSYBKE).

Bit 7 – SHORTPACKETIE Short Packet Interrupt Enable
If this bit is set for non-control OUT pipes, a short packet transmission is guaranteed upon ending a DMA transfer, thus signaling an end of transfer, provided that the End of DMA Buffer Output Enable (USBHS_HSTDMACONTROL.END_B_EN) bit and the Automatic Switch (USBHS_HSTPIPCFG.AUTOSW) bit = 1.

Value	Description
0	Cleared when USBHS_HSTPIPIDR.SHORTPACKETEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.SHORTPACKETE).
1	Set when USBHS_HSTPIPIER.SHORTPACKETIES = 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.SHORTPACKETIE).

Bit 6 – RXSTALLDE Received STALLed Interrupt Enable

Value	Description
0	Cleared when USBHS_HSTPIPIDR.RXSTALLDEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.RXSTALLDE).
1	Set when USBHS_HSTPIPIER.RXSTALLDES= 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.RXSTALLDE).

Bit 5 – OVERFIE Overflow Interrupt Enable

40.14.1 HSMCI Control Register

Name: HSMCI_CR
Offset: 0x00
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	SWRST				PWSDIS	PWSEN	MCIDIS	MCIEN
Access								
Reset								

Bit 7 – SWRST Software Reset

Value	Description
0	No effect.
1	Resets the HSMCI. A software triggered hardware reset of the HSMCI is performed.

Bit 3 – PWSDIS Power Save Mode Disable

Value	Description
0	No effect.
1	Disables the Power Saving Mode.

Bit 2 – PWSEN Power Save Mode Enable

WARNING Before enabling this mode, the user must set a value different from 0 in the PWSDIV field of the HSMCI_MR.

Value	Description
0	No effect.
1	Enables the Power Saving Mode if PWSDIS is 0.

40.14.2 HSMCI Mode Register

Name: HSMCI_MR
Offset: 0x04
Reset: 0x0
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the HSMCI Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								0

Bit	15	14	13	12	11	10	9	8
Access								
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
Access								
Reset	0	0	0	0	0	0	0	0

Bit 16 – CLKODD Clock divider is odd
This bit is the least significant bit of the clock divider and indicates the clock divider parity.

Bit 14 – PADV Padding Value
PADV may be only in manual transfer.

Value	Description
0	0x00 value is used when padding data in write transfer.
1	0xFF value is used when padding data in write transfer.

Bit 13 – FBYTE Force Byte Transfer
Enabling Force Byte Transfer allow byte transfers, so that transfer of blocks with a size different from modulo 4 can be supported.

WARNING BLKLEN value depends on FBYTE.

0	Baud Rate Clock Disabled			
1 to 65535	CD = Selected Clock / (16 × Baud Rate)	CD = Selected Clock / (8 × Baud Rate)	CD = Selected Clock / Baud Rate	CD = Selected Clock / (FI_DI_RATIO × Baud Rate)

49.6.24 MCAN High Priority Message Status

Name: MCAN_HPMS
Offset: 0x94
Reset: 0x00000000
Property: Read-only

This register is updated every time a Message ID filter element configured to generate a priority event matches. This can be used to monitor the status of incoming high priority messages and to enable fast access to these messages.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	FLST	FIDX[6:0]						
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MSI[1:0]		BIDX[5:0]					
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 15 – FLST Filter List
Indicates the filter list of the matching filter element.

Value	Description
0	Standard filter list
1	Extended filter list

Bits 14:8 – FIDX[6:0] Filter Index
Index of matching filter element. Range is 0 to MCAN_SIDFC.LSS - 1 resp. MCAN_XIDFC.LSE - 1.

Bits 7:6 – MSI[1:0] Message Storage Indicator

Value	Name	Description
0	NO_FIFO_SEL	No FIFO selected.
1	LOST	FIFO message lost.
2	FIFO_0	Message stored in FIFO 0.
3	FIFO_1	Message stored in FIFO 1.

55.5.2.3 ICM Region Control Structure Member

Name: ICM_RCTRL
Property: Read/Write

Register offset is calculated as ICM_DSCR+0x008+RID*(0x10).

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	TRSIZE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bit	7	6	5	4	3	2	1	0
	TRSIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset								

Bits 15:0 – TRSIZE[15:0] Transfer Size for the Current Chunk of Data
ICM performs a transfer of (TRSIZE + 1) blocks of 512 bits.

56.6.6 TRNG Output Data Register

Name: TRNG_ODATA
Offset: 0x50
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	ODATA[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ODATA[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ODATA[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ODATA[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – ODATA[31:0] Output Data
The 32-bit Output Data register contains the 32-bit random data.