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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70q21a-an

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31.20.10 PMC Clock Generator PLLA Register

Name: CKGR_PLLAR
Offset: 0x0028
Reset: 0x00003F00
Property: Read/Write

Possible limitations on PLLA input frequencies and multiplier factors should be checked before using the PMC.

WARNING Bit 29 must always be set to ‘1’ when programming the CKGR_PLLAR.

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
			ONE			MULA[10:8]		
Access								
Reset			0			0	0	0

Bit	23	22	21	20	19	18	17	16
	MULA[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
			PLLACOUNT[5:0]					
Access								
Reset			1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	DIVA[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit 29 – ONE Must Be Set to 1
Bit 29 must always be set to ‘1’ when programming the CKGR_PLLAR.

Bits 26:16 – MULA[10:0] PLLA Multiplier
1 up to 62 = PLLCK frequency is the PLLA input frequency multiplied by MULA + 1.

Unlisted values are forbidden.

Value	Description
0	The PLLA is disabled (PLLA also disabled if DIVA = 0).

Bits 13:8 – PLLACOUNT[5:0] PLLA Counter
Specifies the number of SLCK cycles before the LOCKA bit is set in PMC_SR after CKGR_PLLAR is written.

32.6.1.7 PIO Input Filter Enable Register

Name: PIO_IFER
Offset: 0x0020
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Input Filter Enable

Value	Description
0	No effect.
1	Enables the input glitch filter on the I/O line.

32.6.1.19 PIO Multi-driver Disable Register

Name: PIO_MDDR
Offset: 0x0054
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Multi-drive Disable

Value	Description
0	No effect.
1	Disables multi-drive on the I/O line.

37.6.9 ISI Color Space Conversion RGB to YCrCb Set 2 Register

Name: ISI_R2Y_SET2
Offset: 0x20
Reset: 0x01384A4B
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
								Boff
Access								R/W
Reset								1

Bit	23	22	21	20	19	18	17	16
		C8[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	1	1	1	0	0	0

Bit	15	14	13	12	11	10	9	8
		C7[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	0	0	1	0	1	0

Bit	7	6	5	4	3	2	1	0
		C6[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		1	0	0	1	0	1	1

Bit 24 – Boff Color Space Conversion Blue Component Offset

Value	Description
0	No offset.
1	Offset = 128.

Bits 22:16 – C8[6:0] Color Space Conversion Matrix Coefficient C8
C8 element default step is 1/128, ranges from 0 to 0.9921875.

Bits 14:8 – C7[6:0] Color Space Conversion Matrix Coefficient C7
C7 element default step is 1/256, ranges from 0 to 0.49609375.

Bits 6:0 – C6[6:0] Color Space Conversion Matrix Coefficient C6
C6 element default step is 1/512, ranges from 0 to 0.2480468875.

The highest priority queue always has priority regardless of which queue has the most credit.

38.6.20 LPI Operation in the EMAC

It is best to use firmware to control LPI. LPI operation happens at the system level. Firmware gives maximum control and flexibility of operation. LPI operation is straightforward and firmware should be capable of responding within the required timeframes.

Autonegotiation:

1. Indicate EEE capability using next page autonegotiation.

For the transmit path:

1. If the link has been up for 1 second and there is nothing being transmitted, write to the TXLPIEN bit in the Network Control register.
2. Wake up by clearing the TXLPIEN bit in the Network Control register.

For the receive path:

1. Enable RXLPISBC bit in GMAC_IER. The bit RXLPIS is set in Network Status Register triggering an interrupt.
2. Wait for an interrupt to indicate that LPI has been received.
3. Disable relevant parts of the receive path if desired.
4. The RXLPIS bit in Network Status Register gets cleared to indicate that regular idle has been received. This triggers an interrupt.
5. Re-enable the receive path.

38.6.21 PHY Interface

Different PHY interfaces are supported by the Ethernet MAC:

- MII
- RMII

The MII interface is provided for 10/100 operation and uses txd[3:0] and rxd[3:0]. The RMII interface is provided for 10/100 operation and uses txd[1:0] and rxd[1:0].

38.6.22 10/100 Operation

The 10/100 Mbps speed bit in the Network Configuration register is used to select between 10 Mbps and 100 Mbps.

38.6.23 Jumbo Frames

The jumbo frames enable bit in the Network Configuration register allows the GMAC, in its default configuration, to receive jumbo frames up to 10240 bytes in size. This operation does not form part of the IEEE 802.3 specification and is normally disabled. When jumbo frames are enabled, frames received with a frame size greater than 10240 bytes are discarded.

38.7 Programming Interface

38.7.1 Initialization

38.7.1.1 Configuration

Initialization of the GMAC configuration (e.g., loop back mode, frequency ratios) must be done while the transmit and receive circuits are disabled. See the description of the Network Control register and Network Configuration register earlier in this document.

38.8.10 GMAC Interrupt Status Register

Name: GMAC_ISR
Offset: 0x024
Reset: 0x00000000
Property: Read-only

This register indicates the source of the interrupt. An interrupt source must be enabled in the mask register first so the corresponding bits of this register will be set and the GMAC interrupt signal will be asserted in the system.

Bit	31	30	29	28	27	26	25	24
			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
Access	R	R	R	R	R	R		
Reset	0	0	0	0	0	0		

Bit	15	14	13	12	11	10	9	8
		PFTR	PTZ	PFNZ	HRESP	ROVR		
Access		R	R	R	R	R		
Reset		0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 29 – TSUTIMCMP TSU Timer Comparison
Indicates when TSU timer count value is equal to programmed value.

Cleared on read.

Bit 28 – WOL Wake On LAN
WOL interrupt. Indicates a WOL message has been received.

Bit 27 – RXLPISBC Receive LPI indication Status Bit Change
Receive LPI indication status bit change.

Cleared on read.

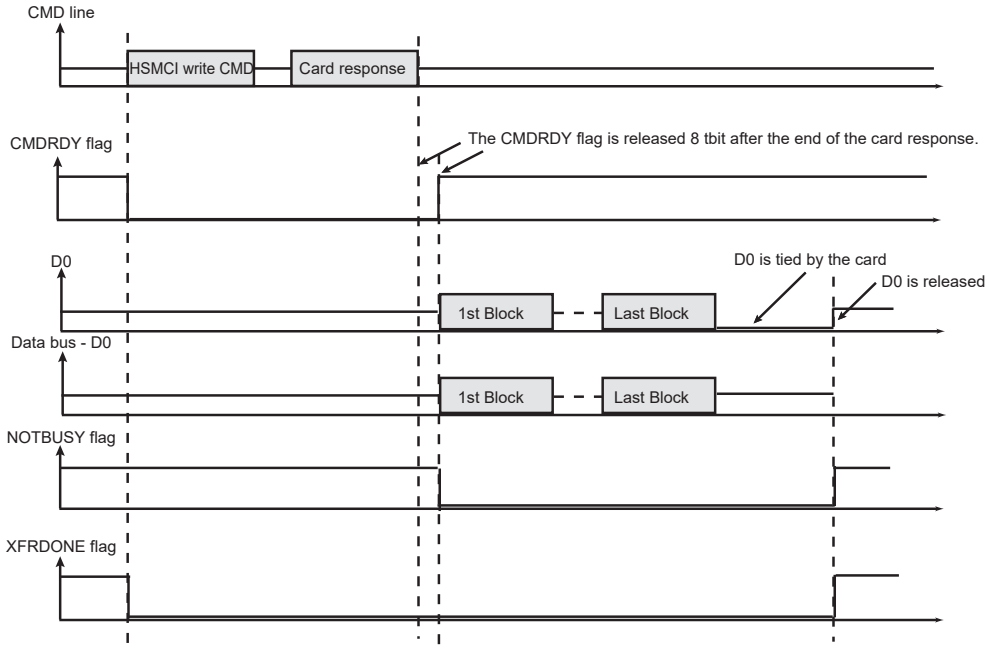
Bit 26 – SRI TSU Seconds Register Increment
Indicates the register has incremented.

Cleared on read.

Bit 25 – PDRSFT PDelay Response Frame Transmitted
Indicates a PTP pdelay_resp frame has been transmitted.

Offset	Name	Bit Pos.								
0x0308	USBHS_DEVDMACONTROL1	7:0	BURST_LCK	DESC_LD_IT	END_BUFFIT	END_TR_IT	END_B_EN	END_TR_EN	LDNXT_DSC	CHANN_ENB
		15:8								
		23:16	BUFF_LENGTH[7:0]							
		31:24	BUFF_LENGTH[15:8]							
0x030C	USBHS_DEVDMASTATUS1	7:0		DESC_LDST	END_BF_ST	END_TR_ST			CHANN_ACT	CHANN_ENB
		15:8								
		23:16	BUFF_COUNT[7:0]							
		31:24	BUFF_COUNT[15:8]							
0x0310	USBHS_DEVDMANXTDSC2	7:0	NXT_DSC_ADD[7:0]							
		15:8	NXT_DSC_ADD[15:8]							
		23:16	NXT_DSC_ADD[23:16]							
		31:24	NXT_DSC_ADD[31:24]							
0x0314	USBHS_DEVDMAADDRESS2	7:0	BUFF_ADD[7:0]							
		15:8	BUFF_ADD[15:8]							
		23:16	BUFF_ADD[23:16]							
		31:24	BUFF_ADD[31:24]							
0x0318	USBHS_DEVDMACONTROL2	7:0	BURST_LCK	DESC_LD_IT	END_BUFFIT	END_TR_IT	END_B_EN	END_TR_EN	LDNXT_DSC	CHANN_ENB
		15:8								
		23:16	BUFF_LENGTH[7:0]							
		31:24	BUFF_LENGTH[15:8]							
0x031C	USBHS_DEVDMASTATUS2	7:0		DESC_LDST	END_BF_ST	END_TR_ST			CHANN_ACT	CHANN_ENB
		15:8								
		23:16	BUFF_COUNT[7:0]							
		31:24	BUFF_COUNT[15:8]							
0x0320	USBHS_DEVDMANXTDSC3	7:0	NXT_DSC_ADD[7:0]							
		15:8	NXT_DSC_ADD[15:8]							
		23:16	NXT_DSC_ADD[23:16]							
		31:24	NXT_DSC_ADD[31:24]							
0x0324	USBHS_DEVDMAADDRESS3	7:0	BUFF_ADD[7:0]							
		15:8	BUFF_ADD[15:8]							
		23:16	BUFF_ADD[23:16]							
		31:24	BUFF_ADD[31:24]							
0x0328	USBHS_DEVDMACONTROL3	7:0	BURST_LCK	DESC_LD_IT	END_BUFFIT	END_TR_IT	END_B_EN	END_TR_EN	LDNXT_DSC	CHANN_ENB
		15:8								
		23:16	BUFF_LENGTH[7:0]							
		31:24	BUFF_LENGTH[15:8]							
0x032C	USBHS_DEVDMASTATUS3	7:0		DESC_LDST	END_BF_ST	END_TR_ST			CHANN_ACT	CHANN_ENB
		15:8								
		23:16	BUFF_COUNT[7:0]							
		31:24	BUFF_COUNT[15:8]							
0x0330	USBHS_DEVDMANXTDSC4	7:0	NXT_DSC_ADD[7:0]							
		15:8	NXT_DSC_ADD[15:8]							
		23:16	NXT_DSC_ADD[23:16]							
		31:24	NXT_DSC_ADD[31:24]							
0x0334	USBHS_DEVDMAADDRESS4	7:0	BUFF_ADD[7:0]							
		15:8	BUFF_ADD[15:8]							

Figure 40-12. XFRDONE During a Write Access



40.13 Register Write Protection

To prevent any single software error from corrupting HSMCI behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the HSMCI Write Protection Mode Register (HSMCI_WPMR).

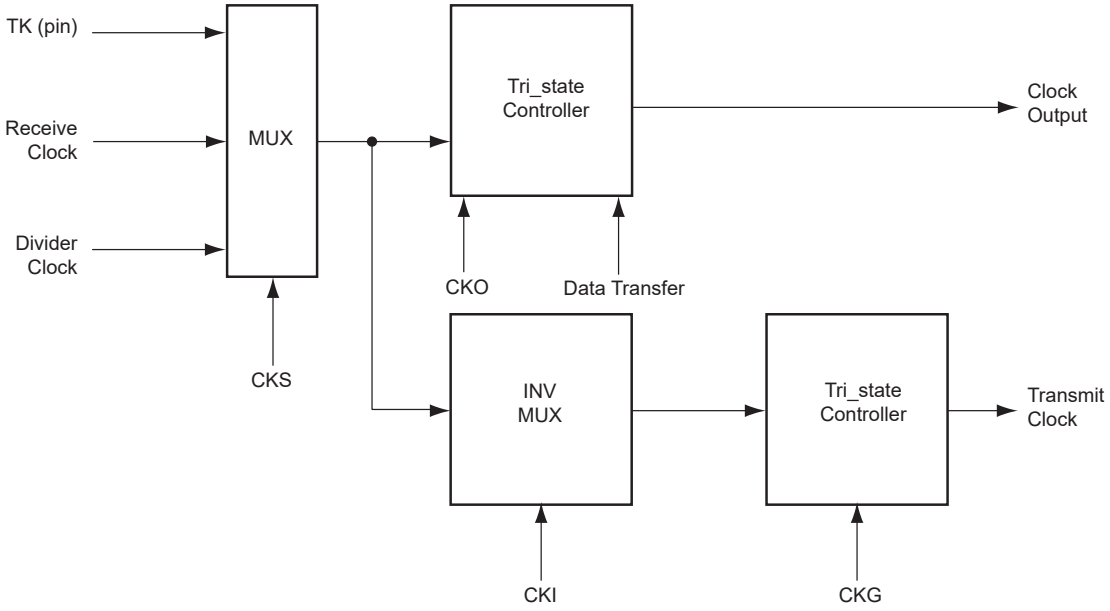
If a write access to a write-protected register is detected, the WPVS bit in the HSMCI Write Protection Status Register (HSMCI_WPSR) is set and the field WPVSRC indicates the register in which the write access has been attempted.

The WPVS bit is automatically cleared after reading the HSMCI_WPSR.

The following registers can be protected:

- HSMCI Mode Register
- HSMCI Data Timeout Register
- HSMCI SDCard/SDIO Register
- HSMCI Completion Signal Timeout Register
- HSMCI DMA Configuration Register
- HSMCI Configuration Register

Figure 44-9. Transmit Clock Management

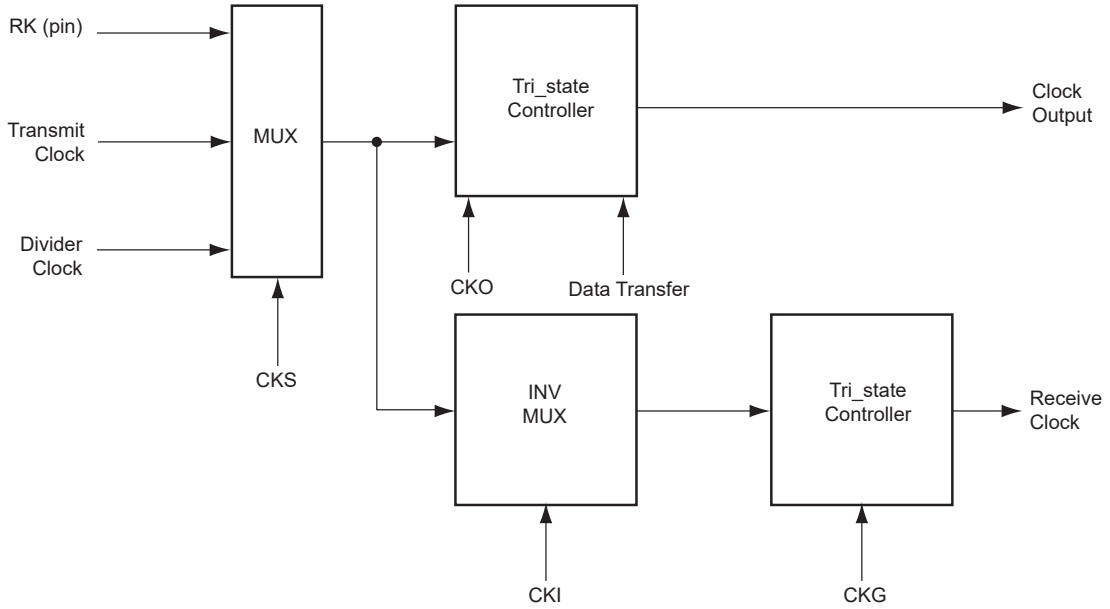


44.8.1.3 Receive Clock Management

The receive clock is generated from the transmit clock or the divider clock or an external clock scanned on the RK I/O pad. The Receive Clock is selected by the CKS field in SSC_RCMR (Receive Clock Mode Register). Receive Clocks can be inverted independently by the CKI bits in SSC_RCMR.

The receiver can also drive the RK I/O pad continuously or be limited to the current data transfer. The clock output is configured by the SSC_RCMR. The Receive Clock Inversion (CKI) bits have no effect on the clock outputs. Programming the SSC_RCMR to select RK pin (CKS field) and at the same time Continuous Receive Clock (CKO field) can lead to unpredictable results.

Figure 44-10. Receive Clock Management



44.9.16 SSC Interrupt Mask Register

Name: SSC_IMR
Offset: 0x4C
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					RXSYN	TXSYN	CP1	CP0
Access					R	R	R	R
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
			OVRUN	RXRDY			TXEMPTY	TXRDY
Access			R	R			R	R
Reset			0	0			0	0

Bit 11 – RXSYN Rx Sync Interrupt Mask

Value	Description
0	The Rx Sync Interrupt is disabled.
1	The Rx Sync Interrupt is enabled.

Bit 10 – TXSYN Tx Sync Interrupt Mask

Value	Description
0	The Tx Sync Interrupt is disabled.
1	The Tx Sync Interrupt is enabled.

Bit 9 – CP1 Compare 1 Interrupt Mask

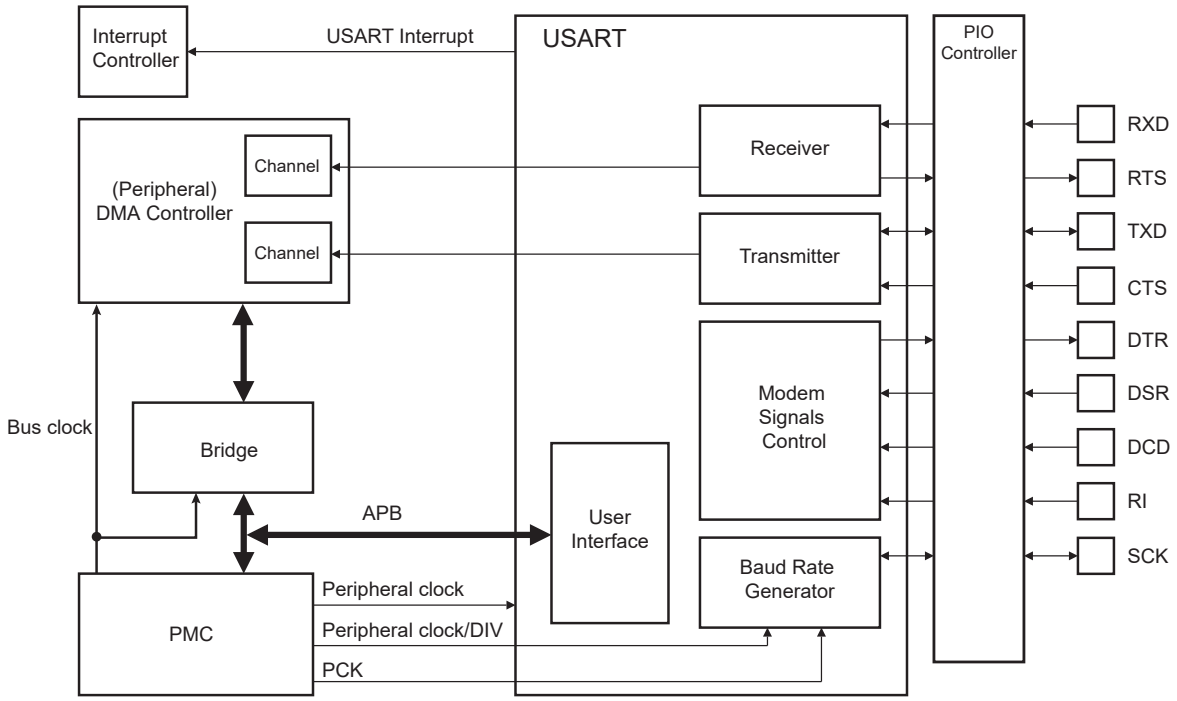
Value	Description
0	The Compare 1 Interrupt is disabled.
1	The Compare 1 Interrupt is enabled.

Bit 8 – CP0 Compare 0 Interrupt Mask

Value	Description
0	The Compare 0 Interrupt is disabled.
1	The Compare 0 Interrupt is enabled.

46.3 Block Diagram

Figure 46-1. USART Block Diagram



46.4 I/O Lines Description

Table 46-1. I/O Line Description

Name	Description	Type	Active Level
SCK	Serial Clock	I/O	—
TXD	Transmit Serial Data or Master Out Slave In (MOSI) in SPI Master mode or Master In Slave Out (MISO) in SPI Slave mode	I/O	—
RXD	Receive Serial Data or Master In Slave Out (MISO) in SPI Master mode or Master Out Slave In (MOSI) in SPI Slave mode	Input	—
RI	Ring Indicator	Input	Low
DSR	Data Set Ready	Input	Low
DCD	Data Carrier Detect	Input	Low
DTR	Data Terminal Ready	Output	Low
LCOL	LON Collision Detection	Input	Low
CTS	Clear to Send	Input	Low

46.7.28 USART FI DI RATIO Register (LON_MODE)

Name: US_FIDI (LON_MODE)
Offset: 0x0040
Reset: 0x174
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	BETA2[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	BETA2[15:8]							
Access								
Reset	0	0	0	0	0	0	0	1

Bit	7	6	5	4	3	2	1	0
	BETA2[7:0]							
Access								
Reset	0	1	1	1	0	1	0	0

Bits 23:0 – BETA2[23:0] LON BETA2 Length

Value	Description
1-16777215	LON BETA2 length in t_{bit}.

47.6.9 UART Baud Rate Generator Register

Name: UART_BRGR
Offset: 0x20
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	CD[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CD[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CD[15:0] Clock Divisor

Value	Description
0	Baud rate clock is disabled
1 to 65,535	If BRSRCCK = 0: $CD = \frac{f_{peripheral\ clock}}{16 \times Baud\ Rate}$ If BRSRCCK = 1: $CD = \frac{f_{PCKx}}{16 \times Baud\ Rate}$

buffer is read from system memory. Software should set the buffer depth to contain the exact number of complete packets for that buffer. Segmented buffers are not supported for Tx packet channels in multiple-packet mode.

For Rx packet channels in multiple-packet mode, PSn has no meaning and should be ignored. Software is responsible for keeping track of where each packet starts and ends within the multiple-packet buffer via the packet PML. The buffer done bit (DNEn) is set in hardware for Rx channels when a buffer is full (see Buffer 1 in Figure 48-23) or if a packet ends exactly 1-byte before the end of the buffer (see Buffer 2 in Figure 48-23). Multiple-packet mode also supports segmented Rx packets spanning two or more buffers (see Buffers 3–6 in Figure 48-23).

Table 48-24 shows the format for multiple-packet mode asynchronous and control ADT entries. The field definitions are defined in Table 48-20.

Figure 48-23. Multiple-packet Asynchronous or Control System Memory Structure

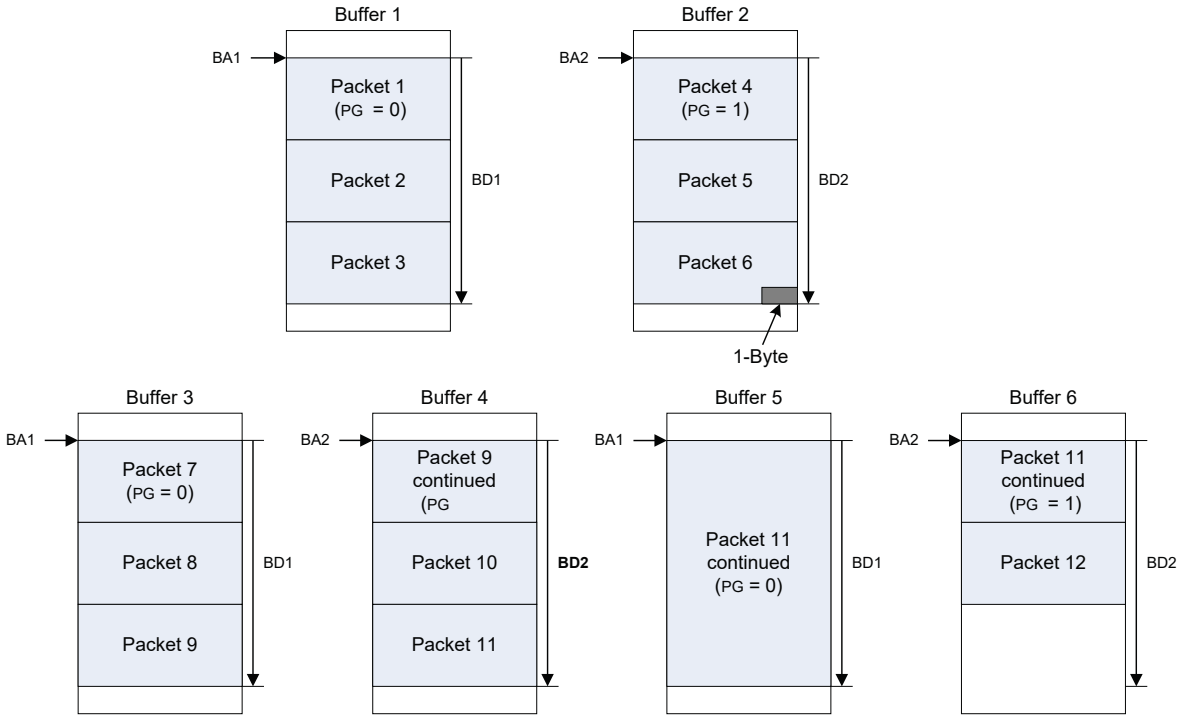


Table 48-24. Multiple-packet Asynchronous and Control Entry Format

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CE	LE	PG	Reserved												
16	Reserved															
32	RDY1	DNE1	ERR1	PS1(1)	BD1[11:0]											
48	RDY2	DNE2	ERR2	PS2(1)	BD2[11:0]											
64	BA1[15:0]															
80	BA1[31:16]															
96	BA2[15:0]															
112	BA2[31:16]															

55.6.3 ICM Status Register

Name: ICM_SR
Offset: 0x08
Reset: –
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RMDIS[3:0]				RAWRMDIS[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	–	0	0	0	–

Bit	7	6	5	4	3	2	1	0
								ENABLE
Access								R
Reset								–

Bits 15:12 – RMDIS[3:0] Region Monitoring Disabled Status

Value	Description
0	Region i is being monitored (occurs after integrity check value has been calculated and written to Hash area).
1	Region i monitoring is not being monitored.

Bits 11:8 – RAWRMDIS[3:0] Region Monitoring Disabled Raw Status

Value	Description
0	Region i monitoring has been activated by writing a 1 in RMEN[i] of ICM_CTRL.
1	Region i monitoring has been deactivated by writing a 1 in RMDIS[i] of ICM_CTRL.

Bit 0 – ENABLE ICM Enable Register

Value	Description
0	ICM is disabled.
1	ICM is activated.

Figure 58-2. VDDCORE Power-On Reset Characteristics

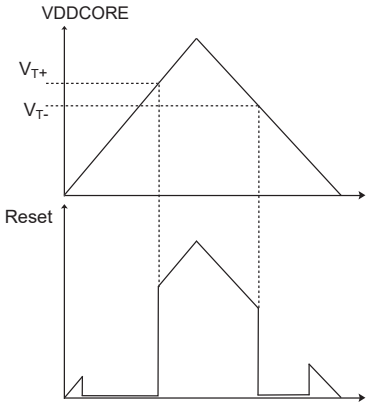


Table 58-8. VDDIO Supply Monitor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_T	Supply Monitor Threshold	16 selectable steps (see the Threshold Selection table below)	–	–	–	V
T_{ACC}	Threshold Accuracy	–	-4	–	4	%
V_{hys}	Hysteresis Voltage	–	–	38	45	mV
t_{START}	Startup Time	From disabled state to enabled state	–	–	300	µs

Table 58-9. Threshold Selection

Symbol	Parameter	Digital Code	Min	Typ	Max	Unit
V_T	Supply Monitor Threshold	0	–	1.6	–	V
		1	–	1.72	–	
		10	–	1.84	–	
		11	–	1.96	–	
		100	–	2.08	–	
		101	–	2.2	–	
		110	–	2.32	–	
		111	–	2.44	–	
		1000	–	2.56	–	
		1001	–	2.68	–	
		1010	–	2.8	–	
		1011	–	2.92	–	
		1100	–	3.04	–	
		1101	–	3.16	–	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Gain = 2		±2.1		
		Gain = 4		±2.5		
DNL	Differential Non-Linearity	–	-6	±2	6	LSB
Single-Ended Mode						
INL	Integral Non-Linearity	Gain = 1	-12	±2	12	LSB
		Gain = 2		±2.6		
		Gain = 4		±2.7		
DNL	Differential Non-Linearity	–	-6	±2	6	LSB

Note: INL/DNL given inside the linear range of the AFE: 2% to 98% of VREFP.

Table 59-36. AFE Offset and Gain Error, V_{VREFP} = 1.7V to 3.3V

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
Differential Mode						
E_O	Differential Offset Error (see **Note 1**)	Gain=1	-20	–	35	LSB
E_G	Differential Gain Error	Gain=1	-0.3	0	0.7	%
		Gain=2	-0.3	0.3	1.4	
		Gain=4	-0.3	0.7	3.3	
Single-Ended Mode						
E_O	Single-ended Offset Error (see **Note 1**)	Gain=1	-20	–	35	LSB
E_G	Single-ended Gain Error	Gain=1	0.3	0.7	1.8	%
		Gain=2	0.3	1.3	3.6	
		Gain=4	0.3	1.7	4.7	

59.8.6 AFE Channel Input Impedance

Figure 59-15. Input Channel Model

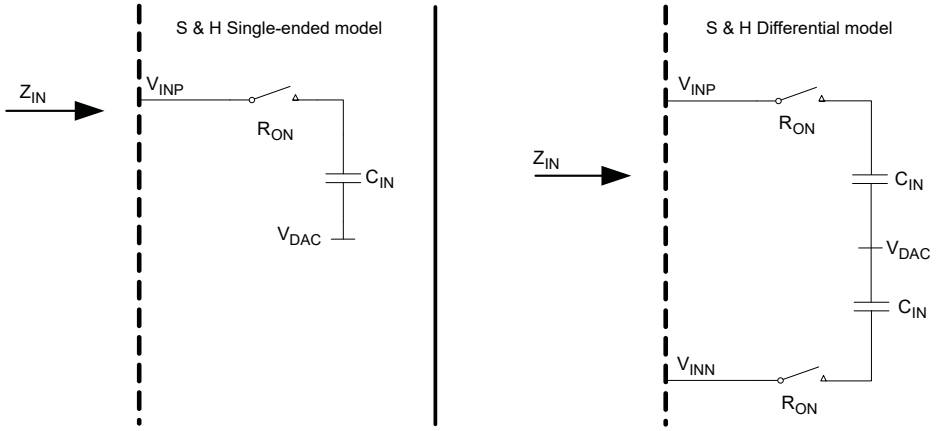
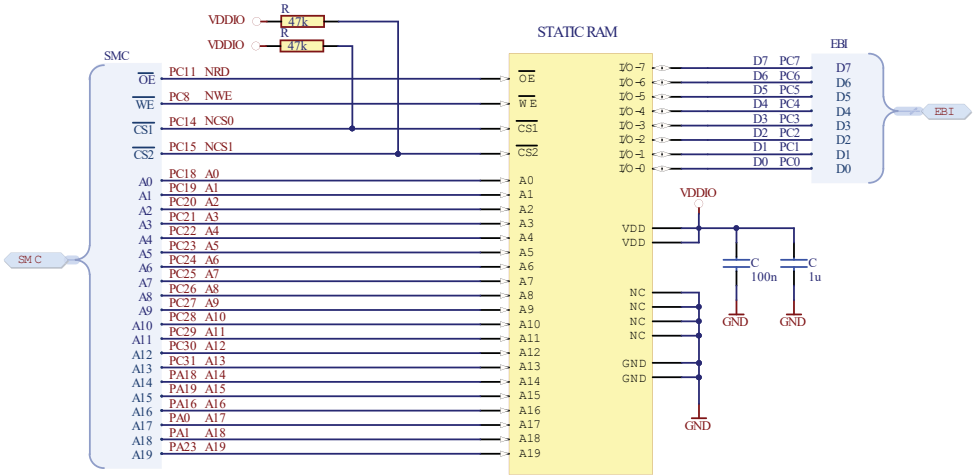
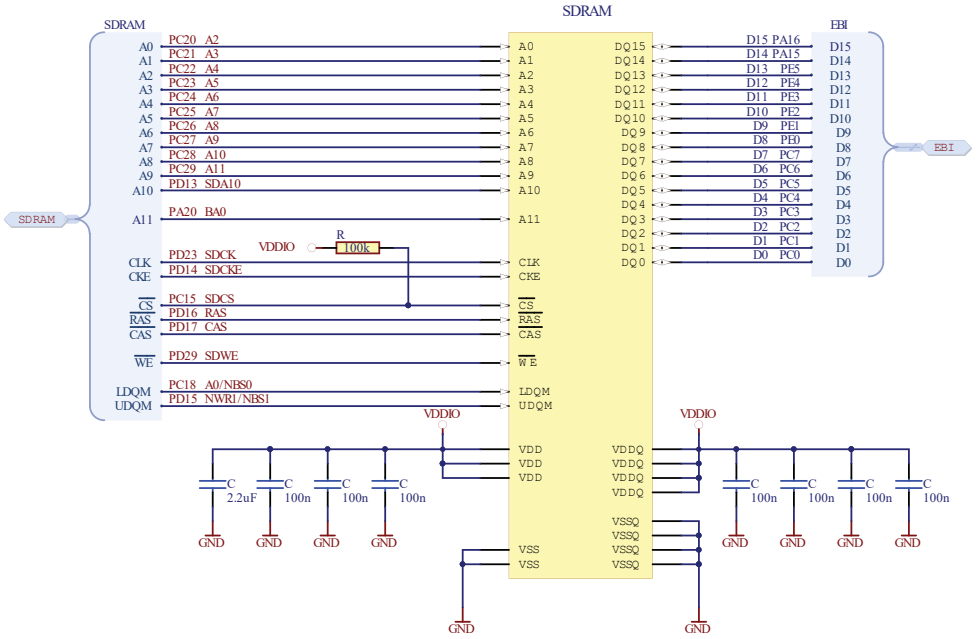


Figure 60-3. Schematic Example with a 8 Mb/8-bit Static RAM



Note: For more details on the pin configuration of the EBI, refer to Table 33-3.

Figure 60-4. Schematic Example with a 16 Mb/16-bit SDRAM



Note:

1. It is required to adjust the drive (LOW/HIGH) and it may be required to add external resistors for impedance adjustment.
2. For more details on the pin configuration of the EBI, refer to Table 33-3.

Date	Comments
01-June-16	Section 42. “Quad SPI Interface (QSPI)” Section 42.2 “Embedded Characteristics”: added bullet on Single Data Rate and Double Data Rate modes. Figure 42-2 “QSPI Transfer Format (QSPI_SCR.CPHA = 0, 8 bits per transfer)” and Figure 42-3 “QSPI Transfer Format (QSPI_SCR.CPHA = 1, 8 bits per transfer)””: modified NSS to QCS. Section 42.7.2 “QSPI Mode Register”: updated CSMODE description. Section 42.7.5 “QSPI Status Register”: updated descriptions of bits CSR and INSTRE.
	Section 43. “Two-wire Interface (TWIHS)” Updated Figure 43-1 “Block Diagram”. Section 43.6.3.9 “SMBus Mode”: deleted bullet on SMBALERT. Section 43.6.5.6 “SMBus Mode”: deleted bullet on SMBALERT. Section 43.7.5 “TWIHS Clock Waveform Generator Register”: Bit 20 now ‘reserved’ (was CKSRC: Transfer Rate Clock Source). HOLD field extended to 6 bits.
	Section 44. “Synchronous Serial Controller (SSC)” in Figure 44-19 “Interrupt Block Diagram”: renamed RXSYNC to RXSYN; renamed TXSYNC to TXSYN.
	Section 45. “Inter-IC Sound Controller (I2SC)” Throughout: In text, tables and figures, pin names changed to: - I2SC_MCK - I2SC_CK - I2SC_WS - I2SC_DI - I2SC_DO Updated Figure 45-1 “I2SC Block Diagram”. Section 45.6.1 “Initialization”: modified register name from CCFG_I2SCLKSEL to CCFG_PCCR. Section 45.6.5 “Serial Clock and Word Select Generation”: updated paragraph on I2SC input clock selection in Master mode. Updated Figure 45-3 “I2SC Clock Generation”. Section 45.8.2 “I2SC Mode Register”: updated MODE bit description for value ‘1’. Updated IMCKDIV and IMCKMODE field descriptions.
	Section 46. “Universal Synchronous Asynchronous Receiver Transceiver (USART)” Section 46.2 “Embedded Characteristics”: added bullet “Optimal for Node-to-Node Communication (no embedded digital line filter)” to LON Mode features.