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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70q21a-ant

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
n+1	Write handshaking	ADDR1	Memory Address
n+2	Read handshaking	DATA	*Memory Address++
n+3	Read handshaking	DATA	*Memory Address++
...	...	...	...

18.3.5.2 Flash Write Command

This command is used to write the Flash contents.

The Flash memory plane is organized into several pages. Data to be written are stored in a load buffer that corresponds to a Flash memory page. The load buffer is automatically flushed to the Flash:

- before access to any page other than the current one
- when a new command is validated (MODE = CMDE)

The Write Page command (WP) is optimized for consecutive writes. Write handshaking can be chained; an internal address buffer is automatically increased.

Table 18-7. Write Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	WP or WPL or EWP or EWPL
2	Write handshaking	ADDR0	Memory Address LSB
3	Write handshaking	ADDR1	Memory Address
4	Write handshaking	DATA	*Memory Address++
5	Write handshaking	DATA	*Memory Address++
...	...	...	...
n	Write handshaking	ADDR0	Memory Address LSB
n+1	Write handshaking	ADDR1	Memory Address
n+2	Write handshaking	DATA	*Memory Address++
n+3	Write handshaking	DATA	*Memory Address++
...	...	...	...

The Flash command Write Page and Lock (WPL) is equivalent to the Flash Write Command. However, the lock bit is automatically set at the end of the Flash write operation. As a lock region is composed of several pages, the programmer writes to the first pages of the lock region using Flash write commands and writes to the last page of the lock region using a Flash write and lock command.

The Flash command Erase Page and Write (EWP) is equivalent to the Flash Write Command. However, before programming the load buffer, the page is erased.

The Flash command Erase Page and Write the Lock (EWPL) combines EWP and WPL commands.

18.3.5.3 Flash Full Erase Command

This command is used to erase the Flash memory planes.

19.4.4 Bus Matrix Priority Registers B For Slaves

Name: MATRIX_PRBSx
Offset: 0x84 + x*0x08 [x=0..8]
Reset: 0x00000222
Property: Read/Write

This register can only be written if the WPE bit is cleared in the Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							M12PR[1:0]	
Access							R/W	R/W
Reset							0	0

Bit	15	14	13	12	11	10	9	8
			M11PR[1:0]				M10PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			1	0

Bit	7	6	5	4	3	2	1	0
			M9PR[1:0]				M8PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			1	0			1	0

Bits 0:1, 4:5, 8:9, 12:13, 16:17 – MxPR Master 8 Priority
Fixed priority of Master x for accessing the selected slave. The higher the number, the higher the priority.

All the masters programmed with the same MxPR value for the slave make up a priority pool.

Round-robin arbitration is used in the lowest (MxPR = 0) and highest (MxPR = 3) priority pools.

Fixed priority is used in intermediate priority pools (MxPR = 1) and (MxPR = 2).

See “Arbitration Priority Scheme” for details.

- Can Be Used to Interface a CMOS Digital Image Sensor, an ADC, etc.
- One Clock, 8-bit Parallel Data and Two Data Enable on I/O Lines
- Data Can be Sampled Every Other Time (For Chrominance Sampling Only)
- Supports Connection of One DMA Controller Channel Which Offers Buffer Reception Without Processor Intervention

32.3 Block Diagram

Figure 32-1. Block Diagram

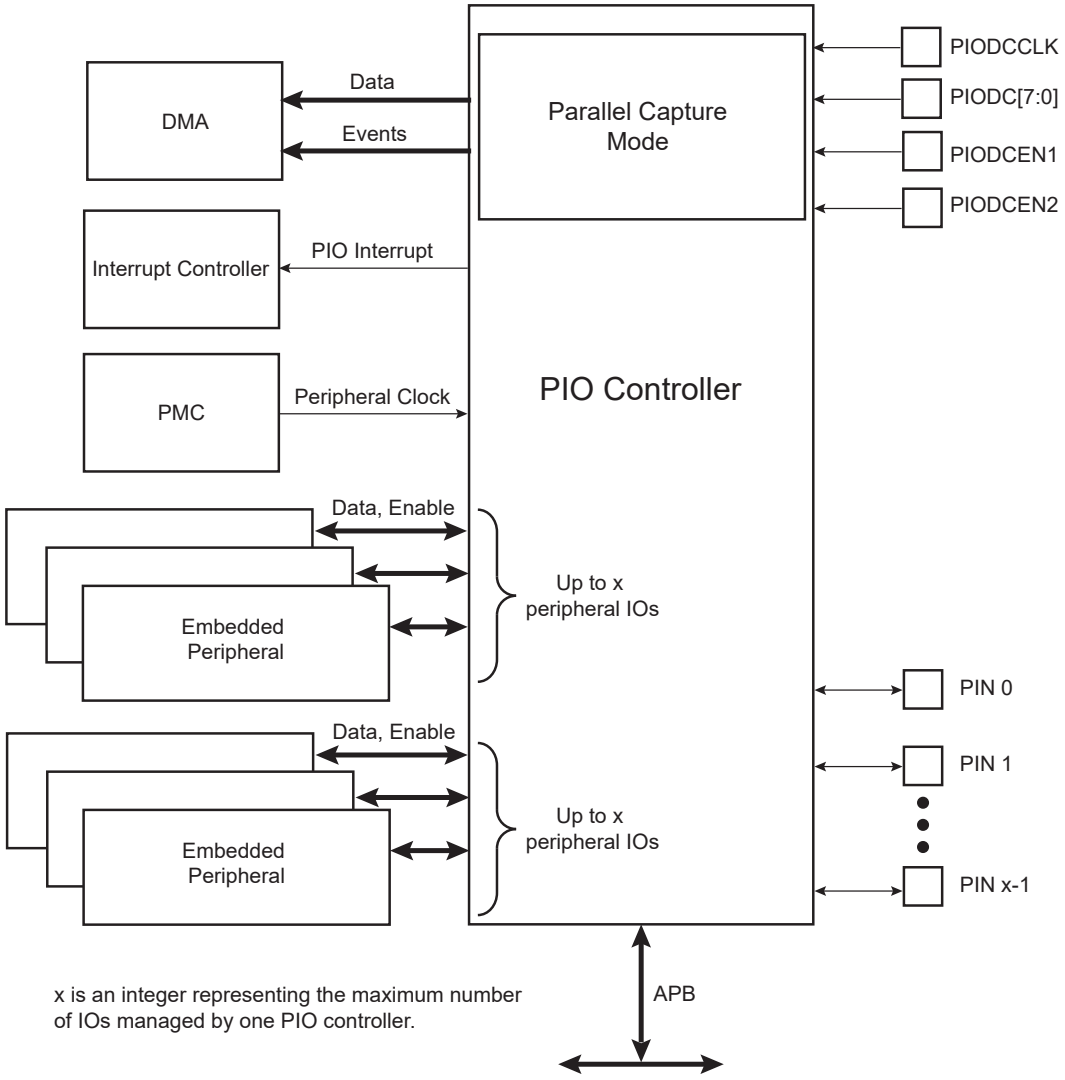


Table 32-1. Signal Description

Signal Name	Signal Description	Signal Type
PIODCCLK	Parallel Capture Mode Clock	Input
PIODC[7:0]	Parallel Capture Mode Data	Input

32.6.1.26 PIO Input Filter Slow Clock Disable Register

Name: PIO_IFSCDR
Offset: 0x0080
Property: Write-only

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Peripheral Clock Glitch Filtering Select

Value	Description
0	No effect.
1	The glitch filter is able to filter glitches with a duration < $t_{peripheral\ clock}/2$.

34.7.10 SDRAMC Configuration Register 1

Name: SDRAMC_CFR1
Offset: 0x28
Reset: 0x00000002
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
								UNAL
Access								R/W
Reset								0

Bit	7	6	5	4	3	2	1	0
					TMRD[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	1	0

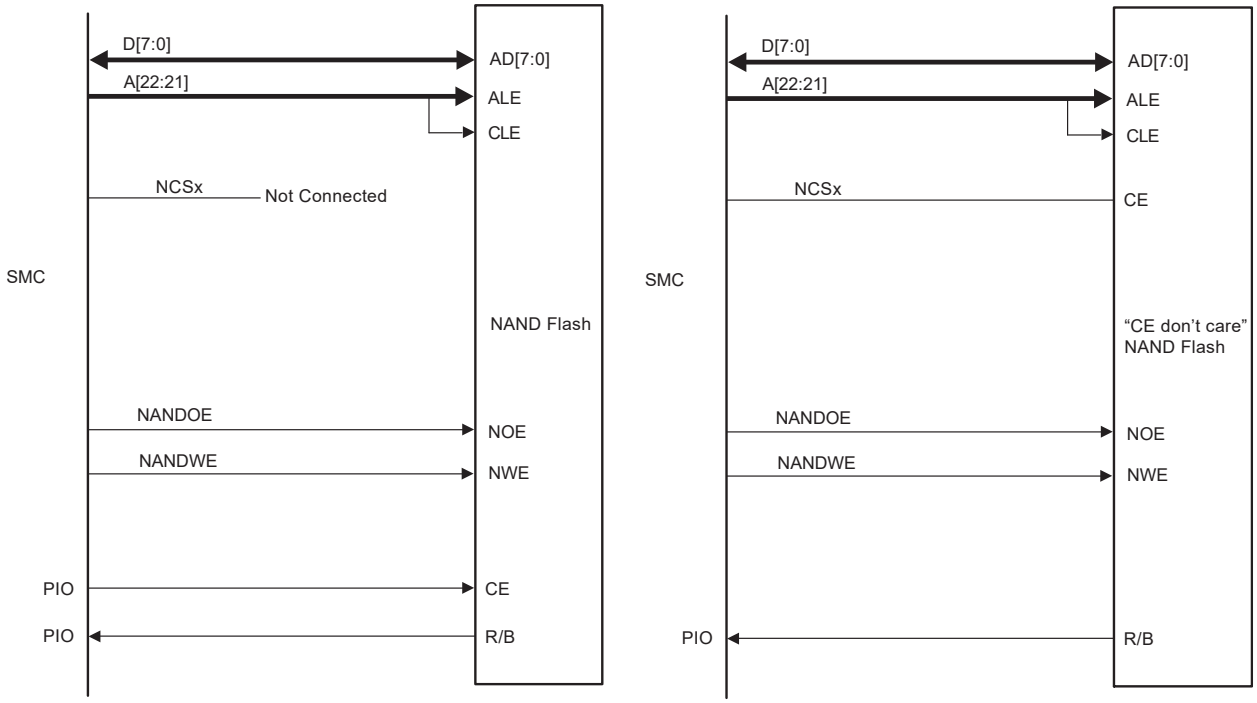
Bit 8 – UNAL Support Unaligned Access
This mode is enabled with masters which have an AXI interface.

Value	Name	Description
0	UNSUPPORTED	Unaligned access is not supported.
1	SUPPORTED	Unaligned access is supported.

Bits 3:0 – TMRD[3:0] Load Mode Register Command to Active or Refresh Command
Reset value is 2 cycles.

This field defines the delay between a “Load Mode Register” command and an active or refresh command in number of cycles. Number of cycles is between 0 and 15.

Figure 35-6. Standard and "CE don't care" NAND Flash Application Examples



Related Links

19. Bus Matrix (MATRIX)

35.8 Application Example

35.8.1 Implementation Examples

Hardware configurations are given for illustration only. The user should refer to the manufacturer web site to check for memory device availability.

For hardware implementation examples, refer to the evaluation kit schematics for this microcontroller, which show examples of a connection to an LCD module and NAND Flash.

35.16.1.9 SMC Write Protection Status Register

Name: SMC_WPSR
Offset: 0xE8
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	WPVSRC[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	WPVSRC[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
								WPVS
Access								
Reset								0

Bits 23:8 – WPVSRC[15:0] Write Protection Violation Source
When WPVS = 1, WPVSRC indicates the register address offset at which a write access has been attempted.

Bit 0 – WPVS Write Protection Violation Status

Value	Description
0	No write protection violation has occurred since the last read of the SMC_WPSR register.
1	A write protection violation has occurred since the last read of the SMC_WPSR register. If this violation is an unauthorized attempt to write a protected register, the associated violation is reported into field WPVSRC.

Value	Name	Description
0	FIXED_AM	The address remains unchanged.
1	INCREMENTED_AM	The addressing mode is incremented (the increment size is set to the data size).
2	UBS_AM	The microblock stride is added at the microblock boundary.
3	UBS_DS_AM	The microblock stride is added at the microblock boundary; the data stride is added at the data boundary.

Bits 17:16 – SAM[1:0] Channel x Source Addressing Mode

Value	Name	Description
0	FIXED_AM	The address remains unchanged.
1	INCREMENTED_AM	The addressing mode is incremented (the increment size is set to the data size).
2	UBS_AM	The microblock stride is added at the microblock boundary.
3	UBS_DS_AM	The microblock stride is added at the microblock boundary, the data stride is added at the data boundary.

Bit 14 – DIF Channel x Destination Interface Identifier
0 (AHB_IF0): The data is written through system bus interface 0.

1 (AHB_IF1): The data is written though system bus interface 1.

Bit 13 – SIF Channel x Source Interface Identifier
0 (AHB_IF0): The data is read through system bus interface 0.

1 (AHB_IF1): The data is read through system bus interface 1.

Bits 12:11 – DWIDTH[1:0] Channel x Data Width

Value	Name	Description
0	BYTE	The data size is set to 8 bits
1	HALFWORD	The data size is set to 16 bits
2	WORD	The data size is set to 32 bits

Bits 10:8 – CSIZE[2:0] Channel x Chunk Size

Value	Name	Description
0	CHK_1	1 data transferred
1	CHK_2	2 data transferred
2	CHK_4	4 data transferred
3	CHK_8	8 data transferred
4	CHK_16	16 data transferred

Bit 7 – MEMSET Channel x Fill Block of Memory
0 (NORMAL_MODE): Memset is not activated.

1 (HW_MODE): Sets the block of memory pointed by DA field to the specified value. This operation is performed on 8-, 16- or 32-bit basis.

Bit 6 – SWREQ Channel x Software Request Trigger
0 (HWR_CONNECTED): Hardware request line is connected to the peripheral request line.

38.8.43 GMAC Pause Frames Transmitted Register

Name: GMAC_PFT
Offset: 0x114
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PFTX[15:0] Pause Frames Transmitted Register
This register counts the number of pause frames transmitted. Only pause frames triggered by the register interface or through the external pause pins are counted as pause frames. Pause frames received through the FIFO interface are counted in the frames transmitted counter.

Offset	Name	Bit Pos.								
0x0524	USBHS_HSTPIPCFG9	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16					PEPNUM[3:0]			
		31:24	INTFRQ[7:0]							
0x0524	USBHS_HSTPIPCFG9 (HSBOHSCP)	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16				PINGEN	PEPNUM[3:0]			
		31:24	BINTERVAL[7:0]							
0x0528 ... 0x052F	Reserved									
0x0530	USBHS_HSTPIPISR0	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	TXSTPI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0530	USBHS_HSTPIPISR0 (INTPIPES)	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0530	USBHS_HSTPIPISR0 (ISOPIPES)	7:0	SHORTPACKETI	CRCERRI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0534	USBHS_HSTPIPISR1	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	TXSTPI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0534	USBHS_HSTPIPISR1 (INTPIPES)	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0534	USBHS_HSTPIPISR1 (ISOPIPES)	7:0	SHORTPACKETI	CRCERRI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0538	USBHS_HSTPIPISR2	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	TXSTPI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						

Value	Description
0	Cleared when USBHS_HSTPIPICR.TXOUTIC = 1.
1	Set when the current OUT bank is free and can be filled. This triggers an interrupt if USBHS_HSTPIPIMR.TXOUTE = 1.

Bit 0 – RXINI Received IN Data Interrupt

Value	Description
0	Cleared when USBHS_HSTPIPICR.RXINIC = 1.
1	Set when a new USB message is stored in the current bank of the pipe. This triggers an interrupt if USBHS_HSTPIPIMR.RXINE = 1.

Value	Description
	• (INRQ+1) in requests have been processed. • A Pipe Reset (USBHS_HSTPIP.PRSTx rising) has occurred. • A Pipe Enable (USBHS_HSTPIP.PEN rising) has occurred.

Bit 16 – PDISHDMA Pipe Interrupts Disable HDMA Request Enable
See the USBHS_DEVEPTIMR.EPDISHDMA bit description.

Bit 14 – FIFOCON FIFO Control
For OUT and SETUP pipes:

0: Cleared when USBHS_HSTPIPIDR.FIFOCONC = 1. This sends the FIFO data and switches the bank.

1: Set when the current bank is free, at the same time as USBHS_HSTPIPISR.TXOUTI or TXSTPI.

For IN pipes:

0: Cleared when USBHS_HSTPIPIDR.FIFOCONC = 1. This frees the current bank and switches to the next bank.

1: Set when a new IN message is stored in the current bank, at the same time as USBHS_HSTPIPISR.RXINI.

Bit 12 – NBUSYBKE Number of Busy Banks Interrupt Enable

Value	Description
0	Cleared when USBHS_HSTPIPIDR.NBUSYBKEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.NBUSYBKE).
1	Set when USBHS_HSTPIPIER.NBUSYBKES = 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.NBUSYBKE).

Bit 7 – SHORTPACKETIE Short Packet Interrupt Enable
If this bit is set for non-control OUT pipes, a short packet transmission is guaranteed upon ending a DMA transfer, thus signaling an end of transfer, provided that the End of DMA Buffer Output Enable (USBHS_HSTDMACONTROL.END_B_EN) bit and the Automatic Switch (USBHS_HSTPIPCFG.AUTOSW) bit = 1.

Value	Description
0	Cleared when USBHS_HSTPIPIDR.SHORTPACKETEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.SHORTPACKETE).
1	Set when USBHS_HSTPIPIER.SHORTPACKETIES = 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.SHORTPACKETIE).

Bit 6 – RXSTALLDE Received STALLed Interrupt Enable

Value	Description
0	Cleared when USBHS_HSTPIPIDR.RXSTALLDEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.RXSTALLDE).
1	Set when USBHS_HSTPIPIER.RXSTALLDES= 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.RXSTALLDE).

Bit 5 – OVERFIE Overflow Interrupt Enable

Bit 5 – OVERFIEC Overflow Interrupt Disable

Bit 4 – NAKEDEC NAKed Interrupt Disable

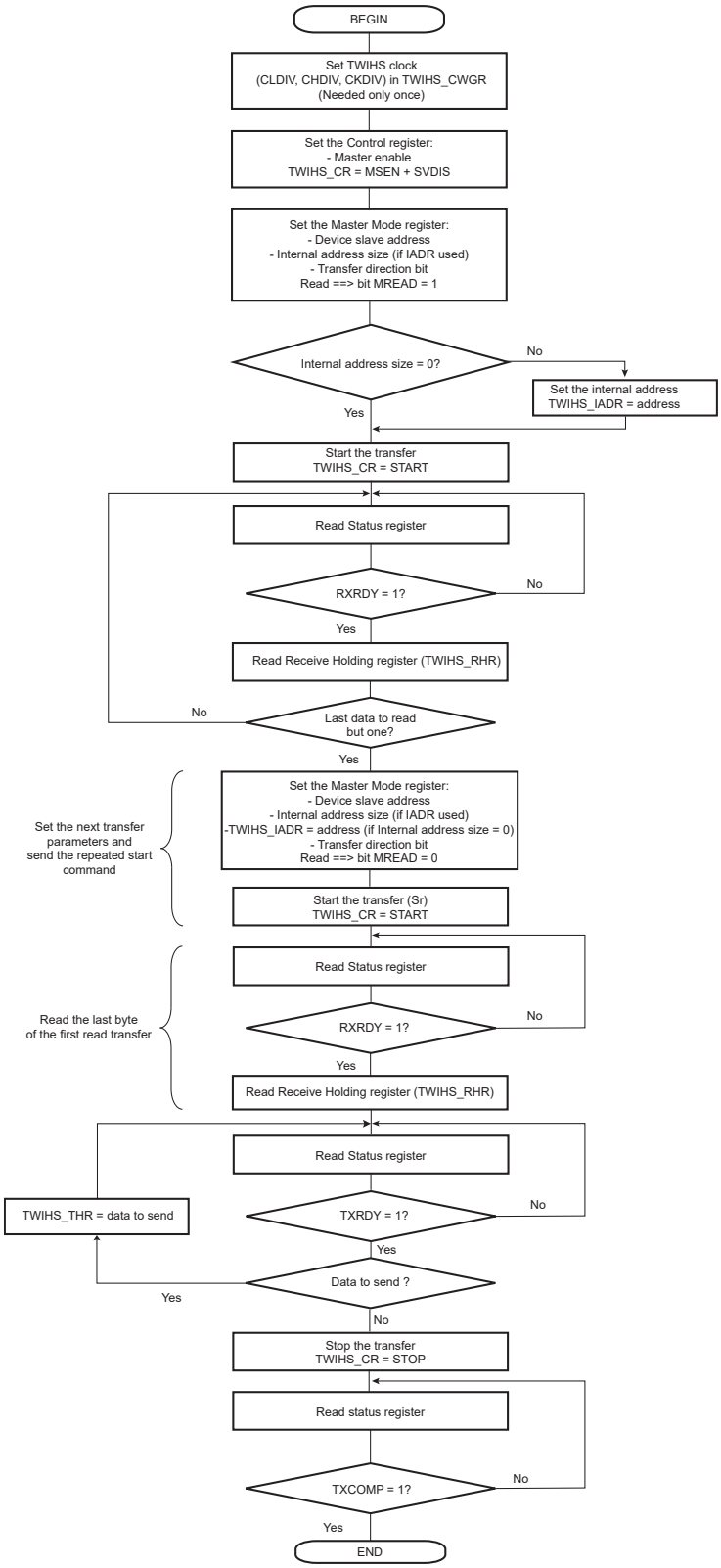
Bit 3 – PERREC Pipe Error Interrupt Disable

Bit 2 – UNDERFIEC Underflow Interrupt Disable

Bit 1 – TXOUTEC Transmitted OUT Data Interrupt Disable

Bit 0 – RXINEC Received IN Data Interrupt Disable

Figure 43-26. TWIHS Read Operation with Multiple Data Bytes + Write Operation with Multiple Data Bytes (Sr)



43.7.15 TWIHS Write Protection Mode Register

Name: TWIHS_WPMR
Offset: 0xE4
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	WPKEY[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	WPKEY[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	WPKEY[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
								WPEN
Access								R/W
Reset								0

Bits 31:8 – WPKEY[23:0] Write Protection Key

Value	Name	Description
0x545749	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

Bit 0 – WPEN Write Protection Enable
See Register Write Protection for the list of registers that can be write-protected.

Value	Description
0	Disables the write protection if WPKEY corresponds to 0x545749 (“TWI” in ASCII).
1	Enables the write protection if WPKEY corresponds to 0x545749 (“TWI” in ASCII).

43.7.16 TWIHS Write Protection Status Register

Name: TWIHS_WPSR
Offset: 0xE8
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	WPVSRC[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	WPVSRC[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	WPVSRC[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
								WPVS
Access								R
Reset								0

Bits 31:8 – WPVSRC[23:0] Write Protection Violation Source
When WPVS = 1, WPVSRC indicates the register address offset at which a write access has been attempted.

Bit 0 – WPVS Write Protection Violation Status

Value	Description
0	No write protection violation has occurred since the last read of the TWIHS_WPSR.
1	A write protection violation has occurred since the last read of the TWIHS_WPSR. If this violation is an unauthorized attempt to write a protected register, the associated violation is reported into field WPVSRC.

49.6.4 MCAN Data Bit Timing and Prescaler Register

Name: MCAN_DBTP
Offset: 0x0C
Reset: 0x00000A33
Property: Read/Write

This register can only be written if the bits CCE and INIT are set in MCAN CC Control Register.

The CAN bit time may be programmed in the range of 4 to 25 time quanta. The CAN time quantum may be programmed in the range of 1 to 32 CAN core clock periods. t_q = (DBRP + 1) CAN core clock periods.

DTSEG1 is the sum of Prop_Seg and Phase_Seg1. DTSEG2 is Phase_Seg2.

Therefore the length of the bit time is (programmed values) [DTSEG1 + DTSEG2 + 3] t_q
or (functional values) [Sync_Seg + Prop_Seg + Phase_Seg1 + Phase_Seg2] t_q.

The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

With a CAN core clock frequency of 8 MHz, the reset value of 0x00000A33 configures the MCAN for a fast bit rate of 500 kbit/s.

The bit rate configured for the CAN FD data phase via MCAN_DBTP must be higher than or equal to the bit rate configured for the arbitration phase via MCAN_NBTP.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	TDC			DBRP[4:0]				
Access	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				DTSEG1[4:0]				
Access				R/W	R/W	R/W	R/W	R/W
Reset				0	1	0	1	0

Bit	7	6	5	4	3	2	1	0
	DTSEG2[3:0]					DSJW[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	1	1		0	1	1

Bit 23 – TDC Transmitter Delay Compensation
0 (DISABLED): Transmitter Delay Compensation disabled.

1 (ENABLED): Transmitter Delay Compensation enabled.

52.7.10 AFEC Interrupt Enable 1 Register

Name: AFEC_IER
Offset: 0x24
Reset: –
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
		TEMPCHG				COMPE	GOVRE	DRDY
Access		W				W	W	W
Reset		–				–	–	–

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					EOC11	EOC10	EOC9	EOC8
Access					W	W	W	W
Reset					–	–	–	–

Bit	7	6	5	4	3	2	1	0
	EOC7	EOC6	EOC5	EOC4	EOC3	EOC2	EOC1	EOC0
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bit 30 – TEMPCHG Temperature Change Interrupt Enable

Bit 26 – COMPE Comparison Event Interrupt Enable

Bit 25 – GOVRE General Overrun Error Interrupt Enable

Bit 24 – DRDY Data Ready Interrupt Enable

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 – EOCx End of Conversion Interrupt Enable x

Symbol	Parameter	Digital Code	Min	Typ	Max	Unit
		1110	–	3.28	–	
		1111	–	3.4	–	

Figure 59-3. VDDIO Supply Monitor

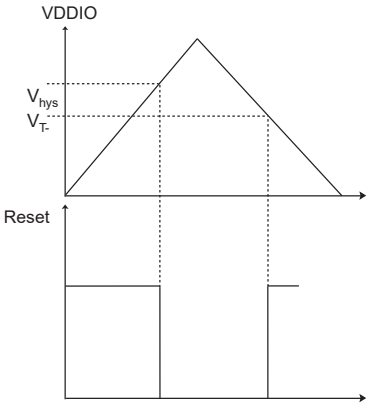
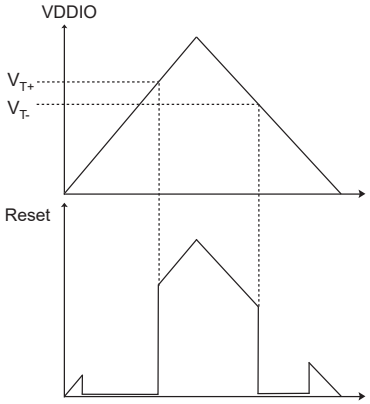


Table 59-10. VDDIO Power-On Reset Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{T+}	Threshold Voltage Rising	–	1.45	1.53	1.61	V
V_{T-}	Threshold Voltage Falling	–	1.37	1.46	–	V
V_{hys}	Hysteresis	–	40	80	130	mV
t_{RES}	Reset Time-out Period	–	240	320	800	µs

Figure 59-4. VDDIO Power-On Reset Characteristics



59.3 Power Consumption

- Power consumption of the device depending on the different Low-Power modes (Backup, Wait, Sleep) and Active mode
- Power consumption on power supply in different modes: Backup, Wait, Sleep and Active
- Power consumption by peripheral:

Signal Name	Recommended Pin Connection	Description
PCx PDx PEx		Refer to the column “Reset State” of the pin description tables in the section "Package and Pinout". Schmitt trigger on all inputs. To reduce power consumption if not used, the concerned PIO can be configured as an output, driven at ‘0’ with internal pullup disabled.

Related Links

6. Package and Pinout

60.2.6 Parallel Capture Mode

Signal Name	Recommended Pin Connection	Description
PIODC0–7	Application dependent. (Pullup at VDDIO)	Parallel mode capture data All are pulled-up inputs (100 kOhm) to VDDIO at reset.
PIODCCLK	Application dependent. (Pullup at VDDIO)	Parallel mode capture clock Pulled-up input (100 kOhm) to VDDIO at reset.
PIODCEN1–2	Application dependent. (Pullup at VDDIO)	Parallel mode capture mode enable All are pulled-up inputs (100 kOhm) to VDDIO at reset.

60.2.7 Analog Reference, Analog Front-End and DAC

Signal Name	Recommended Pin Connection	Description
Analog Voltage References		
VREFP	1.7V to VDDIN LC Filter is required.	Positive reference voltage. VREFP is a pure analog input. VREFP is the voltage reference for the AFEC (ADC, PGA DAC and Analog Comparator). To reduce power consumption, if analog features are not used, connect VREFP to GND. Noise must be lower than 100 µVrms
VREFN	Analog Negative Reference	AFE, DAC and Analog Comparator negative reference VREFN must be connected to GND or GNDANA.
12-bit Analog Front-End		