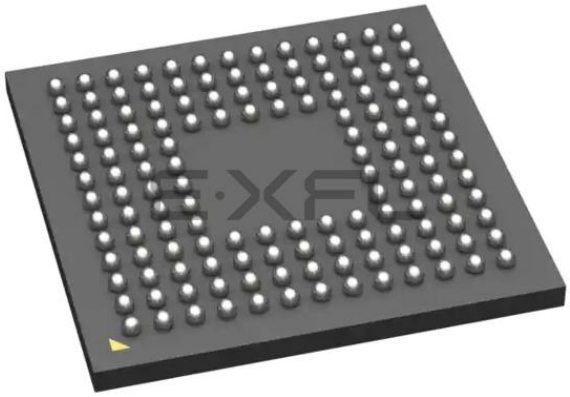

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-UFBGA
Supplier Device Package	144-UFBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70q21a-cfn

Table 1-3. SAM V70 Family Features (Without CAN-FD, Ethernet Control)

Device	Flash Memory (KB)	Multi-port SRAM Memory (KB)	Pins	Packages	Digital Peripherals																					Analog		
					USB (see Note	USART/UART	QSPI	USART/SPI	TWIHS	HSMCI port/bits	CAN-FD	Media LB	Image Sensor Interface (ISI)	SPI0	SPI1	External Bus Interface (EBI)	SDRAM Interface	DMA Channels	SSC	ETM	Timer Counter Channels	Timer Counter Channels I/O	I2SC	I/O Pins	12-bit ADC Channels	Analog Comparators	DAC (Channels)
SAMV70Q19	512	256	144	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	2	Y	12 -bit	Y	Y	Y	Y	24	Y	Y	12	36	2	114	24	Y	2
SAMV70Q20	1024	384																									
SAMV70N19	512	256	100	LQFP, TFBGA	HS	3/5	Y	3	3	1/4	2	Y	12 -bit	Y	N	N	N	24	Y	Y	12	9	1	75	10	Y	2
SAMV70N20	1024	384																									
SAMV70J19	512	256	64	LQFP	FS	2/3	SPI only	0	2	N	1	N	8-bit	N	N	N	N	24	Y	Y	12	3	0	44	5	Y	1
SAMV70J20	1024	384																									

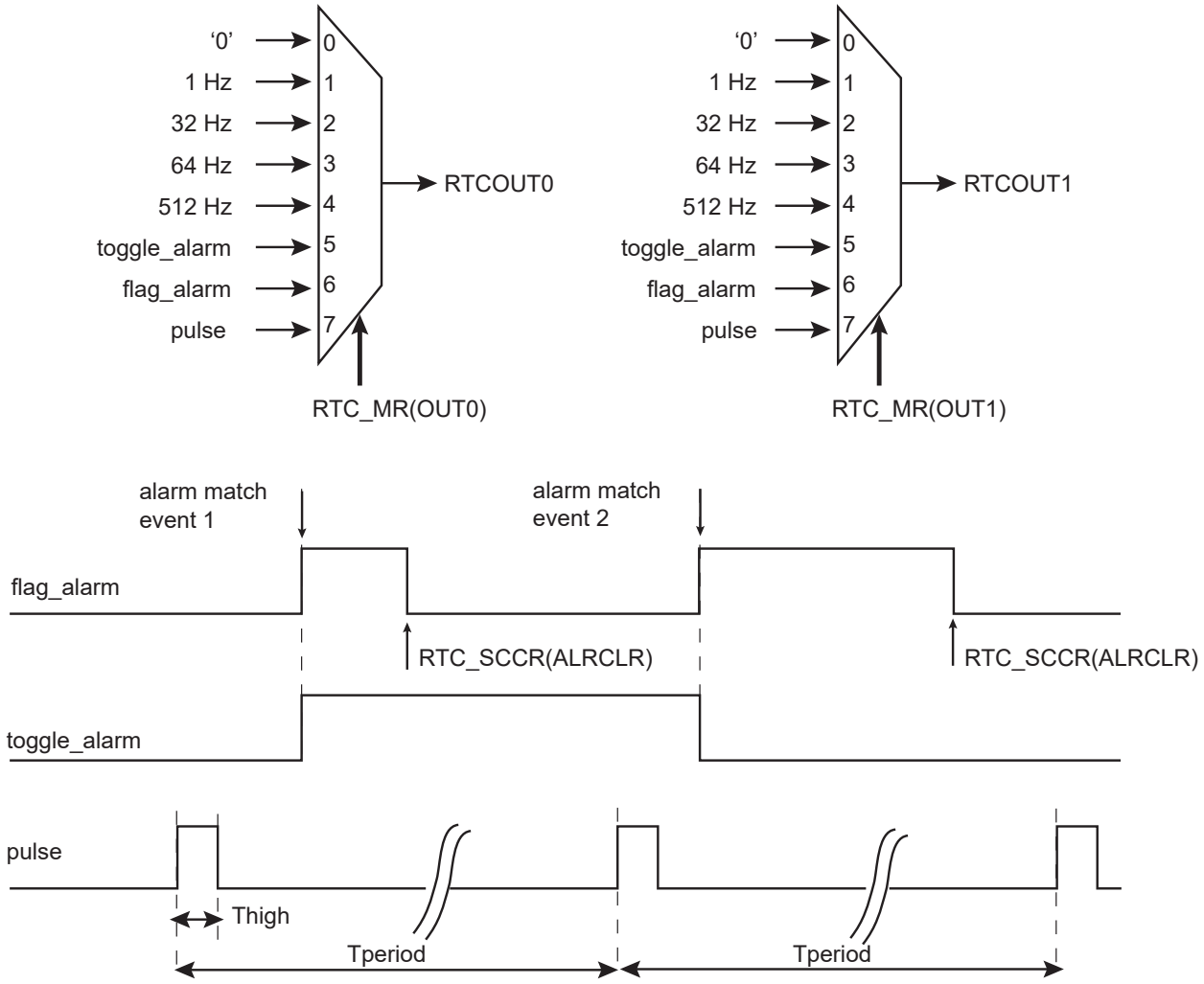
Note: HS = High-Speed; FS = Full-Speed.

Table 1-4. SAM S70 Family Features (Without CAN-FD, Ethernet AVB and Media LB)

Device	Flash Memory (KB)	Multi-port SRAM Memory (KB)	Pins	Packages	Digital Peripherals																		Analog		
					USB (see Note)	USART/UART	QSPI	USART/SPI	TWIHS	HSMCI port/bits	Image Sensor Interface (ISI)	SPI0	SPI1	External Bus Interface (EBI)	SDRAM Interface	DMA Channels	SSC	ETM	Timer Counter Channels	Timer Counter Channels I/O	I2SC	I/O Pins	12-bit ADC Channels	Analog Comparators	DAC Channels
SAMS70Q19	512	256	144	LQFP, LFBGA, UFBGA	HS	3/5	Y	3	3	1/4	12 -bit	Y	Y	Y	Y	24	Y	Y	12	36	2	114	24	Y	2
SAMS70Q20	1024	384																							
SAMS70Q21	2048																								
SAMS70N19	512	256	100	LQFP, TFBGA, VFBGA	HS	3/5	Y	3	3	1/4	12 -bit	Y	N	N	N	24	Y	Y	12	9	1	75	10	Y	2
SAMS70N20	1024	384																							
SAMS70N21	2048																								
SAMS70J19	512	256	64	LQFP, QFN	FS	0/5	SPI only	0	2	N	8-bit	N	N	N	N	24	Y	Y	12	3	0	44	5	Y	1
SAMS70J20	1024	384																							
SAMS70J21	2048																								

Note: HS = High-Speed; FS = Full-Speed.

Figure 27-6. Waveform Generation



The user can adjust the value of the Main RC oscillator frequency by modifying the trimming values done in production on 8 MHz and 12 MHz. This may be used to compensate frequency drifts due to temperature or voltage. The values stored in the Flash cannot be erased by a Flash erase command or by the ERASE signal. Values written by the user application in the Oscillator Calibration Register (PMC_OCR) are reset after each power-up or peripheral reset.

By default, SEL4/SEL8/SEL12 are cleared, so the Main RC oscillator is driven with the factory-programmed Flash calibration bits which are programmed during chip production.

In order to calibrate the oscillator lower frequency, SEL4 must be set to ‘1’ and a valid frequency value must be configured in CAL4. Likewise, SEL8/12 must be set to ‘1’ and a trim value must be configured in CAL8/12 in order to adjust the other frequencies of the oscillator.

It is possible to adjust the oscillator frequency while operating from this oscillator. For example, when running on lowest frequency, it is possible to change the CAL4 value if SEL4 is set in PMC_OCR.

At any time, the user can measure the main RC oscillator output frequency by means of the Main Frequency Counter (refer to "Main Frequency Counter"). Once the frequency measurement is done, the main RC oscillator calibration fields (CALMIN, CALx) can be adjusted accordingly to correct this oscillator output frequency.

Related Links

58. Electrical Characteristics for SAM V70/V71
59. Electrical Characteristics for SAM E70/S70

30.5.3 Main Crystal Oscillator

After reset, the Main crystal oscillator is disabled and is not selected as the source of MAINCK.

As the source of MAINCK, the Main crystal oscillator provides a very precise frequency. The software enables or disables this oscillator in order to reduce power consumption via CKGR_MOR.MOSCXTEN.

When disabling this oscillator by clearing the CKGR_MOR.MOSCXTEN, PMC_SR.MOSCXTS is automatically cleared, indicating the oscillator is off.

When enabling this oscillator, the user must initiate the startup time counter. The startup time depends on the characteristics of the external device connected to this oscillator.

When CKGR_MOR.MOSCXTEN and CKGR_MOR.MOSCXTST are written to enable this oscillator, the PIO lines multiplexed with XIN and XOUT are driven by the Main crystal oscillator. PMC_SR.MOSCXTS is cleared and the counter starts counting down on SLCK divided by 8 from the CKGR_MOR.MOSCXTST value. Since the CKGR_MOR.MOSCXTST value is coded with 8 bits, the startup time can be programmed up to 65536 SLCKperiods, corresponding to about 62 ms when running at 32.768 kHz.

When the startup time counter reaches ‘0’, PMC_SR.MOSCXTS is set, indicating that the oscillator is stabilized. Setting the MOSCXTS bit in the Interrupt Mask Register (PMC_IMR) can trigger an interrupt to the processor.

30.5.4 Main Clock Source Selection

The source of MAINCK can be selected from the following:

- The Main RC oscillator
- The Main crystal oscillator
- An external clock signal provided on the XIN input (Bypass mode of the Main crystal oscillator)

The advantage of the Main RC oscillator is its fast startup time. By default, this oscillator is selected to start the system and it must be selected prior to entering Wait mode.

Clock Name	Peripheral
PCK5	MCANx
PCK6	TCx
PCK7	TC0

Note: USB, GMAC and MLB do not require PCKx to operate independently of core and bus peripherals.

31.9 Peripheral and Generic Clock Controller

The PMC controls the clocks of the embedded peripherals by means of the Peripheral Control register (PMC_PCR). With this register, the user can enable and disable the different clocks used by the peripherals:

- Peripheral clocks (periph_clk[PID]), routed to every peripheral and derived from the master clock (MCK), and
- Generic clocks (GCLK[PID]), routed to I2SC0 and I2SC1. These clocks are independent of the core and bus clocks (HCLK, MCK and periph_clk[PID]). They are generated by selection and division of the following sources: SLCK, MAINCK, UPLLCKDIV, PLLACK and MCK. Refer to the description of each peripheral for the limitation to be applied to GCLK[PID] compared to periph_clk[PID].

To configure a peripheral's clocks, PMC_PCR.CMD must be written to '1' and PMC_PCR.PID must be written with the index of the corresponding peripheral. All other configuration fields must be correctly set.

To read the current clock configuration of a peripheral, PMC_PCR.CMD must be written to '0' and PMC_PCR.PID must be written with the index of the corresponding peripheral regardless of the values of other fields. This write does not modify the configuration of the peripheral. The PMC_PCR can then be read to know the configuration status of the corresponding PID.

The user can also enable and disable these clocks by configuring the Peripheral Clock Enable (PMC_PCERx) and Peripheral Clock Disable (PMC_PCDRx) registers. The status of the peripheral clock activity can be read in the Peripheral Clock Status registers (PMC_PCSRx).

When a peripheral or a generic clock is disabled, it is immediately stopped. These clocks are disabled after a reset.

To stop a peripheral clock, it is recommended that the system software wait until the peripheral has executed its last programmed operation before disabling the clock. This is to avoid data corruption or erroneous behavior of the system.

The bit number in PMC_PCERx, PMC_PCDRx, and PMC_PCSRx is the Peripheral Identifier defined at the product level. The bit number corresponds to the interrupt source number assigned to the peripheral.

31.10 Asynchronous Partial Wakeup

31.10.1 Description

The asynchronous partial wakeup wakes up a peripheral in a fully asynchronous way when activity is detected on the communication line. The asynchronous partial wakeup function automatically manages the peripheral clock. It reduces overall power consumption of the system by clocking peripherals only when needed.

Asynchronous partial wakeup can be enabled in Wait mode (SleepWalking), or in Active mode.

Value	Name	Description
3	CLK_8	Selected clock divided by 8
4	CLK_16	Selected clock divided by 16
5	CLK_32	Selected clock divided by 32
6	CLK_64	Selected clock divided by 64
7	CLK_3	Selected clock divided by 3

Bits 1:0 – CSS[1:0] Master Clock Source Selection

Value	Name	Description
0	SLOW_CLK	SLCK is selected
1	MAIN_CLK	MAINCK is selected
2	PLLA_CLK	PLLACK is selected
3	UPLL_CLK	UPPLLCKDIV is selected

Value	Description
0	Default value stored in Flash memory.
1	Value written by user in CAL4 field of this register.

Bits 6:0 – CAL4[6:0] Main RC Oscillator Calibration Bits for 4 MHz
Calibration bits applied to the RC Oscillator when SEL4 is set.

32.6.1.24 PIO Peripheral ABCD Select Register 1

Name: PIO_ABCDSR1
Offset: 0x0070
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Peripheral Select
If the same bit is set to '0' in PIO_ABCDSR2:

0: Assigns the I/O line to the Peripheral A function.

1: Assigns the I/O line to the Peripheral B function.

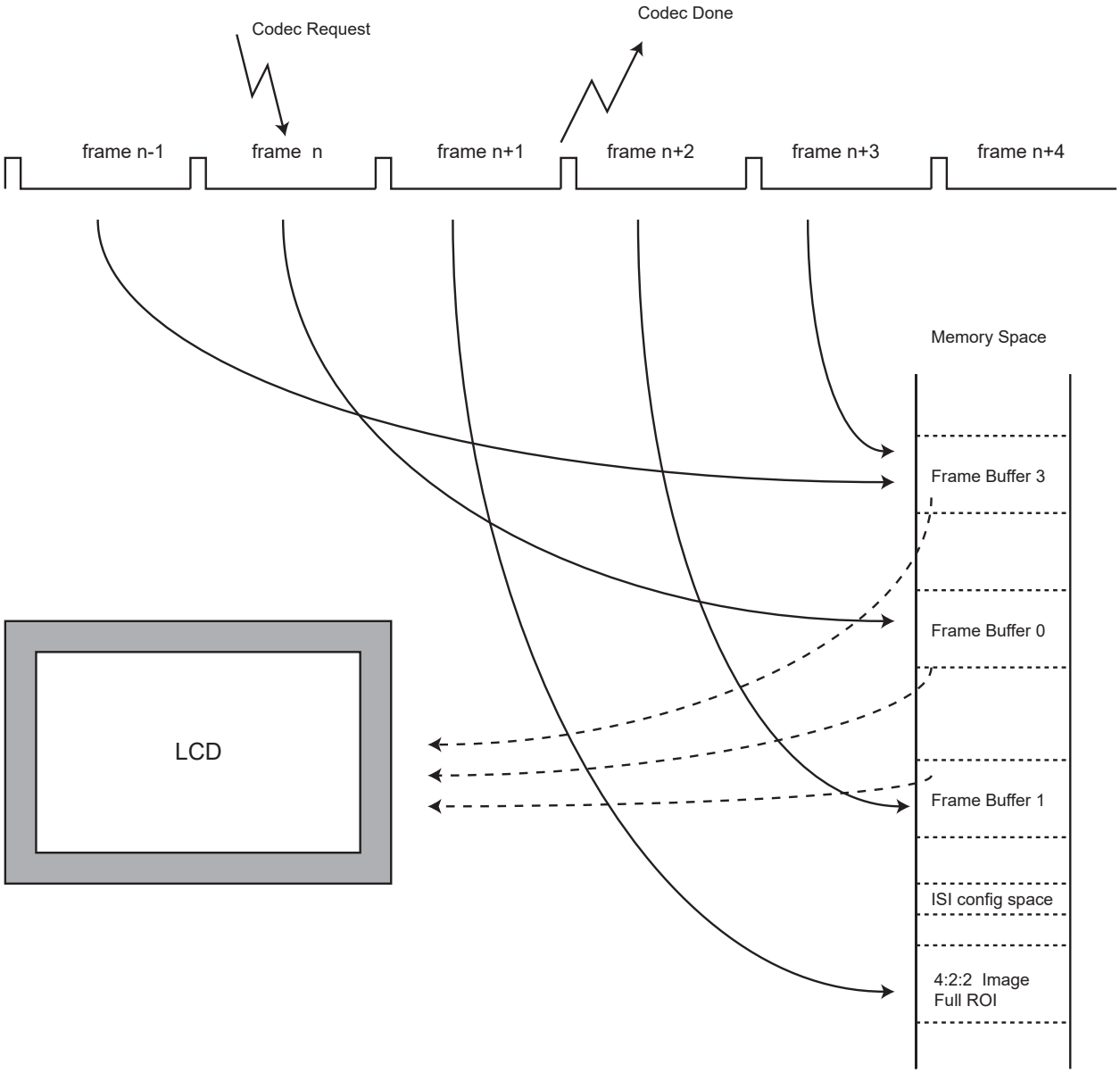
If the same bit is set to '1' in PIO_ABCDSR2:

0: Assigns the I/O line to the Peripheral C function.

1: Assigns the I/O line to the Peripheral D function.

Using this technique, several frame buffers can be configured through the linked list. The following figure illustrates a typical three-frame buffer application. Frame n is mapped to frame buffer 0, frame n+1 is mapped to frame buffer 1, frame n+2 is mapped to frame buffer 2 and further frames wrap. A codec request occurs, and the full-size 4:2:2 encoded frame is stored in a dedicated memory space.

Figure 37-6. Three Frame Buffers Application and Memory Mapping



37.5.5 Codec Path

37.5.5.1 Color Space Conversion

Depending on user selection, this module can be bypassed so that input YCrCb stream is directly connected to the format converter module. If the RGB input stream is selected, this module converts RGB to YCrCb color space with the formulas given below:

38.8.3 GMAC Network Status Register

Name: GMAC_NSR
Offset: 0x008
Reset: 0x000001X0
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						IDLE	MDIO	
Access						R	R	
Reset						0	0	

Bit 2 – IDLE PHY Management Logic Idle
The PHY management logic is idle (i.e., has completed).

Bit 1 – MDIO MDIO Input Status
Returns status of the MDIO pin.

Offset	Name	Bit Pos.								
0x0670	USBHS_HSTPIPINRQ8	7:0	INRQ[7:0]							
		15:8								INMODE
		23:16								
		31:24								
0x0674	USBHS_HSTPIPINRQ9	7:0	INRQ[7:0]							
		15:8								INMODE
		23:16								
		31:24								
0x0678 ... 0x067F	Reserved									
0x0680	USBHS_HSTPIPERR0	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0684	USBHS_HSTPIPERR1	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0688	USBHS_HSTPIPERR2	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x068C	USBHS_HSTPIPERR3	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0690	USBHS_HSTPIPERR4	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0694	USBHS_HSTPIPERR5	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0698	USBHS_HSTPIPERR6	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x069C	USBHS_HSTPIPERR7	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x06A0	USBHS_HSTPIPERR8	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								

39.6.44 Host Pipe x Configuration Register (High-speed Bulk-out or High-speed Control Pipe)

Name: USBHS_HSTPIPCFGx (HSBOHSCP)
Offset: 0x0500 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

This configuration is relevant only if PTYPE = 0x0 or 0x2 in "Host Pipe x Configuration Register".

Bit	31	30	29	28	27	26	25	24
	BINTERVAL[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
				PINGEN	PEPNUM[3:0]			
Access								
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
Access								
Reset			0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
		PSIZE[2:0]			PBK[1:0]		ALLOC	
Access								
Reset		0	0	0	0	0	0	

Bits 31:24 – BINTERVAL[7:0] bInterval Parameter for the Bulk-Out/Ping Transaction
This field contains the Ping/Bulk-out period.

• If BINTERVAL > 0 and PINGEN = 1, one PING token is sent every bInterval microframe until it is ACKed by the peripheral.

• If BINTERVAL = 0 and PINGEN = 1, multiple consecutive PING tokens are sent in the same microframe until they are ACKed.

• If BINTERVAL > 0 and PINGEN = 0, one OUT token is sent every bInterval microframe until it is ACKed by the peripheral.

• If BINTERVAL = 0 and PINGEN = 0, multiple consecutive OUT tokens are sent in the same microframe until they are ACKed.

This value must be in the range from 0 to 255.

Bit 20 – PINGEN Ping Enable
This bit is relevant for High-speed Bulk-out transaction only (including the control data stage and the control status stage).

This bit is cleared upon sending a USB reset.

39.6.64 Host Pipe x Error Register

Name: USBHS_HSTPIPERRx
Offset: 0x0680 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

Writing a zero in a bit/field in this register clears the bit/field. Writing a one has no effect.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
Access								
Reset		0	0	0	0	0	0	0

Bits 6:5 – COUNTER[1:0] Error Counter
This field is incremented each time an error occurs (CRC16, TIMEOUT, PID, DATAPID or DATATGL).

This field is cleared when receiving a USB packet free of error.

When this field reaches 3 (i.e., 3 consecutive errors), this pipe is automatically frozen (USBHS_HSTPIPIMRx.PFREEZE is set).

Bit 4 – CRC16 CRC16 Error

Value	Description
0	No CRC16 error occurred since last clear of this bit.
1	This bit is automatically set when a CRC16 error has been detected.

Bit 3 – TIMEOUT Time-Out Error

Value	Description
0	No Time-Out error occurred since last clear of this bit.
1	This bit is automatically set when a Time-Out error has been detected.

Bit 2 – PID PID Error

40.14.20 HSMCI FIFOx Memory Aperture

Name: HSMCI_FIFOx [x=0..255]
Offset: 0x00
Reset: 0
Property: R/W

Bit	31	30	29	28	27	26	25	24
	DATA[31:24]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DATA[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – DATA[31:0] Data to Read or Data to Write

42.7.8 QSPI Interrupt Mask Register

Name: QSPI_IMR
Offset: 0x1C
Reset: 0x00000000
Property: Read-only

The following configuration values are valid for all listed bit names of this register:

0: The corresponding interrupt is not enabled.

1: The corresponding interrupt is enabled.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
						INSTRE	CSS	CSR
Access						R	R	R
Reset						0	0	0

Bit	7	6	5	4	3	2	1	0
					OVRES	TXEMPTY	TDRE	RDRF
Access					R	R	R	R
Reset					0	0	0	0

Bit 10 – INSTRE Instruction End Interrupt Mask

Bit 9 – CSS Chip Select Status Interrupt Mask

Bit 8 – CSR Chip Select Rise Interrupt Mask

Bit 3 – OVRES Overrun Error Interrupt Mask

Bit 2 – TXEMPTY Transmission Registers Empty Mask

Bit 1 – TDRE Transmit Data Register Empty Interrupt Mask

Bit 0 – RDRF Receive Data Register Full Interrupt Mask

46.7.36 USART LON Preamble Register

Name: US_LONPR
Offset: 0x0064
Reset: 0x0
Property: Read/Write

This register is relevant only if USART_MODE = 0x9 in the USART Mode Register.

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
			LONPL[13:8]					
Access								
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LONPL[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 13:0 – LONPL[13:0] LON Preamble Length

Value	Description
1–16383	LON preamble length in t_{bit} (without byte-sync).

48.7.25 AHB Control Register

Name: MLB_ACTL
Offset: 0x3C0
Reset: 0x00000000
Property: Read/Write

The AHB Control (MLB_ACTL) register is written by the HC to configure the AHB block for channel interrupts. MLB_ACTL contains three configuration fields, one is used to select the DMA mode, one is used to multiplex channel interrupts onto a single interrupt signal, and the last selects the method of clearing channel interrupts (either software or hardware).

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				MPB		DMA_MODE	SMX	SCE
Access								
Reset				0		0	0	0

Bit 4 – MPB DMA Packet Buffering Mode
0 (SINGLE_PACKET): Single-packet mode

1 (MULTIPLE_PACKET): Multiple-packet mode

Bit 2 – DMA_MODE DMA Mode

Value	Description
0	DMA Mode 0
1	DMA Mode 1

Bit 1 – SMX AHB Interrupt Mux Enable

Value	Description
0	MLB_ACSR0 generates an interrupt on MediaLB IRQ0; MLB_ACSR1 generates an interrupt on MediaLB IRQ1
1	MLB_ACSR0 and MLB_ACSR1 generate an interrupts on MediaLB IRQ0 only

Bit 0 – SCE Software Clear Enable

52.7 Register Summary

Offset	Name	Bit Pos.								
0x00	AFEC_CR	7:0							START	SWRST
		15:8								
		23:16								
		31:24								
0x04	AFEC_MR	7:0	FREERUN	FWUP	SLEEP		TRGSEL[2:0]			TRGEN
		15:8	PRESCAL[7:0]							
		23:16	ONE				STARTUP[3:0]			
		31:24	USEQ		TRANSFER[1:0]		TRACKTIM[3:0]			
0x08	AFEC_EMR	7:0	CMPSEL[4:0]						CMPMODE[1:0]	
		15:8			CMPFILTER[1:0]				CMPALL	
		23:16						RES[2:0]		
		31:24			SIGNMODE[1:0]				STM	TAG
0x0C	AFEC_SEQ1R	7:0	USCH1[3:0]				USCH0[3:0]			
		15:8	USCH3[3:0]				USCH2[3:0]			
		23:16	USCH5[3:0]				USCH4[3:0]			
		31:24	USCH7[3:0]				USCH6[3:0]			
0x10	AFEC_SEQ2R	7:0	USCH9[3:0]				USCH8[3:0]			
		15:8	USCH11[3:0]				USCH10[3:0]			
		23:16								
		31:24								
0x14	AFEC_CHER	7:0	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
		15:8					CH11	CH10	CH9	CH8
		23:16								
		31:24								
0x18	AFEC_CHDR	7:0	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
		15:8					CH11	CH10	CH9	CH8
		23:16								
		31:24								
0x1C	AFEC_CHSR	7:0	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
		15:8					CH11	CH10	CH9	CH8
		23:16								
		31:24								
0x20	AFEC_LCDR	7:0	LDATA[7:0]							
		15:8	LDATA[15:8]							
		23:16								
		31:24				CHNB[3:0]				
0x24	AFEC_IER	7:0	EOC7	EOC6	EOC5	EOC4	EOC3	EOC2	EOC1	EOC0
		15:8					EOC11	EOC10	EOC9	EOC8
		23:16								
		31:24		TEMPCHG				COMPE	GOVRE	DRDY
0x28	AFEC_IDR	7:0	EOC7	EOC6	EOC5	EOC4	EOC3	EOC2	EOC1	EOC0
		15:8					EOC11	EOC10	EOC9	EOC8
		23:16								

56.6.2 TRNG Interrupt Enable Register

Name: TRNG_IER
Offset: 0x10
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								DATRDY
Access								W
Reset								–

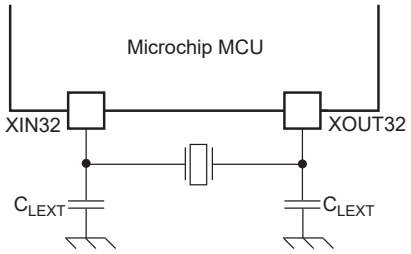
Bit 0 – DATRDY Data Ready Interrupt Enable

Value	Description
0	No effect.
1	Enables the corresponding interrupt.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{XIN_IL}	V_{XIN} Input Low-level Voltage	(see **Note**)	Min of V_{IL} for CLOCK pad	–	Max of V_{IL} for CLOCK pad	V
V_{XIN_IH}	V_{XIN} Input High-level Voltage	(see **Note**)	Min of V_{IH} for CLOCK pad	–	Max of V_{IH} for CLOCK pad	V

Note: These characteristics apply only when the 32.768 kHz crystal oscillator is in Bypass mode.

Figure 59-9. 32.768 kHz Crystal Oscillator Schematics



$C_{LEXT} = 2 \times (C_{CRYSTAL} - C_{PARA} - C_{PCB})$

where C_{PCB} is the capacitance of the printed circuit board (PCB) track layout from the crystal to the pin.

59.4.4 32.768 kHz Crystal Characteristics

Table 59-21. 32.768 kHz Crystal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistor	Crystal at 32.768 kHz	–	50	100	kOhm
C_M	Motional Capacitance	Crystal at 32.768 kHz	2	–	4	fF
C_{SHUNT}	Shunt Capacitance	Crystal at 32.768 kHz	0.6	–	2	pF
$C_{CRYSTAL}$	Allowed Crystal Capacitance Load	From crystal specification	6	–	12.5	pF
P_{ON}	Drive Level	–	–	–	0.2	µW

59.4.5 XIN32 Clock Characteristics in Bypass Mode

Table 59-22. XIN32 Clock Characteristics in Bypass Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPXIN})$	XIN32 Clock Frequency	(see **Note**)	–	–	32	kHz
t_{CHXIN}	XIN32 Clock High Half-period	(see **Note**)	15	–	–	ns
t_{CLXIN}	XIN32 Clock Low Half-period	(see **Note**)	15	–	–	ns
V_{XIN_IL}	V_{XIN} Input Low-level Voltage	(see **Note**)	Min of V_{IL} for CLOCK pad	–	Max of V_{IL} for CLOCK pad	V
V_{XIN_IH}	V_{XIN} Input High-level Voltage	(see **Note**)	Min of V_{IH} for CLOCK pad	–	Max of V_{IH} for CLOCK pad	V

Date	Comments
	Corrected CKx typo in Figure 58-36 “SSC Transmitter, TK and TF in Input”.
	Section 59. “Mechanical Characteristics” All sections: Modified JEDEC classification to J-STD-609 from JESD97.
	Section 60. “Schematic Checklist” Added note following Figure 60-4 “Schematic Example with a 16 Mb/16-bit SDRAM (1)”.
cont’d	
01-June-16	Section 62. “Ordering Information” Updated Table 62-1 “Ordering Codes for SAM V71 Devices”.
	Section 63. “Errata” Added - Section 63.1.1 “AFE Controller (AFEC)”: “AFE max sampling frequency is 1.74 Msps” and “Changing AFEC_COCR.AOFF during conversions is not safe” . - Section 63.1.5 “Boundary Scan Mode”: “Boundary Scan Mode” - Section 63.1.8 “Ethernet MAC (GMAC)”: “Error in number of queues” - Section 63.1.10 “Master CAN-FD Controller (MCAN)”: “Timestamping issue with external clock” - Section 63.1.11 “Parallel Input/Output (PIO)”: “PIO line configuration for AFEC and DACC analog inputs” - Section 63.1.12 “Power Management Controller (PMC)”: “PMC_OCR does not report the Main RC oscillator manufacturing calibration value” - Section 63.1.14 “SDRAM Controller (SDRAMC)”: “Limitation to scrambling/unscrambling use” Added Section 63.2 “Revision B Parts”.
End	

Table 62-4. SAM E70/S70/V70/V71 Datasheet Rev. 44003C – Revision History

Date	Changes
08-Feb-16	Added TFBGA144 package to features, configuration summary, package and pinout, mechanical drawings, ordering information and AMR.
	Deleted LFBGA144 package from features, configuration summary, package and pinout, mechanical drawings, ordering information and AMR.
	Deleted TFBGA64 package from features, configuration summary, package and pinout, mechanical drawings, ordering information and AMR.
	Deleted QFN64 package from features, configuration summary, package and pinout, mechanical drawings, ordering information and AMR.