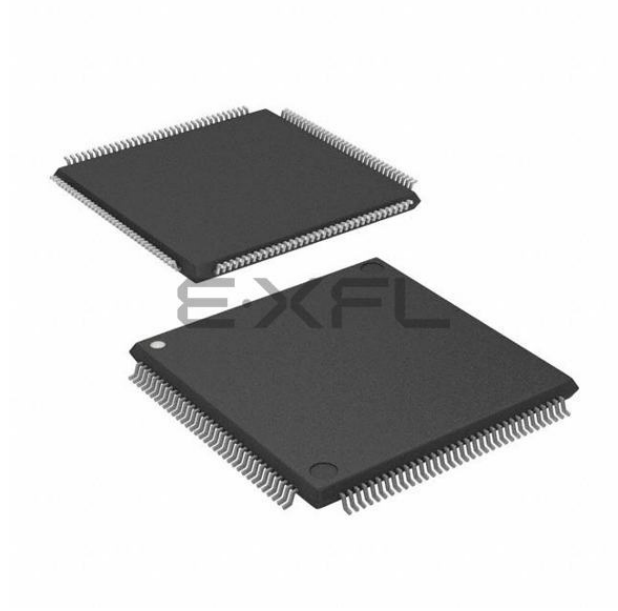

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	1.08V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsams70q21b-ant

Figure 3-2. SAM E70 144-pin Block Diagram

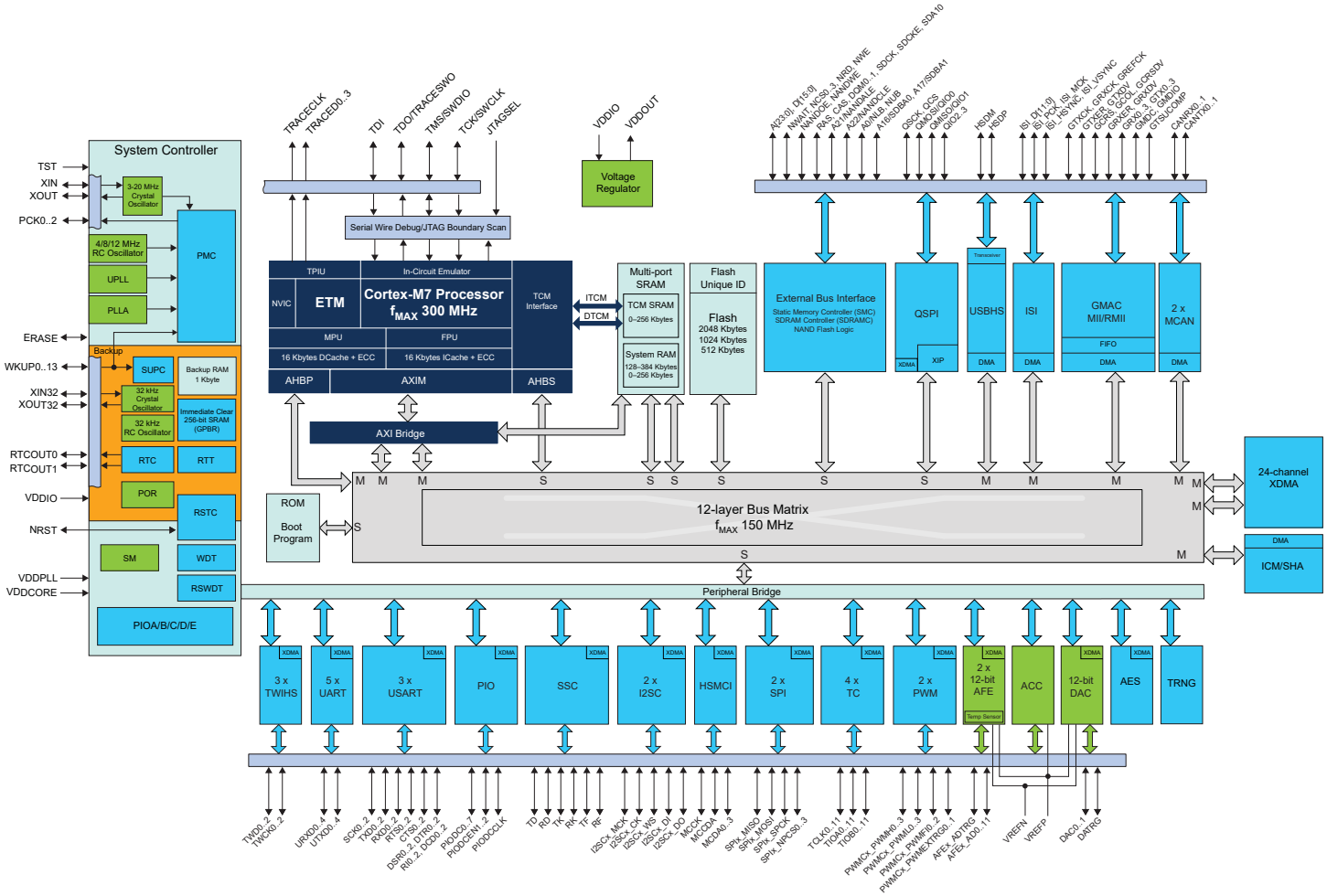


Table 8-1. System I/O Configuration Pin List

CCFG_SYSIO Bit Number	Default Function After Reset	Other Function	Constraints for Normal Start	Configuration
12	ERASE	PB12	Low Level at startup (see **Note 1**)	In Matrix User Interface Registers (Refer to the 19.4.7 CCFG_SYSIO register)
7	TCK/SWCLK	PB7	–	
6	TMS/SWDIO	PB6	–	
5	TDO/ TRACESWO	PB5	–	
4	TDI	PB4	–	
–	PA7	XIN32	–	(see **Note 2**)
–	PA8	XOUT32	–	
–	PB9	XIN	–	(see **Note 3**)
–	PB8	XOUT	–	

Note:

1. If PB12 is used as PIO input in user applications, a low level must be ensured at startup to prevent Flash erase before the user application sets PB12 into PIO mode.
2. Refer to 23.4.2 Slow Clock Generator.
3. Refer to 30.5.3 Main Crystal Oscillator.

8.2.1 Serial Wire Debug Port (SW-DP) Pins

The SW-DP pins SWCLK and SWDIO are commonly provided on a standard 20-pin JTAG connector defined by ARM. For more details about voltage reference and reset state, refer to Table 4-1.

At startup, SW-DP pins are configured in SW-DP mode to allow connection with debugging probe. For more details, refer to 16. Debug and Test Features.

SW-DP pins can be used as standard I/Os to provide users more general input/output pins when the debug port is not needed in the end application. Mode selection between SW-DP mode (System IO mode) and general IO mode is performed through the AHB Matrix Special Function Registers (MATRIX_SFR). Configuration of the pad for pull-up, triggers, debouncing and glitch filters is possible regardless of the mode.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pulldown resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations.

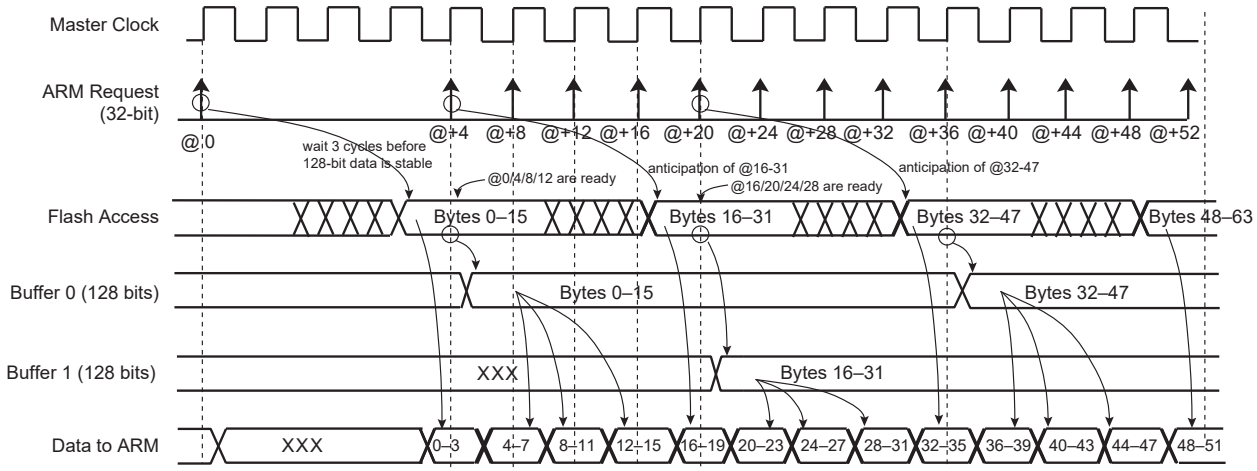
The JTAG Debug Port TDI, TDO, TMS and TCK is inactive. It is provided for Boundary Scan Manufacturing Test purpose only.

8.2.2 Embedded Trace Module (ETM) Pins

The Embedded Trace Module (ETM) depends on the Trace Port Interface Unit (TPIU) to export data out of the system.

The TPUI features the following pins:

Figure 22-4. Code Read Optimization for FWS = 3



Note: When FWS is between 1 and 3, in case of sequential reads, the first access takes (FWS + 1) cycles. The following accesses take only one cycle.

22.4.2.2 Code Loop Optimization

Code loop optimization is enabled when the bit EEFC_FMR.CLOE is set.

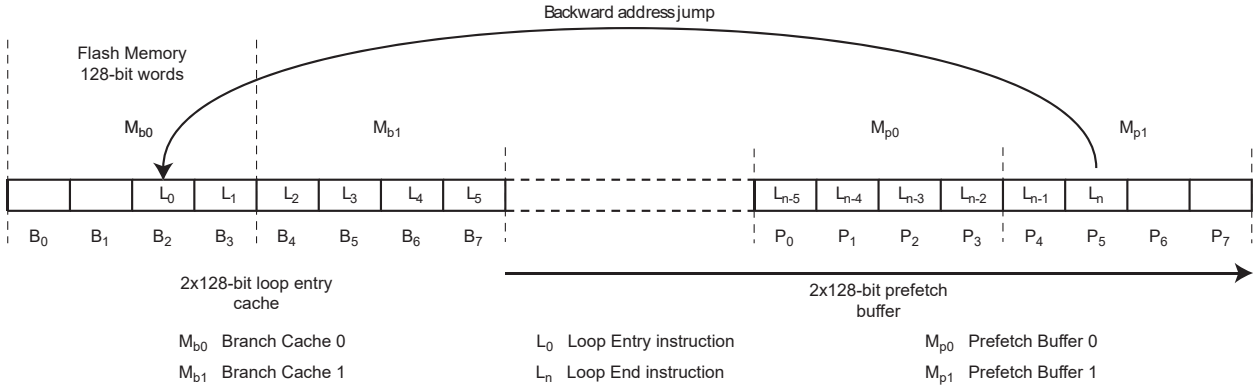
When a backward jump is inserted in the code, the pipeline of the sequential optimization is broken and becomes inefficient. In this case, the loop code read optimization takes over from the sequential code read optimization to prevent the insertion of wait states. The loop code read optimization is enabled by default. In EEFC_FMR, if the bit CLOE is reset to 0 or the bit SCOD is set, these buffers are disabled and the loop code read is not optimized.

When code loop optimization is enabled, if inner loop body instructions L_0 to L_n are positioned from the 128-bit Flash memory cell M_{b0} to the memory cell M_{p1}, after recognition of a first backward branch, the first two Flash memory cells M_{b0} and M_{b1} targeted by this branch are cached for fast access from the processor at the next loop iteration.

Then by combining the sequential prefetch (described in the “Code Read Optimization” section) through the loop body with the fast read access to the loop entry cache, the entire loop can be iterated with no wait state.

The following figure illustrates code loop optimization.

Figure 22-5. Code Loop Optimization



Value	Description
0	The minute-matching alarm is disabled.
1	The minute-matching alarm is enabled.

Bits 14:8 – MIN[6:0] Minute Alarm
This field is the alarm field corresponding to the BCD-coded minute counter.

Bit 7 – SECEN Second Alarm Enable

Value	Description
0	The second-matching alarm is disabled.
1	The second-matching alarm is enabled.

Bits 6:0 – SEC[6:0] Second Alarm
This field is the alarm field corresponding to the BCD-coded second counter.

36.9.14 XDMAC Global Channel Read Write Resume Register

Name: XDMAC_GRWR
Offset: 0x34
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	RWR23	RWR22	RWR21	RWR20	RWR19	RWR18	RWR17	RWR16
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bit	15	14	13	12	11	10	9	8
	RWR15	RWR14	RWR13	RWR12	RWR11	RWR10	RWR9	RWR8
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bit	7	6	5	4	3	2	1	0
	RWR7	RWR6	RWR5	RWR4	RWR3	RWR2	RWR1	RWR0
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 – RWRx XDMAC Channel x Read Write Resume

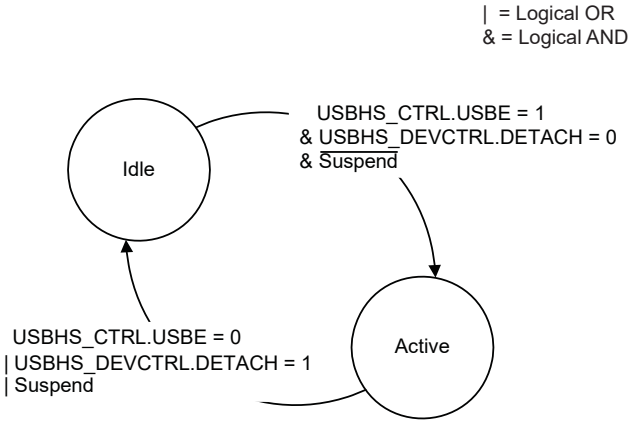
Value	Description
0	No effect.
1	Read and write requests are serviced.

Offset	Name	Bit Pos.								
		23:16								
		31:24								
0x58	ISI_DMA_C_DSCR	7:0	C_DSCR[5:0]							
		15:8	C_DSCR[13:6]							
		23:16	C_DSCR[21:14]							
		31:24	C_DSCR[29:22]							
0x5C ... 0xE3	Reserved									
0xE4	ISI_WPMR	7:0								WPEN
		15:8	WPKEY[7:0]							
		23:16	WPKEY[15:8]							
		31:24	WPKEY[23:16]							
0xE8	ISI_WPSR	7:0								WPVS
		15:8	WPVSRC[7:0]							
		23:16	WPVSRC[15:8]							
		31:24								

39.5.1.6 Pad Suspend

Figure 39-5 shows the pad behavior.

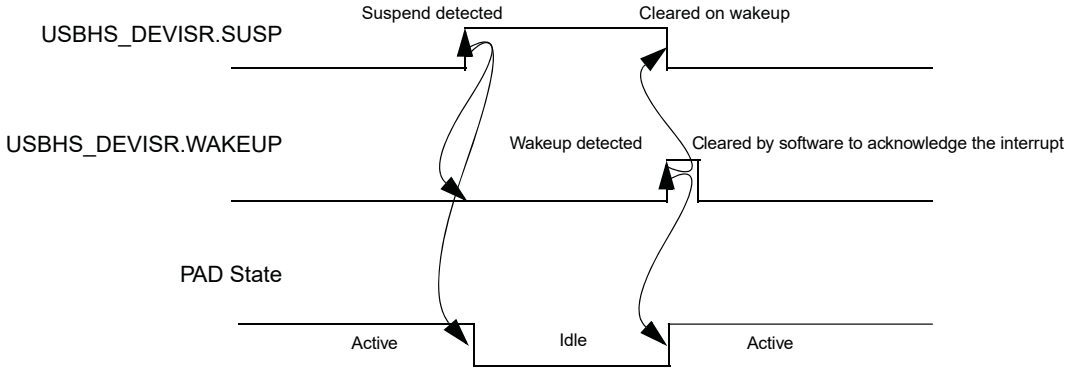
Figure 39-5. Pad Behavior



- In Idle state, the pad is put in Low-power mode, i.e., the differential receiver of the USB pad is off, and internal pull-downs with a strong value (15 K) are set in HSDP/D and HSDM/DM to avoid floating lines.
- In Active state, the pad is working.

Figure 39-6 illustrates the pad events leading to a PAD state change.

Figure 39-6. Pad Events



The USBHS_DEVISR.SUSP bit is set and the Wakeup Interrupt (USBHS_DEVISR.WAKEUP) bit is cleared when a USB “Suspend” state has been detected on the USB bus. This event automatically puts the USB pad in Idle state. The detection of a non-idle event sets USBHS_DEVISR.WAKEUP, clears USBHS_DEVISR.SUSP and wakes up the USB pad.

The pad goes to the Idle state if the USBHS is disabled or if the USBHS_DEVCTRL.DETACH bit = 1. It returns to the Active state when USBHS_CTRL.USBE = 1 and USBHS_DEVCTRL.DETACH = 0.

39.5.2 USB Device Operation

39.5.2.1 Introduction

In Device mode, the USBHS supports high-, full- and low-speed data transfers.

In addition to the default control endpoint, 10 endpoints are provided, which can be configured with an isochronous, bulk or interrupt type, as described in Table 39-1.

As the Device mode starts in Idle state, the pad consumption is reduced to the minimum.

Offset	Name	Bit Pos.								
0x0670	USBHS_HSTPIPINRQ8	7:0	INRQ[7:0]							
		15:8								INMODE
		23:16								
		31:24								
0x0674	USBHS_HSTPIPINRQ9	7:0	INRQ[7:0]							
		15:8								INMODE
		23:16								
		31:24								
0x0678 ... 0x067F	Reserved									
0x0680	USBHS_HSTPIPERR0	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0684	USBHS_HSTPIPERR1	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0688	USBHS_HSTPIPERR2	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x068C	USBHS_HSTPIPERR3	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0690	USBHS_HSTPIPERR4	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0694	USBHS_HSTPIPERR5	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x0698	USBHS_HSTPIPERR6	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x069C	USBHS_HSTPIPERR7	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								
		31:24								
0x06A0	USBHS_HSTPIPERR8	7:0		COUNTER[1:0]		CRC16	TIMEOUT	PID	DATAPID	DATATGL
		15:8								
		23:16								

Value	Description
	• (INRQ+1) in requests have been processed. • A Pipe Reset (USBHS_HSTPIP.PRSTx rising) has occurred. • A Pipe Enable (USBHS_HSTPIP.PEN rising) has occurred.

Bit 16 – PDISHDMA Pipe Interrupts Disable HDMA Request Enable
See the USBHS_DEVEPTIMR.EPDISHDMA bit description.

Bit 14 – FIFOCON FIFO Control
For OUT and SETUP pipes:

0: Cleared when USBHS_HSTPIPIDR.FIFOCONC = 1. This sends the FIFO data and switches the bank.

1: Set when the current bank is free, at the same time as USBHS_HSTPIPISR.TXOUTI or TXSTPI.

For IN pipes:

0: Cleared when USBHS_HSTPIPIDR.FIFOCONC = 1. This frees the current bank and switches to the next bank.

1: Set when a new IN message is stored in the current bank, at the same time as USBHS_HSTPIPISR.RXINI.

Bit 12 – NBUSYBKE Number of Busy Banks Interrupt Enable

Value	Description
0	Cleared when USBHS_HSTPIPIDR.NBUSYBKEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.NBUSYBKE).
1	Set when USBHS_HSTPIPIER.NBUSYBKES = 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.NBUSYBKE).

Bit 7 – SHORTPACKETIE Short Packet Interrupt Enable
If this bit is set for non-control OUT pipes, a short packet transmission is guaranteed upon ending a DMA transfer, thus signaling an end of transfer, provided that the End of DMA Buffer Output Enable (USBHS_HSTDMACONTROL.END_B_EN) bit and the Automatic Switch (USBHS_HSTPIPCFG.AUTOSW) bit = 1.

Value	Description
0	Cleared when USBHS_HSTPIPIDR.SHORTPACKETEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.SHORTPACKETE).
1	Set when USBHS_HSTPIPIER.SHORTPACKETIES = 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.SHORTPACKETIE).

Bit 6 – RXSTALLDE Received STALLed Interrupt Enable

Value	Description
0	Cleared when USBHS_HSTPIPIDR.RXSTALLDEC = 1. This disables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.RXSTALLDE).
1	Set when USBHS_HSTPIPIER.RXSTALLDES= 1. This enables the Transmitted IN Data interrupt (USBHS_HSTPIPIMR.RXSTALLDE).

Bit 5 – OVERFIE Overflow Interrupt Enable

41.5 Signal Description

Table 41-1. Signal Description

Pin Name	Pin Description	Type	
		Master	Slave
MISO	Master In Slave Out	Input	Output
MOSI	Master Out Slave In	Output	Input
SPCK	Serial Clock	Output	Input
NPCS1–NPCS3	Peripheral Chip Selects	Output	Unused
NPCS0/NSS	Peripheral Chip Select/Slave Select	Output	Input

41.6 Product Dependencies

41.6.1 I/O Lines

The pins used for interfacing the compliant external devices can be multiplexed with PIO lines. The programmer must first program the PIO controllers to assign the SPI pins to their peripheral functions.

41.6.2 Power Management

The SPI can be clocked through the Power Management Controller (PMC), thus the programmer must first configure the PMC to enable the SPI clock.

41.6.3 Interrupt

The SPI interface has an interrupt line connected to the interrupt controller. Handling the SPI interrupt requires programming the interrupt controller before configuring the SPI.

41.6.4 Direct Memory Access Controller (DMAC)

The SPI interface can be used in conjunction with the DMAC in order to reduce processor overhead. For a full description of the DMAC, refer to the relevant section.

41.7 Functional Description

41.7.1 Modes of Operation

The SPI operates in Master mode or in Slave mode.

- The SPI operates in Master mode by setting the MSTR bit in the SPI Mode Register (SPI_MR):
  - Pins NPCS0 to NPCS3 are all configured as outputs
  - The SPCK pin is driven
  - The MISO line is wired on the receiver input
  - The MOSI line is driven as an output by the transmitter.
- The SPI operates in Slave mode if the MSTR bit in SPI_MR is written to ‘0’:
  - The MISO line is driven by the transmitter output
  - The MOSI line is wired on the receiver input

45.8.5 I2SC Status Set Register

Name: I2SC_SSR
Offset: 0x10
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			TXURCH[1:0]					
Access			W	W				
Reset			–	–				

Bit	15	14	13	12	11	10	9	8
							RXORCH[1:0]	
Access							W	W
Reset							–	–

Bit	7	6	5	4	3	2	1	0
		TXUR				RXOR		
Access		W				W		
Reset		–				–		

Bits 21:20 – TXURCH[1:0] Transmit Underrun Per Channel Status Set
Writing a ’0’ has no effect.

Writing a ’1’ to any bit in this field sets the corresponding bit in I2SC_SR and the corresponding interrupt request.

Bits 9:8 – RXORCH[1:0] Receive Overrun Per Channel Status Set
Writing a ’0’ has no effect.

Writing a ’1’ to any bit in this field sets the corresponding bit in I2SC_SR and the corresponding interrupt request.

Bit 6 – TXUR Transmit Underrun Status Set
Writing a ’0’ to this bit has no effect.

Writing a ’1’ to this bit sets the status bit.

Bit 2 – RXOR Receive Overrun Status Set
Writing a ’0’ to this bit has no effect.

Writing a ’1’ to this bit sets the status bit.

If a write access to a write-protected register is detected, the WPVS flag in the USART Write Protection Status Register (US_WPSR) is set and the field WPVSRC indicates the register in which the write access has been attempted.

The WPVS bit is automatically cleared after reading the US_WPSR.

The following registers can be write-protected:

- USART Mode Register
- USART Baud Rate Generator Register
- USART Receiver Timeout Register
- USART Transmitter Timeguard Register
- USART Manchester Configuration Register
- USART LON Mode Register
- USART LON Beta1 Tx Register
- USART LON Beta1 Rx Register
- USART LON Priority Register
- USART LON IDT Tx Register
- USART LON IDT Rx Register
- USART IC DIFF Register

A byte-wide value sent by the receiving (Rx) MediaLB Device on the MLBS line, after Command is sent. This status response provides a hardware handshaking mechanism and signals other control information, such as transmission errors, back to the sender.

- Data:

The physical channel contains Data and is sent by the Tx MediaLB Device during the same physical channel in which Command is sent. This physical channel data must be transmitted left-justified, MSB first, most significant byte first. Note the Rx Device might return a status of busy, wherein the Tx Device must retransmit the same data in the next physical channel associated with the logical channel.

To dynamically configure ChannelAddresses for logical channels, a DeviceAddress can be pre-defined for MediaLB Devices. The DeviceAddress is a 16-bit address used in the System Channel with the MLBScan command to detect which MediaLB Devices exist.

48.6.1.1 Channel Addresses

A MediaLB logical channel is defined as all physical channels associated with a single ChannelAddress. A logical channel on MediaLB is unidirectional; therefore, a single MediaLB Device sends data on a logical channel to one or more receiving Devices. If two Devices require bidirectional communication, then two MediaLB logical channels are required.

A ChannelAddress is 16-bits wide. Of the 16-bits, ChannelAddress (CA) bits 15 through 9 and the LSB are always zero. Only the eight bits CA[8:1] vary. A delay of one physical channel exists between the occurrence of the ChannelAddress and the actual physical channel granted. The 0x01FE ChannelAddress is defined as the FRAMESYNC pattern, where the end of the pattern determines the byte boundary, the physical channel boundary, and indicates that the MediaLB frame starts one physical channel later (PC0). The 0x0000 ChannelAddress is defined as the BusIdle state, which indicates that the corresponding physical channel is not assigned and not used by any Device. All odd ChannelAddresses are reserved; therefore, the LSB of a valid ChannelAddress is always zero. The MLBS line is in a consistent known state when not driven by any Device. For 3-pin MediaLB, this is achieved with the required weak pull-down.

Table 48-3. MediaLB ChannelAddresses

ChannelAddress (1)	Description
0x0000	BusIdle - Indicates that the physical channel is not being used, not assigned.
0x0002..0x007E	63 ChannelAddresses - defines the logical channels used in normal operation (3-pin MediaLB)
0x0080..0x01FC	Reserved
0x01FE	FRAMESYNC - MediaLB frame alignment and System Channel ChannelAddress
0x0200..0xFFFF	Reserved

Note: 1. All odd ChannelAddresses are reserved (LSB must be zero for valid ChannelAddresses).

48.6.1.2 Device Addresses

DeviceAddresses are 16-bits wide, must be pre-assigned, and must be unique for each MediaLB Device. Of the 16-bits, DeviceAddress (DA) bits 15 through 9 and the LSB are always zero. Only the eight bits DA[8:1] vary. At the request of the EHC, DeviceAddresses can be scanned for by the MediaLB Controller to dynamically determine which Devices exist on MediaLB. DeviceAddresses are only used with the MLBScan command in the System Channel and are never assigned to physical channels. Once a Device is found, the ChannelAddresses used in normal operation can be assigned.

49.6.29 MCAN Receive FIFO 0 Acknowledge

Name: MCAN_RXF0A
Offset: 0xA8
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			F0AI[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:0 – F0AI[5:0] Receive FIFO 0 Acknowledge Index
After the processor has read a message or a sequence of messages from Receive FIFO 0 it has to write the buffer index of the last element read from Receive FIFO 0 to F0AI. This will set the Receive FIFO 0 Get Index MCAN_RXF0S.F0GI to F0AI + 1 and update the FIFO 0 Fill Level MCAN_RXF0S.F0FL.

49.6.46 MCAN Tx Event FIFO Status

Name: MCAN_TXEFS
Offset: 0xF4
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
							TEFL	EFF
Access							R	R
Reset							0	0

Bit	23	22	21	20	19	18	17	16
				EFPI[4:0]				
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				EFGI[4:0]				
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			EFFL[5:0]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit 25 – TEFL Tx Event FIFO Element Lost
This bit is a copy of interrupt flag MCAN_IR.TEFL. When MCAN_IR.TEFL is reset, this bit is also reset.

Value	Description
0	No Tx Event FIFO element lost.
1	Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero.

Bit 24 – EFF Event FIFO Full

Value	Description
0	Tx Event FIFO not full.
1	Tx Event FIFO full.

Bits 20:16 – EFPI[4:0] Event FIFO Put Index
Tx Event FIFO write index pointer, range 0 to 31.

Bits 12:8 – EFGI[4:0] Event FIFO Get Index
Tx Event FIFO read index pointer, range 0 to 31.

Bits 5:0 – EFFL[5:0] Event FIFO Fill Level
Number of elements stored in Tx Event FIFO, range 0 to 32.

Table 50-2. Channel Signal Description

Signal Name	Description
XC0, XC1, XC2	External Clock Inputs
TIOAx	Capture Mode: Timer Counter Input Waveform Mode: Timer Counter Output
TIOBx	Capture Mode: Timer Counter Input Waveform Mode: Timer Counter Input/Output
INT	Interrupt Signal Output (internal signal)
SYNC	Synchronization Input Signal (from configuration register)

50.4 Pin List

Table 50-3. Pin List

Pin Name	Description	Type
TCLK0–TCLK2	External Clock Input	Input
TIOA0–TIOA2	I/O Line A	I/O
TIOB0–TIOB2	I/O Line B	I/O

50.5 Product Dependencies

50.5.1 I/O Lines

The pins used for interfacing the compliant external devices may be multiplexed with PIO lines. The programmer must first program the PIO controllers to assign the TC pins to their peripheral functions.

50.5.2 Power Management

The TC is clocked through the Power Management Controller (PMC), thus the programmer must first configure the PMC to enable the Timer Counter clock of each channel.

50.5.3 Interrupt Sources

The TC has an interrupt line per channel connected to the interrupt controller. Handling the TC interrupt requires programming the interrupt controller before configuring the TC.

50.5.4 Synchronization Inputs from PWM

The TC has trigger/capture inputs internally connected to the PWM. Refer to “Synchronization with PWM” and to the implementation of the Pulse Width Modulation (PWM) in this product.

50.5.5 Fault Output

The TC has the FAULT output internally connected to the fault input of PWM. Refer to “Fault Mode” and to the implementation of the Pulse Width Modulation (PWM) in this product.

– By using the PWM peripheral clock divided by a given prescaler value “X” (where X = 2^{PREA} is 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, or 1024). The resulting period formula is:

$$\frac{(2 \times X \times \mathrm{CPRD})}{f_{\mathrm{peripheral\ clock}}}$$

– By using the PWM peripheral clock divided by a given prescaler value “X” (see above) and by either the DIVA or the DIVB divider. The formula becomes, respectively:

$$\frac{(2 \times X \times \mathrm{CPRD} \times \mathrm{DIVA})}{f_{\mathrm{peripheral\ clock}}} \text{ or } \frac{(2 \times X \times \mathrm{CPRD} \times \mathrm{DIVB})}{f_{\mathrm{peripheral\ clock}}}$$

52.7.15 AFEC Compare Window Register

Name: AFEC_CWR
Offset: 0x50
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the AFEC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	HIGHTHRES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	HIGHTHRES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	LOWTHRES[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LOWTHRES[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:16 – HIGHTHRES[15:0] High Threshold
High threshold associated to compare settings of AFEC_EMR. For comparisons lower than 16 bits and signed, the sign should be extended up to the bit 15.

Bits 15:0 – LOWTHRES[15:0] Low Threshold
Low threshold associated to compare settings of AFEC_EMR. For comparisons lower than 16 bits and signed, the sign should be extended up to the bit 15.

53. Digital-to-Analog Converter Controller (DACC)

53.1 Description

The Digital-to-Analog Converter Controller (DACC) offers up to two single-ended analog outputs or one differential analog output, making it possible for the digital-to-analog conversion to drive up to two independent analog lines.

The DACC supports 12-bit resolution.

The DACC operates in Free-running mode, Max speed mode, Trigger mode or Interpolation mode.

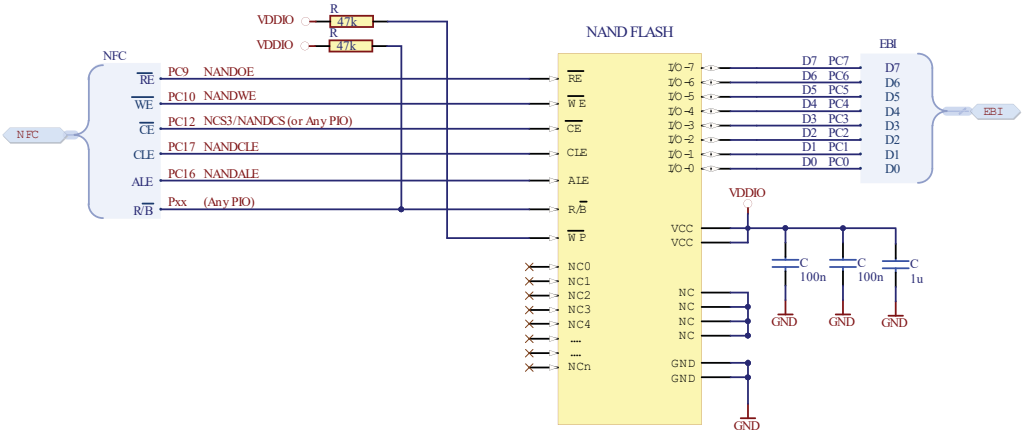
The DACC integrates a Bypass mode which minimizes power consumption in case of a limited sampling rate conversion.

Each channel connects with a separate DMA channel. This feature reduces both power consumption and processor intervention.

53.2 Embedded Characteristics

- Up to Two Independent Single-Ended Analog Outputs or One Differential Analog Output
- 12-bit Resolution
- Integrated Interpolation Filter with 2×, 4×, 8×, 16× or 32× Oversampling Ratio (OSR)
- Reduced Number of System Bus Accesses (Word Transfer Mode)
- Individual Control of Each Analog Channel
- Hardware Triggers
  - One Trigger Selection Per Channel
    – External trigger pin
    – Internal events
- DMA Support
- One Internal FIFO per Channel
- Register Write Protection

Figure 60-5. Schematic Example with a 2 Gb/8-bit NAND Flash

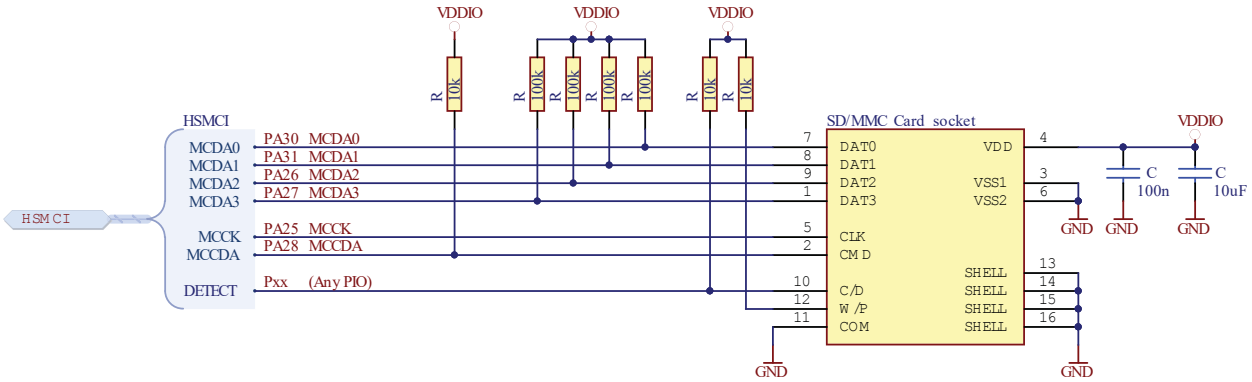


Note: For more details on the pin configuration of the EBI, refer to Table 33-3.

60.2.10 High-Speed Multimedia Card Interface (HSMCI)

Signal Name	Recommended Pin Connection	Description
MCCK	Application dependent	Multimedia Card Clock Pulled-up input (100 kOhm) to VDDIO at reset.
MCCDA	Application dependent (Pullup at VDDIO)	Multimedia Card Slot A Command Pulled-up input (100 kOhm) to VDDIO at reset.
MCDA0–MCDA3	Application dependent (Pullup at VDDIO)	Multimedia Card Slot A Data Pulled-up inputs (100 kOhm) to VDDIO at reset.

Figure 60-6. Schematic Example with SD/MMC Card Interface



60.2.11 QSPI Interface

Signal Name	Recommended Pin Connection	Description
QSCK	Application dependent.	QSPI Serial Clock Pulled-up input (100 kOhm) to VDDIO at reset.
QCS	Application dependent.	QSPI Chip Select