Microchip Technology - ATSAMV70N20B-AAB Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv70n20b-aab

19.4.8 Peripheral Clock Configuration Register

Name: CCFG_PCCR
Offset: 0x0118
Reset: 0x00022224
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		I2SC1CC	I2SC0CC	TC0CC				
Access								
Reset		0	0	0				

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								
Reset								

Bit 22 – I2SC1CC I2SC1 Clock Configuration

Value	Description
0	Peripheral clock of I2SC1 is used.
1	GCLK is used.

Bit 21 – I2SC0CC I2SC0 Clock Configuration

Value	Description
0	Peripheral clock of I2SC0 is used.
1	GCLK is used.

Bit 20 – TC0CC TC0 Clock Configuration

Value	Description
0	PCK6 is used (default).
1	PCK7 is used.

Bit 1 – ALRDIS Alarm Interrupt Disable

Value	Description
0	No effect.
1	The alarm interrupt is disabled.

Bit 0 – ACKDIS Acknowledge Update Interrupt Disable

Value	Description
0	No effect.
1	The acknowledge for update interrupt is disabled.

Value	Description
0	No clock failure detection of the Main crystal oscillator clock has occurred since the last read of PMC_SR.
1	At least one clock failure detection of the Main crystal oscillator clock has occurred since the last read of PMC_SR.

Bit 17 – MOSCRCS Main RC Oscillator Status

Value	Description
0	Main RC oscillator is not stabilized.
1	Main RC oscillator is stabilized.

Bit 16 – MOSCSELS Main Clock Source Oscillator Selection Status

Value	Description
0	Selection is in progress.
1	Selection is done.

Bits 8, 9, 10, 11, 12, 13, 14 – PCKRDY Programmable Clock Ready Status

Value	Description
0	Programmable Clock x is not ready.
1	Programmable Clock x is ready.

Bit 7 – OSCSELS Slow Clock Source Oscillator Selection

Value	Description
0	Slow RC oscillator is selected.
1	32.768 kHz crystal oscillator is selected.

Bit 6 – LOCKU UTMI PLL Lock Status

Value	Description
0	UTMI PLL is not locked
1	UTMI PLL is locked.

Bit 3 – MCKRDY Master Clock Status

Value	Description
0	Master Clock is not ready.
1	Master Clock is ready.

Bit 1 – LOCKA PLLA Lock Status

Value	Description
0	PLLA is not locked
1	PLLA is locked.

Bit 0 – MOSCXTS Main Crystal Oscillator Status

– Can Be Used to Interface a CMOS Digital Image Sensor, an ADC, etc.
– One Clock, 8-bit Parallel Data and Two Data Enable on I/O Lines
– Data Can be Sampled Every Other Time (For Chrominance Sampling Only)
– Supports Connection of One DMA Controller Channel Which Offers Buffer Reception Without Processor Intervention

32.3 Block Diagram

Figure 32-1. Block Diagram

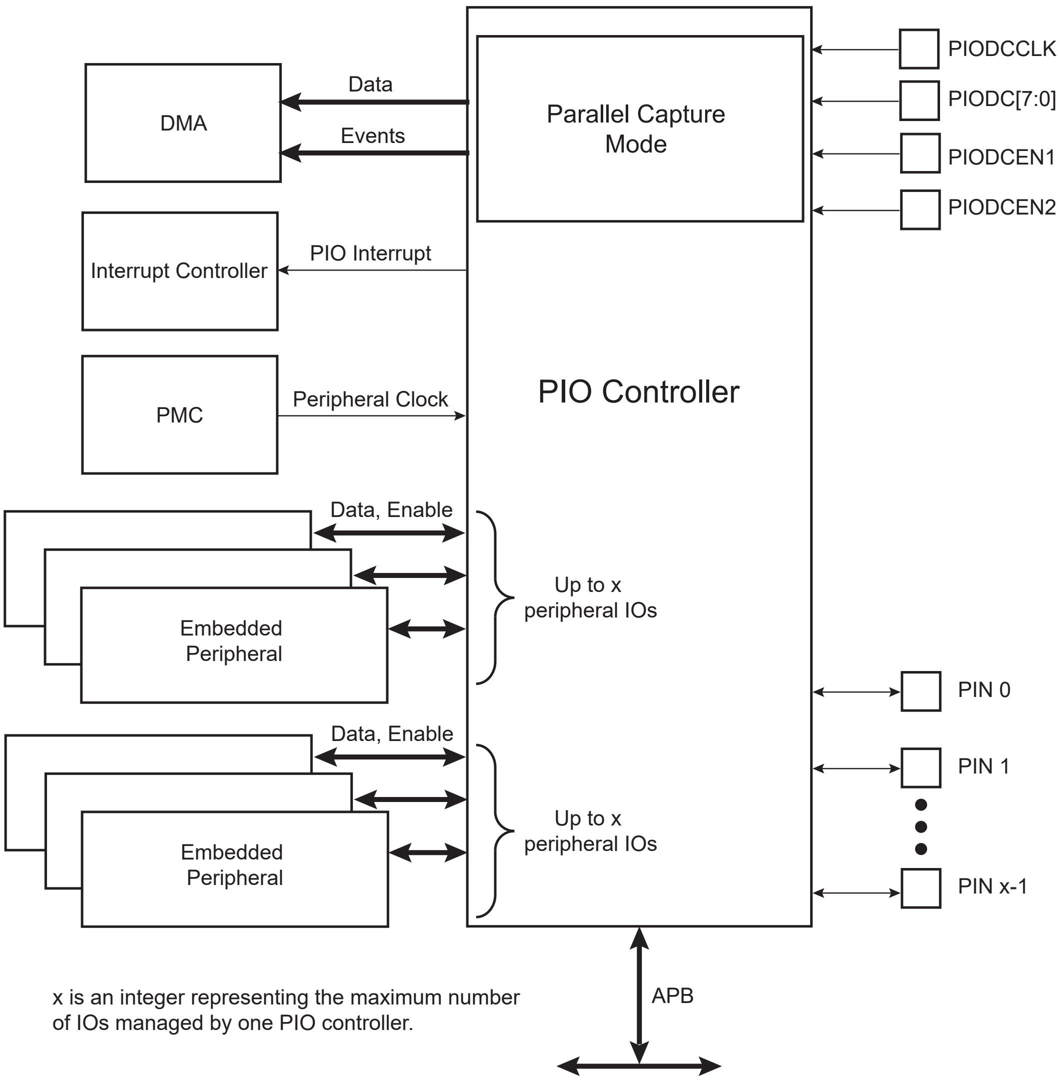
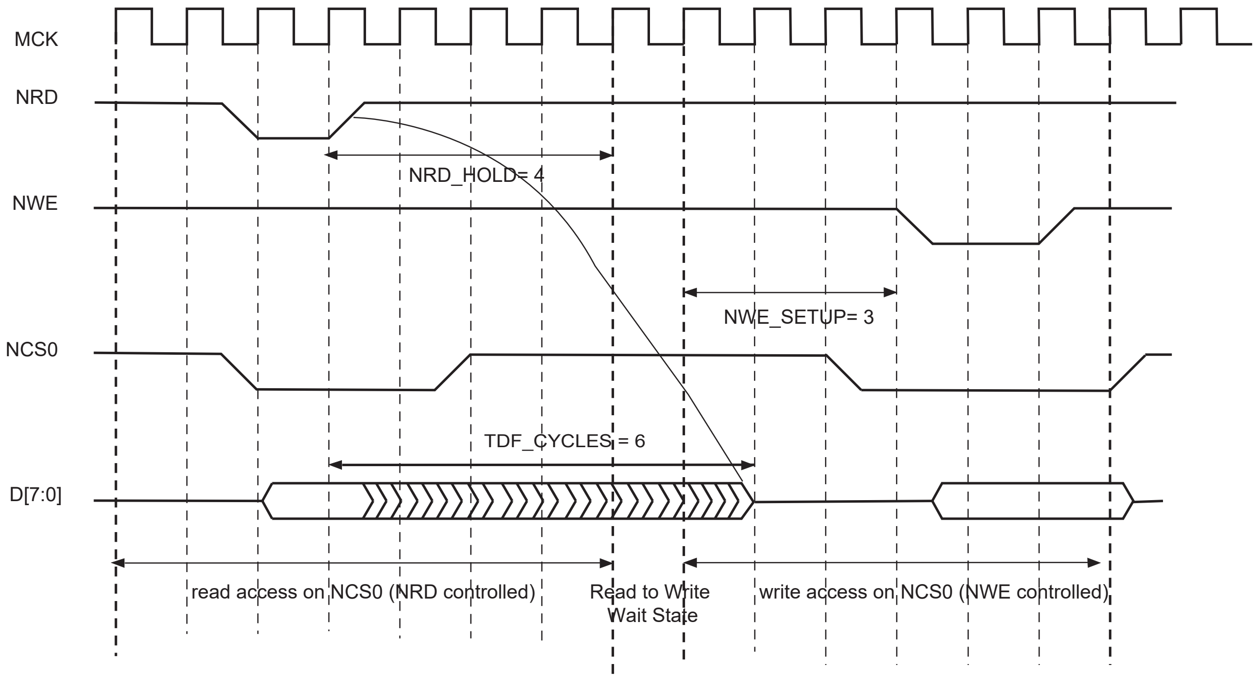


Table 32-1. Signal Description

Signal Name	Signal Description	Signal Type
PIODCCLK	Parallel Capture Mode Clock	Input
PIODC[7:0]	Parallel Capture Mode Data	Input

Figure 35-23. TDF Optimization: No TDF wait states are inserted if the TDF period is over when the next access begins



35.12.3 TDF Optimization Disabled (SMC_MODE.TDF_MODE = 0)

When optimization is disabled, TDF Wait states are inserted at the end of the read transfer, so that the data float period is ended when the second access begins. If the hold period of the read1 controlling signal overlaps the data float period, no additional TDF Wait states will be inserted.

Figure 35-24, Figure 35-25 and Figure 35-26 illustrate the cases:

- read access followed by a read access on another Chip Select,
- read access followed by a write access on another Chip Select,
- read access followed by a write access on the same Chip Select,

with no TDF optimization.

Offset	Name	Bit Pos.								
		23:16	ADDR[23:16]							
		31:24	ADDR[31:24]							
0x8C	GMAC_SAT1	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16								
		31:24								
0x90	GMAC_SAB2	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16	ADDR[23:16]							
		31:24	ADDR[31:24]							
0x94	GMAC_SAT2	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16								
		31:24								
0x98	GMAC_SAB3	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16	ADDR[23:16]							
		31:24	ADDR[31:24]							
0x9C	GMAC_SAT3	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16								
		31:24								
0xA0	GMAC_SAB4	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16	ADDR[23:16]							
		31:24	ADDR[31:24]							
0xA4	GMAC_SAT4	7:0	ADDR[7:0]							
		15:8	ADDR[15:8]							
		23:16								
		31:24								
0xA8	GMAC_TIDM1	7:0	TID[7:0]							
		15:8	TID[15:8]							
		23:16								
		31:24	ENIDn							
0xAC	GMAC_TIDM2	7:0	TID[7:0]							
		15:8	TID[15:8]							
		23:16								
		31:24	ENIDn							
0xB0	GMAC_TIDM3	7:0	TID[7:0]							
		15:8	TID[15:8]							
		23:16								
		31:24	ENIDn							
0xB4	GMAC_TIDM4	7:0	TID[7:0]							
		15:8	TID[15:8]							
		23:16								
		31:24	ENIDn							

Bit 5 – EORSM End of Resume Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.EORSMC bit is written to one to acknowledge the interrupt.
1	Set when the USBHS detects a valid “End of Resume” signal initiated by the host. This triggers a USB interrupt if USBHS_DEVIMR.EORSME = 1.

Bit 4 – WAKEUP Wakeup Interrupt
This interrupt is generated even if the clock is frozen by the USBHS_CTRL.FRZCLK bit.

Value	Description
0	Cleared when the USBHS_DEVICR.WAKEUPC bit is written to one to acknowledge the interrupt (USB clock inputs must be enabled before), or when the Suspend (SUSP) interrupt bit is set.
1	Set when the USBHS is reactivated by a filtered non-idle signal from the lines (not by an upstream resume). This triggers an interrupt if USBHS_DEVIMR.WAKEUPE = 1.

Bit 3 – EORST End of Reset Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.EORSTC bit is written to one to acknowledge the interrupt.
1	Set when a USB “End of Reset” has been detected. This triggers a USB interrupt if USBHS_DEVIMR.EORSTE = 1.

Bit 2 – SOF Start of Frame Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.SOFC bit is written to one to acknowledge the interrupt.
1	Set when a USB “Start of Frame” PID (SOF) has been detected (every 1 ms). This triggers a USB interrupt if SOFE = 1. The FNUM field is updated. In High-speed mode, the MFNUM field is cleared.

Bit 1 – MSOF Micro Start of Frame Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.MSOFC bit is written to one to acknowledge the interrupt.
1	Set in High-speed mode when a USB “Micro Start of Frame” PID (SOF) has been detected (every 125 μs). This triggers a USB interrupt if MSOFE = 1. The MFNUM field is updated. The FNUM field is unchanged.

Bit 0 – SUSP Suspend Interrupt

Value	Description
0	Cleared when the USBHS_DEVICR.SUSPC bit is written to one to acknowledge the interrupt, or when the Wakeup (WAKEUP) interrupt bit is set.
1	Set when a USB “Suspend” idle bus state has been detected for 3 frame periods (J state for 3 ms). This triggers a USB interrupt if USBHS_DEVIMR.SUSPE = 1.

Bit 1 – RXOUTIC Received OUT Data Interrupt Clear

Bit 0 – TXINIC Transmitted IN Data Interrupt Clear

39.6.24 Device Endpoint Interrupt Disable Register (Isochronous Endpoints)

Name: USBHS_DEVEPTIDRx (ISOENPT)
Offset: 0x0220 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

This register view is relevant only if EPTYPE = 0x1 in "Device Endpoint x Configuration Register".

For additional information, see "Device Endpoint x Mask Register (Isochronous Endpoints)".

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Clears the corresponding bit in USBHS_DEVEPTIMRx.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
								EPDISHDMAC
Access								
Reset								0

Bit	15	14	13	12	11	10	9	8
		FIFOCONC		NBUSYBKEC		ERRORTRANSEC	DATAXEC	MDATEC
Access								
Reset		0		0		0	0	0

Bit	7	6	5	4	3	2	1	0
	SHORTPACKETEC	CRCERREC	OVERFEC	HBISOFLUSHEC	HBISOINERREC	UNDERFEC	RXOUTEC	TXINEC
Access								
Reset	0	0	0	0	0	0	0	0

Bit 16 – EPDISHDMAC Endpoint Interrupts Disable HDMA Request Clear

Bit 14 – FIFOCONC FIFO Control Clear

Bit 12 – NBUSYBKEC Number of Busy Banks Interrupt Clear

Bit 10 – ERRORTRANSEC Transaction Error Interrupt Clear

Bit 9 – DATAXEC DataX Interrupt Clear

Bit 8 – MDATEC MData Interrupt Clear

39.6.39 Host Address 1 Register

Name: USBHS_HSTADDR1
Offset: 0x0424
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
		HSTADDRP3[6:0]						
Access								
Reset		0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
		HSTADDRP2[6:0]						
Access								
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
		HSTADDRP1[6:0]						
Access								
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		HSTADDRP0[6:0]						
Access								
Reset		0	0	0	0	0	0	0

Bits 30:24 – HSTADDRP3[6:0] USB Host Address
This field contains the address of the Pipe3 of the USB device.

This field is cleared when a USB reset is requested.

Bits 22:16 – HSTADDRP2[6:0] USB Host Address
This field contains the address of the Pipe2 of the USB device.

This field is cleared when a USB reset is requested.

Bits 14:8 – HSTADDRP1[6:0] USB Host Address
This field contains the address of the Pipe1 of the USB device.

This field is cleared when a USB reset is requested.

Bits 6:0 – HSTADDRP0[6:0] USB Host Address
This field contains the address of the Pipe0 of the USB device.

This field is cleared when a USB reset is requested.

Bit 5 – OVERFIES Overflow Interrupt Enable

Bit 4 – NAKEDES NAKed Interrupt Enable

Bit 3 – PERRES Pipe Error Interrupt Enable

Bit 2 – UNDERFIES Underflow Interrupt Enable

Bit 1 – TXOUTES Transmitted OUT Data Interrupt Enable

Bit 0 – RXINES Received IN Data Interrupt Enable

One physical channel after the ChannelAddress is sent on MLBS, the transmitting MediaLB Device associated with that ChannelAddress outputs a command byte (Command) on MLBS and respective data (Data) on MLBD, concurrently. The Command byte contains information about the data simultaneously being transmitted. The MediaLB Device receiving the data outputs a status byte (RxStatus) on MLBS after the transmitting Device sends the Command byte. This status response can indicate that the Device is ready to receive the data, or that the receiving Device is busy (e.g. cannot receive the data at present). Since synchronous stream data is sent in a broadcast fashion, Devices receiving synchronous data can never return a busy status response. In this situation, the RxStatus byte must not be actively driven onto the MLBS line by Devices receiving synchronous data.

The ChannelAddresses output by the Controller for each logical channel are used in normal data transport and can be statically or dynamically assigned. To support dynamic configuration of MediaLB Devices, a unique DeviceAddress must be assigned to all MediaLB Devices before startup. DeviceAddresses allow the External Host Controller (EHC) and MediaLB Controller to dynamically determine which Devices exist on the bus. At the request of a MediaLB Device (e.g. EHC), the Controller scans for DeviceAddresses in the System Channel. Once a Device is detected, a ChannelAddress for each logical channel can be assigned.

The DeviceAddress, ChannelAddress, Command, and RxStatus structures are described in the Link Layer section.

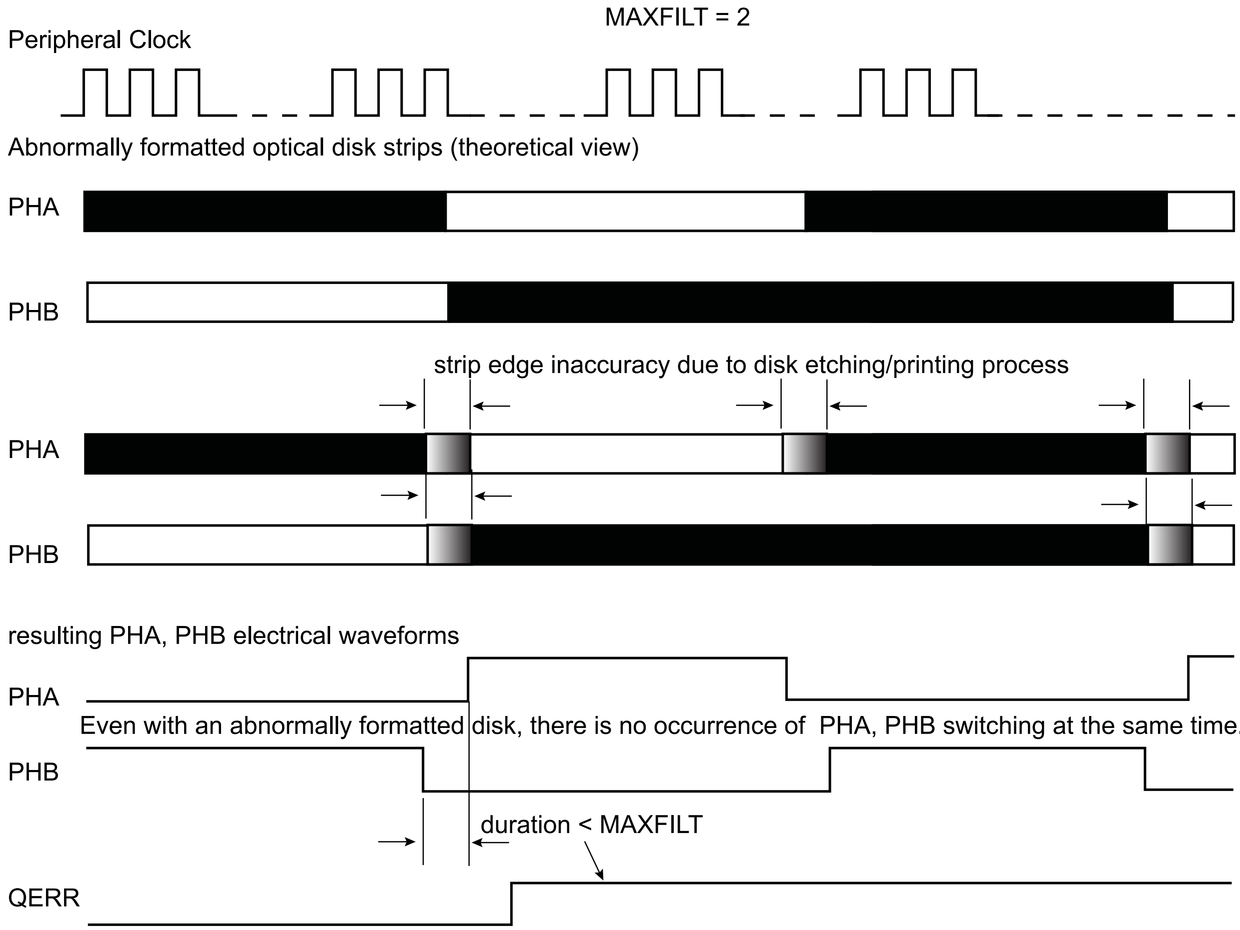
48.2 Embedded Characteristics

- Support of all MOST data transport methods: synchronous stream data, asynchronous packet data, control message data, and isochronous data
- Multiple clock rates supported
- Scalable data rate for all MOST Network data transport methods
- A frame synchronization pattern (FRAMESYNC) enables easy Device synchronization to MOST Networks
- Dedicated system-broadcast channel for administration
- Support of MediaLB Controller to MediaLB Device transfers and inter-MediaLB Devices transfers
- Broadcast support from one transmitter to multiple receivers for synchronous stream data

48.3 Block Diagram

The following figure is the top-level block diagram of the MLB behavioral models.

Figure 50-21. Quadrature Error Detection



MAXFILT must be tuned according to several factors such as the peripheral clock frequency, type of rotary sensor and rotation speed to be achieved.

50.6.16.4 Position and Rotation Measurement

When TC_BMR.POSEN is set, the motor axis position is processed on channel 0 (by means of the PHA, PHB edge detections) and the number of motor revolutions are recorded on channel 1 if the IDX signal is provided on the TIOB1 input. If no IDX signal is available, the internal counter can be cleared for each revolution if the number of counts per revolution is configured in TC_RC0.RC and the TC_CMR.CPCTRG bit is written to '1'. The position measurement can be read in the TC_CV0 register and the rotation measurement can be read in the TC_CV1 register.

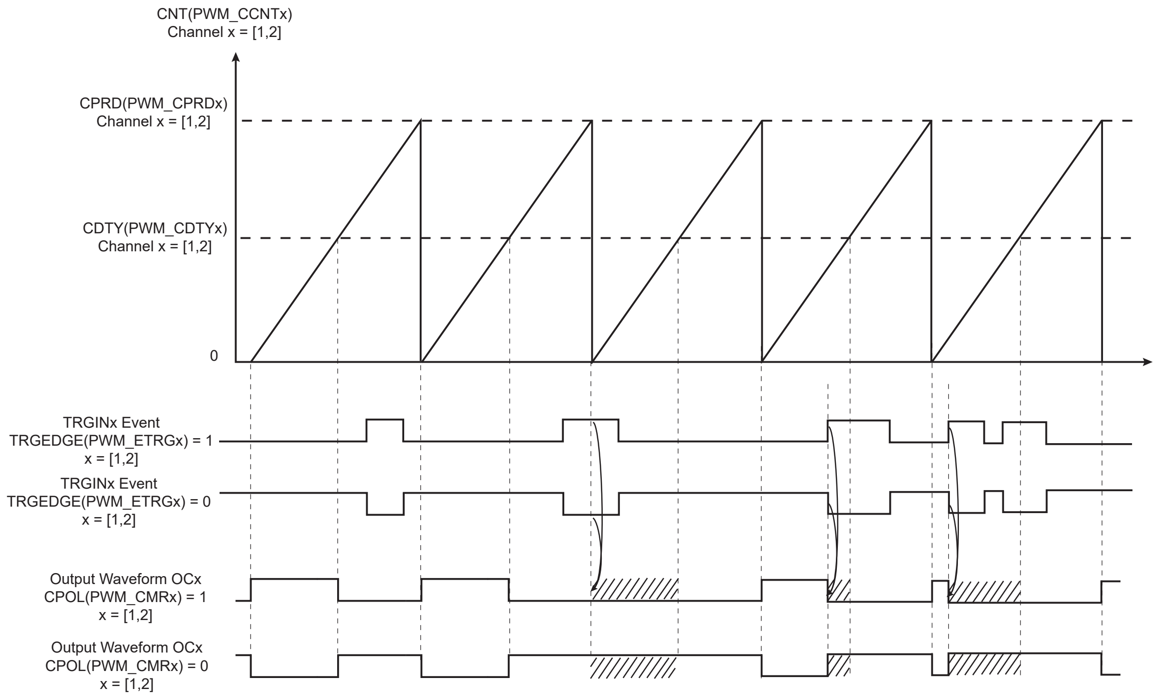
Channel 0 and 1 must be configured in Capture mode (TC_CMR0.WAVE = 0). 'Rising edge' must be selected as the External Trigger Edge (TC_CMR.ETRGEDG = 0x01) and 'TIOAx' must be selected as the External Trigger (TC_CMR.ABETRG = 0x1). The process must be started by configuring TC_CCR.CLKEN and TC_CCR.SWTRG.

In parallel, the number of edges are accumulated on TC channel 0 and can be read on the TC_CV0 register.

Therefore, the accurate position can be read on both TC_CV registers and concatenated to form a 32-bit word.

The TC channel 0 is cleared for each increment of IDX count value.

Figure 51-31. Cycle-By-Cycle Duty Mode



51.6.5.3.2 Application Example

The figure below illustrates an application example of the Cycle-by-cycle Duty mode.

In an LED string control circuit, Cycle-by-cycle Duty mode can be used to automatically limit the current in the LED string.

51.7 Register Summary

Offset	Name	Bit Pos.								
0x00	PWM_CLK	7:0	DIVA[7:0]							
		15:8					PREA[3:0]			
		23:16	DIVB[7:0]							
		31:24					PREB[3:0]			
0x04	PWM_ENA	7:0					CHID3	CHID2	CHID1	CHID0
		15:8								
		23:16								
		31:24								
0x08	PWM_DIS	7:0					CHID3	CHID2	CHID1	CHID0
		15:8								
		23:16								
		31:24								
0x0C	PWM_SR	7:0					CHID3	CHID2	CHID1	CHID0
		15:8								
		23:16								
		31:24								
0x10	PWM_IER1	7:0					CHID3	CHID2	CHID1	CHID0
		15:8								
		23:16					FCHID3	FCHID2	FCHID1	FCHID0
		31:24								
0x14	PWM_IDR1	7:0					CHID3	CHID2	CHID1	CHID0
		15:8								
		23:16					FCHID3	FCHID2	FCHID1	FCHID0
		31:24								
0x18	PWM_IMR1	7:0					CHID3	CHID2	CHID1	CHID0
		15:8								
		23:16					FCHID3	FCHID2	FCHID1	FCHID0
		31:24								
0x1C	PWM_ISR1	7:0					CHID3	CHID2	CHID1	CHID0
		15:8								
		23:16					FCHID3	FCHID2	FCHID1	FCHID0
		31:24								
0x20	PWM_SCM	7:0					SYNC3	SYNC2	SYNC1	SYNC0
		15:8								
		23:16	PTRCS[2:0]			PTRM			UPDM[1:0]	
		31:24								
0x24	PWM_DMAR	7:0	DMADUTY[7:0]							
		15:8	DMADUTY[15:8]							
		23:16	DMADUTY[23:16]							
		31:24								
0x28	PWM_SCUC	7:0								UPDULOCK
		15:8								
		23:16								

Value	Description
0	The comparison x is disabled and can not match.
1	The comparison x is enabled and can match.

52.5.7 Fault Output

The AFEC has the Fault output connected to the FAULT input of PWM. See Fault Output and implementation of the PWM in the product.

52.5.8 Conversion Performances

For performance and electrical characteristics of the AFE, refer to the AFE Characteristics in the section "Electrical Characteristics".

Related Links

58. Electrical Characteristics for SAM V70/V71

52.6 Functional Description

52.6.1 Analog Front-End Conversion

The AFE embeds programmable gain amplifiers that must be enabled prior to any conversion. The bits PGA0EN and PGA1EN in the Analog Control register (AFEC_ACR) must be set.

The AFE uses the AFE clock to perform conversions. In order to guarantee a conversion with minimum error, after any start of conversion, the AFEC waits a number of AFE clock cycles (called transfer time) before changing the channel selection again (and so starts a new tracking operation).

AFE conversions are sequenced by two operating times: the tracking time and the conversion time.

- The tracking time represents the time between the channel selection change and the time for the controller to start the AFEC. The AFEC allows a minimum tracking time of 15 AFE clock periods.
- The conversion time represents the time for the AFEC to convert the analog signal.

The AFE clock frequency is selected in the PRESCAL field of the AFEC_MR. The tracking phase starts during the conversion of the previous channel. If the tracking time is longer than the conversion time of the12-bit AD converter (t_{CONV}), the tracking phase is extended to the end of the previous conversion.

The AFE clock frequency ranges from $f_{peripheral\ clock}/2$ if PRESCAL is 1, and $f_{peripheral\ clock}/256$ if PRESCAL is set to 255 (0xFF). PRESCAL must be programmed to provide the AFE clock frequency given in the section "Electrical Characteristics".

The AFE conversion time (t_{AFE_conv}) is applicable for all modes and is calculated as follows:

$$t_{\mathrm{AFE\_conv}} = 23 \times t_{\mathrm{AFE\ Clock}}$$

When the averager is activated, the AFE conversion time is multiplied by the OSR value.

In Free Run mode, the sampling frequency (f_S) is calculated as $1/t_{AFE\_conv}$.

57.5.3 AES Interrupt Enable Register

Name: AES_IER
Offset: 0x10
Reset: –
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
								TAGRDY
Access								W
Reset								–

Bit	15	14	13	12	11	10	9	8
								URAD
Access								W
Reset								–

Bit	7	6	5	4	3	2	1	0
								DATRDY
Access								W
Reset								–

Bit 16 – TAGRDY GCM Tag Ready Interrupt Enable

Bit 8 – URAD Unspecified Register Access Detection Interrupt Enable

Bit 0 – DATRDY Data Ready Interrupt Enable

Table 58-51. Embedded Flash Wait States for Worst-Case Conditions

FWS	Read Operations	Maximum Operating Frequency (MHz) - VDDIO 3.0V
0	1 cycle	23
1	2 cycles	46
2	3 cycles	69
3	4 cycles	92
4	5 cycles	115
5	6 cycles	138
6	7 cycles	150

58.13 Timings for STH Conditions

58.13.1 AC Characteristics

58.13.1.1 Processor Clock Characteristics

Table 58-52. Processor Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Unit
$1/(t_{CPPCK})$	Processor Clock Frequency	Worst case	–	300	MHz

58.13.1.2 Master Clock Characteristics

Table 58-53. Master Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Unit
$1/(t_{CPMCK})$	Master Clock Frequency	Worst case	–	150	MHz

58.13.1.3 I/O Characteristics

Criteria used to define the maximum frequency of the I/Os:

- Output duty cycle (40%-60%)
- Minimum output swing: 100 mV to V_{DDIO} - 100 mV
- Addition of rising and falling time inferior to 75% of the period

Table 58-54. I/O Characteristics

Symbol	Parameter	Conditions			Min	Max	Unit
		Load	V_{DDIO}	Drive Level			
FreqMax1	Pin Group 1 (1) Maximum output frequency	10 pF	3.0V	Low	–	65	MHz
				High	–	115	
		25 pF		Low	–	28	

Date	Changes
	Removed redundant Section 15.7.2. NRST Pin and Section 15.7.3. ERASE Pin (already in Section 8. “Input/Output Lines”). Removed references to Embedded Trace Buffer (ETB). Section 16.7.8 ”IEEE1149.1 JTAG Boundary Scan”: updated condtions to enable boundary scan.
	Section 18. “Fast Flash Programming Interface (FFPI)” Table 18-1 “Signal Description List“: updated XIN information. Deleted comment for XIN. Section 18.3 “Parallel Fast Flash Programming”, Figure 18-1, “16-bit Parallel Programming Interface”: changed input source for XIN. Section 18.3.3 “Entering Parallel Programming Mode”: deleted note on device clocking. Reworded steps 2 and 3.
	Section 19. “Bus Matrix (MATRIX)” Table 19-4 “Register Mapping”: corrected reset values for MATRIX_PRASx and MATRIX_PRBSx registers. In Section 19.4.8 “SMC NAND Flash Chip Select Configuration Register”: - added warning to bit description SMC_NFCS1. - changed SDRAMEN bit description and added warning.
	Section 22. “Enhanced Embedded Flash Controller (EEFC)” Updated Section 22.2 “Embedded Characteristics”. Added Figure 22-1, “Flash Memory Areas”. Section 22.4.3.6 “Calibration Bit”: updated oscillators that are calibrated in production. Section 22.4.3.7 “Security Bit Protection”: added detail on ETM.
	Section 23. “Supply Controller (SUPC)” Figure 23-2, “Separate Backup Supply Powering Scheme”: updated figure and corrected min voltage in note on ADC/DAC/ACC.
	Section 24. “Watchdog Timer (WDT)” Section 24.1 “Description”: Replaced “Idle mode” with “Sleep mode (Idle mode)”. Section 24.4 “Functional Description”: replaced “Idle mode” with “Sleep mode” Section 24.4 “Functional Description”, Section 24.5.2 “Watchdog Timer Mode Register”: modified information on WDDIS bit setting to read “When setting the WDDIS bit, and while it is set, the fields WDV and WDD must not be modified.” Section 24.5.1 “Watchdog Timer Control Register”: added note on modification of WDT_CR values.. Section 24.5.2 “Watchdog Timer Mode Register”: added Note (2) on modification of WDT_MR values.
	Section 25. “Reinforced Safety Watchdog Timer (RSWDT)”