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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv70n20b-aabt

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
PCK0–PCK2	Programmable Clock Output	Output	–		–
Real Time Clock					
RTCOUT0	Programmable RTC Waveform Output	Output	–	VDDIO	–
RTCOUT1	Programmable RTC Waveform Output	Output	–		–
Serial Wire Debug/JTAG Boundary Scan					
SWCLK/TCK	Serial Wire Clock / Test Clock (Boundary scan mode only)	Input	–	VDDIO	–
TDI	Test Data In (Boundary scan mode only)	Input	–		–
TDO/TRACESWO	Test Data Out (Boundary scan mode only)	Output	–		–
SWDIO/TMS	Serial Wire Input/ Output / Test Mode Select (Boundary scan mode only)	I/O / Input	–		–
JTAGSEL	JTAG Selection	Input	High		–
Trace Debug Port					
TRACECLK	Trace Clock	Output	–	VDDIO	PCK3 is used for ETM
TRACED0–TRACED3	Trace Data	Output	–		–
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	–
Reset/Test					
NRST	Synchronous Microcontroller Reset	I/O	Low	VDDIO	–
TST	Test Select	Input	–		–
Universal Asynchronous Receiver Transceiver - UART(x=[0:4])					

LQFP Pin	LFBGA/ TFBGA Ball	UFBGA Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		PIO Peripheral D		Reset State
					Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
77	K12	L12	VDDIO	GPIO	PA4	I/O	WKUP3/ PIODC1(3)	I	TWCK0	O	TCLK0	I	UTXD1	O	–	–	PIO, I, PU, ST
73	M11	N13	VDDIO	GPIO_AD	PA5	I/O	WKUP4/ PIODC2(3)	I	PWMC1_PWML3	O	ISI_D4	I	URXD1	I	–	–	PIO, I, PU, ST
114	B9	B11	VDDIO	GPIO_AD	PA6	I/O	–	–	–	–	PCK0	O	UTXD1	O	–	–	PIO, I, PU, ST
35	L2	N1	VDDIO	CLOCK	PA7	I/O	XIN32(4)	I	–	–	PWMC0_PWMH3	O	–	–	–	–	PIO, HiZ
36	M2	N2	VDDIO	CLOCK	PA8	I/O	XOUT32(4)	O	PWMC1_PWMH3	O	AFE0_ADTRG	I	–	–	–	–	PIO, HiZ
75	M12	L11	VDDIO	GPIO_AD	PA9	I/O	WKUP6/ PIODC3(3)	I	URXD0	I	ISI_D3	I	PWMC0_PWMFI0	I	–	–	PIO, I, PU, ST
66	L9	M10	VDDIO	GPIO_AD	PA10	I/O	PIODC4(2)	I	UTXD0	O	PWMC0_PWMEXTRG0	I	RD	I	–	–	PIO, I, PU, ST
64	J9	N10	VDDIO	GPIO_AD	PA11	I/O	WKUP7/ PIODC5(3)	I	QCS	O	PWMC0_PWMH0	O	PWMC1_PWML0	O	–	–	PIO, I, PU, ST
68	L10	N11	VDDIO	GPIO_AD	PA12	I/O	PIODC6(2)	I	QIO1	I/O	PWMC0_PWMH1	O	PWMC1_PWMH0	O	–	–	PIO, I, PU, ST
42	M3	M4	VDDIO	GPIO_AD	PA13	I/O	PIODC7(2)	I	QIO0	I/O	PWMC0_PWMH2	O	PWMC1_PWML1	O	–	–	PIO, I, PU, ST
51	K6	M6	VDDIO	GPIO_CLK	PA14	I/O	WKUP8/ PIODCEN1(3)	I	QSCK	O	PWMC0_PWMH3	O	PWMC1_PWMH1	O	–	–	PIO, I, PU, ST
49	L5	N6	VDDIO	GPIO_AD	PA15	I/O	–	–	D14	I/O	TIOA1	I/O	PWMC0_PWML3	O	I2SC0_WS	I/O	PIO, I, PU, ST
45	K5	L4	VDDIO	GPIO_AD	PA16	I/O	–	–	D15	I/O	TIOB1	I/O	PWMC0_PWML2	O	I2SC0_DI	I	PIO, I, PU, ST
25	J1	J4	VDDIO	GPIO_AD	PA17	I/O	AFE0_AD6(5)	I	QIO2	I/O	PCK1	O	PWMC0_PWMH3	O	–	–	PIO, I, PU, ST
24	H2	J3	VDDIO	GPIO_AD	PA18	I/O	AFE0_AD7(5)	I	PWMC1_PWMEXTRG1	I	PCK2	O	A14	O	–	–	PIO, I, PU, ST
23	H1	J2	VDDIO	GPIO_AD	PA19	I/O	AFE0_AD8/ WKUP9(6)	I	–	–	PWMC0_PWML0	O	A15	O	I2SC1_MCK	O	PIO, I, PU, ST
22	H3	J1	VDDIO	GPIO_AD	PA20	I/O	AFE0_AD9/ WKUP10(6)	I	–	–	PWMC0_PWML1	O	A16/BA0	O	I2SC1_CK	I/O	PIO, I, PU, ST
32	K2	M1	VDDIO	GPIO_AD	PA21	I/O	AFE0_AD1/ PIODCEN2(8)	I	RXD1	I	PCK1	O	PWMC1_PWMFI0	I	–	–	PIO, I, PU, ST
37	K3	M2	VDDIO	GPIO_AD	PA22	I/O	PIODCCLK(2)	I	RK	I/O	PWMC0_PWMEXTRG1	I	NCS2	O	–	–	PIO, I, PU, ST
46	L4	N5	VDDIO	GPIO_AD	PA23	I/O	–	–	SCK1	I/O	PWMC0_PWMH0	O	A19	O	PWMC1_PWML2	O	PIO, I, PU, ST
56	L7	N8	VDDIO	GPIO_AD	PA24	I/O	–	–	RTS1	O	PWMC0_PWMH1	O	A20	O	ISI_PCK	I	PIO, I, PU, ST
59	K8	L8	VDDIO	GPIO_AD	PA25	I/O	–	–	CTS1	I	PWMC0_PWMH2	O	A23	O	MCCK	O	PIO, I, PU, ST
62	J8	M9	VDDIO	GPIO	PA26	I/O	–	–	DCD1	I	TIOA2	O	MCDA2	I/O	PWMC1_PWMFI1	I	PIO, I, PU, ST
70	J10	N12	VDDIO	GPIO_AD	PA27	I/O	–	–	DTR1	O	TIOB2	I/O	MCDA3	I/O	ISI_D7	I	PIO, I, PU, ST
112	C9	C11	VDDIO	GPIO	PA28	I/O	–	–	DSR1	I	TCLK1	I	MCCDA	I/O	PWMC1_PWMFI2	I	PIO, I, PU, ST

Table 19-1. Bus Matrix Masters

Master Index	Name
0	Cortex-M7
1	Cortex-M7
2	Cortex-M7 Peripheral Port
3	Integrated Check Monitor
4, 5	XDMAC
6	ISI DMA
7	Media LB
8	USB DMA
9	Ethernet MAC DMA
10	CAN0 DMA
11	CAN1 DMA
12	Cortex-M7

Note: Master 12 (Cortex-M7) is only on revision B.

19.2.2 Matrix Slaves

The MATRIX manages the slaves listed in the following table. Each slave has its own arbiter, providing a different arbitration per slave.

Table 19-2. Bus Matrix Slaves

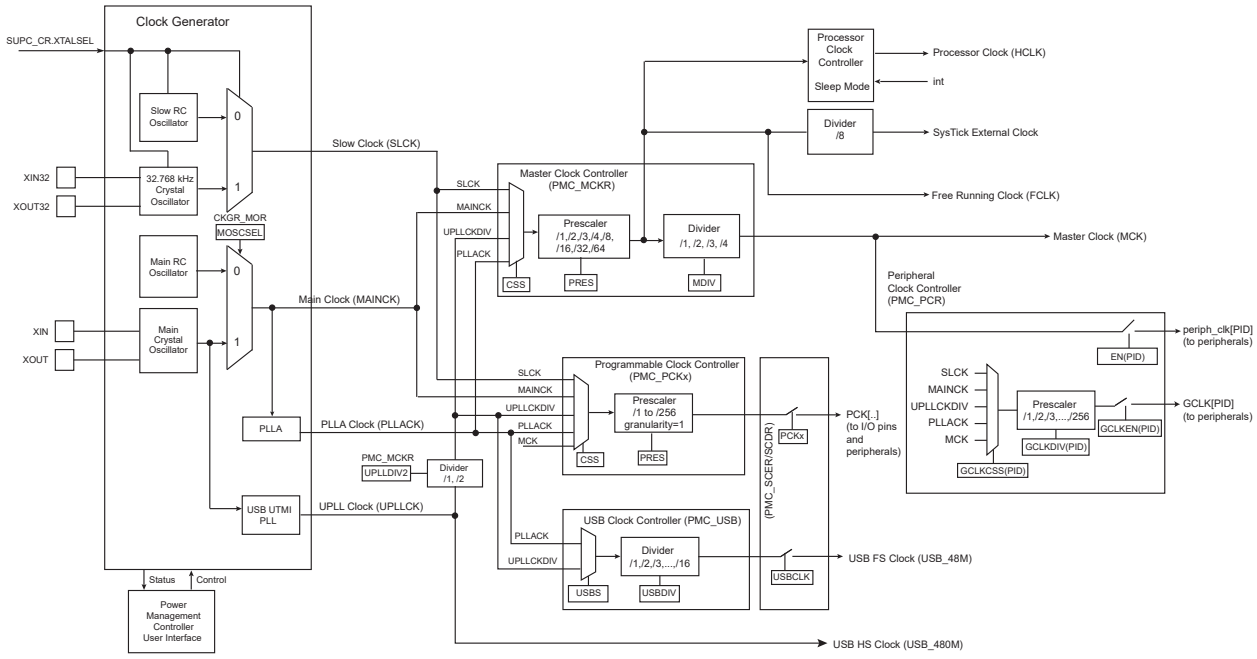
Slave Index	Name
0	Internal SRAM
1	Internal SRAM
2	Internal ROM
3	Internal Flash
4	USB High Speed Dual Port RAM (DPR)
5	External Bus Interface
6	QSPI
7	Peripheral Bridge
8	AHB Slave

19.2.3 Master to Slave Access

The following table provides valid paths for master to slave accesses. The paths shown as “-” are forbidden or not wired.

31.3 Block Diagram

Figure 31-1. General Clock Distribution Block Diagram



31.4 Master Clock Controller

The Master Clock Controller provides the Master Clock (MCK) with the selection and division of the clock generator's output signals. MCK is the source clock of the peripheral clocks.

The clock to be selected between SLCK, MAINCK, PLLACK and UPLLCKDIV is configured in PMC_MCKR.CSS. The prescaler supports the 1, 2, 3, 4, 8, 16, 32, 64 division factors and is configured using PMC_MCKR.PRES.

Each time PMC_MCKR is configured to define a new MCK, the MCKRDY bit is cleared in PMC_SR. It reads ‘0’ until MCK is established. Then, the MCKRDY bit is set and can trigger an interrupt to the processor. This feature is useful when switching from a high-speed clock to a lower one to inform the software when the change is completed.

Note: It is forbidden to modify MDIV and CSS at the same access. Each field must be modified separately with a wait for the MCKRDY flag between the first field modification and the second field modification.

31.5 Processor Clock Controller

The PMC features a Processor Clock (HCLK) Controller that implements the processor Sleep mode. HCLK can be disabled by executing the WFI (WaitForInterrupt) or the WFE (WaitForEvent) processor instruction while the LPM bit is at ‘0’ in the PMC Fast Startup Mode register (PMC_FSMR).

HCLK is enabled after a reset and is automatically re-enabled by any enabled interrupt. The processor Sleep mode is entered by disabling HCLK, which is automatically re-enabled by any enabled fast or normal interrupt, or by the reset of the product.

When processor Sleep mode is entered, the current instruction is finished before the clock is stopped, but this does not prevent data transfers from other masters of the system bus.

Table 34-3. SDRAM Configuration Mapping: 4K Rows, 256/512/1024/2048 Columns

CPU Address Line																										
27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					Bk[1:0]		Row[11:0]												Column[7:0]								M0
				Bk[1:0]			Row[11:0]												Column[8:0]								M0
			Bk[1:0]				Row[11:0]												Column[9:0]								M0
		Bk[1:0]					Row[11:0]												Column[10:0]								M0

Note: M0 is the byte address inside a 16-bit half-word and Bk[1] = BA1, Bk[0] = BA0.

Table 34-4. SDRAM Configuration Mapping: 8K Rows, 256/512/1024/2048 Columns

CPU Address Line																										
27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				Bk[1:0]		Row[12:0]													Column[7:0]								M0
			Bk[1:0]			Row[12:0]													Column[8:0]								M0
		Bk[1:0]				Row[12:0]													Column[9:0]								M0
	Bk[1:0]					Row[12:0]													Column[10:0]								M0

Note: M0 is the byte address inside a 16-bit half-word and Bk[1] = BA1, Bk[0] = BA0.

34.5 Product Dependencies

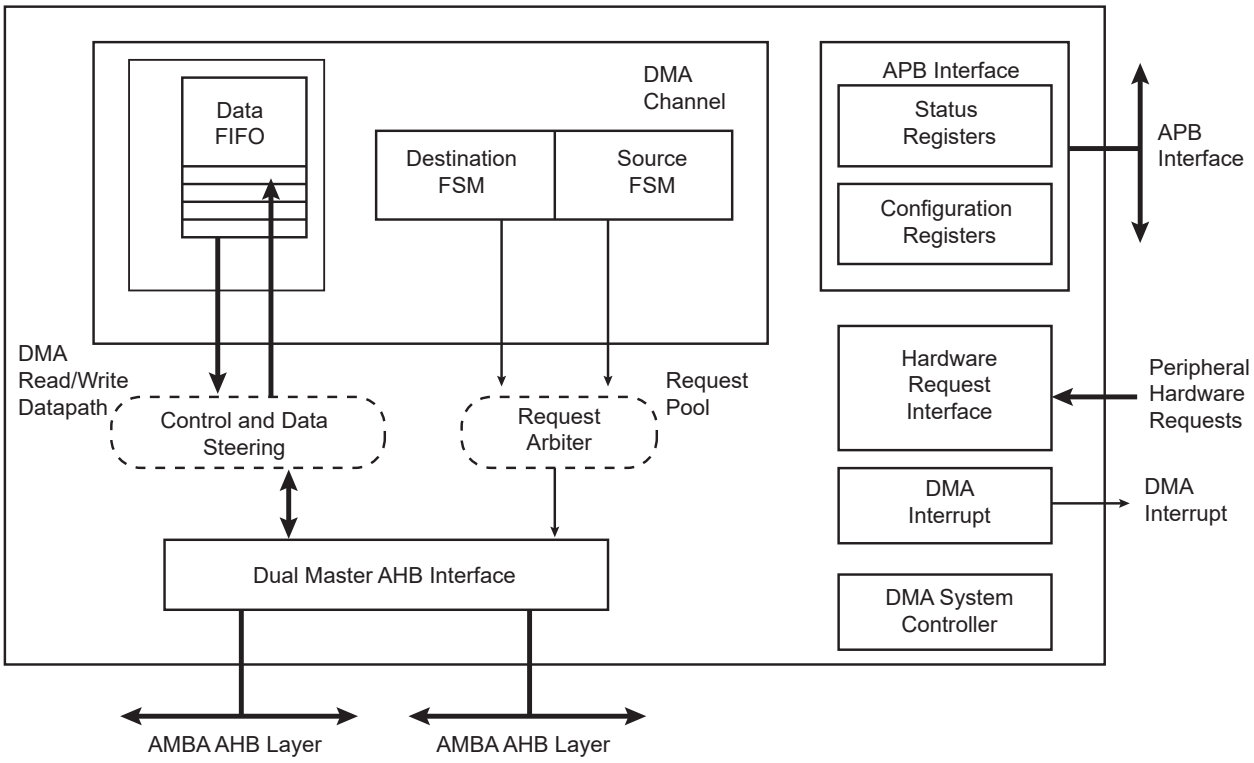
34.5.1 SDRAM Device Initialization

The initialization sequence is generated by software. The sequence to initialize SDRAM devices is the following:

1. Set the SDRAM features in the SDRAMC_CR: asynchronous timings (TRC, TRAS, etc.), number of columns, number of rows, CAS latency and data bus width. Set UNAL bit in SDRAMC_CFR1.
2. For mobile SDRAM, configure temperature-compensated self-refresh (TCSR), drive strength (DS) and partial array self-refresh (PASR) in the Low Power register (SDRAMC_LPR).
3. Select the SDRAM memory device type in the Memory Device register (SDRAMC_MDR).
4. A pause of at least 200 µs must be observed before a signal toggle.
5. A NOP command is issued to the SDRAM devices. The application must write a 1 to the MODE field in the Mode register (SDRAMC_MR) (see **Note**). Read the SDRAMC_MR and add a memory barrier assembler instruction just after the read. Perform a write access to any SDRAM address.
6. An All Banks Precharge command is issued to the SDRAM. The application must write a 2 to the MODE field in the SDRAMC_MR. Read the SDRAMC_MR and add a memory barrier assembler instruction just after the read. Perform a write access to any SDRAM address.
7. Eight autorefresh (CBR) cycles are provided. The application must set the MODE field to 4 in the SDRAMC_MR. Read the SDRAMC_MR and add a memory barrier assembler instruction just after the read. Perform a write access to any SDRAM location eight times.

36.3 Block Diagram

Figure 36-1. DMA Controller (XDMAC) Block Diagram



36.4 DMA Controller Peripheral Connections

Table 36-1. Peripheral Hardware Requests

Peripheral Name	Transfer Type	HW Interface Number (XDMAC_CC.PERID)
HSMCI	Transmit/Receive	0
SPI0	Transmit	1
SPI0	Receive	2
SPI1	Transmit	3
SPI1	Receive	4
QSPI	Transmit	5
QSPI	Receive	6
USART0	Transmit	7
USART0	Receive	8
USART1	Transmit	9
USART1	Receive	10
USART2	Transmit	11

Frame Segment	Value
Type (Octets 12–13)	86dd
IP stuff (Octets 14–19)	—
UDP (Octet 20)	11
IP stuff (Octets 21–37)	—
IP DA (Octets 38–53)	FF0X00000000018
Source IP port (Octets 54–55)	—
Dest IP port (Octets 56–57)	013F
Other stuff (Octets 58–61)	—
Message type (Octet 62)	00
Other stuff (Octets 63–93)	—
Version PTP (Octet 94)	02

Table 38-11. Example of Pdelay_Resp Frame in 1588 Version 2 (UDP/IPv6) Format

Frame Segment	Value
Preamble/SFD	55555555555555D5
DA (Octets 0–5)	—
SA (Octets 6–11)	—
Type (Octets 12–13)	86dd
IP stuff (Octets 14–19)	—
UDP (Octet 20)	11
IP stuff (Octets 21–37)	—
IP DA (Octets 38–53)	FF0200000000006B
Source IP port (Octets 54–55)	—
Dest IP port (Octets 56–57)	013F
Other stuff (Octets 58–61)	—
Message type (Octet 62)	03
Other stuff (Octets 63–93)	—
Version PTP (Octet 94)	02

For the multicast address 011B19000000 sync and delay request frames are recognized depending on the message type field, 00 for sync and 01 for delay request.

Figure 39-19. Example of an IN Pipe with one Data Bank

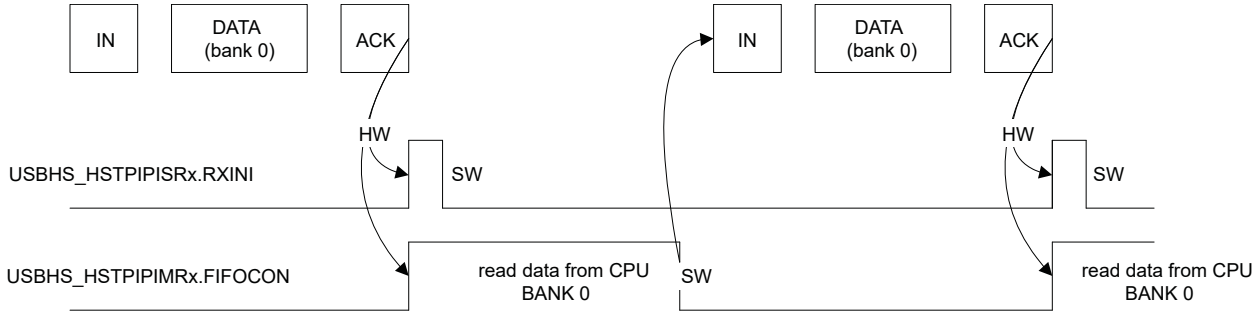
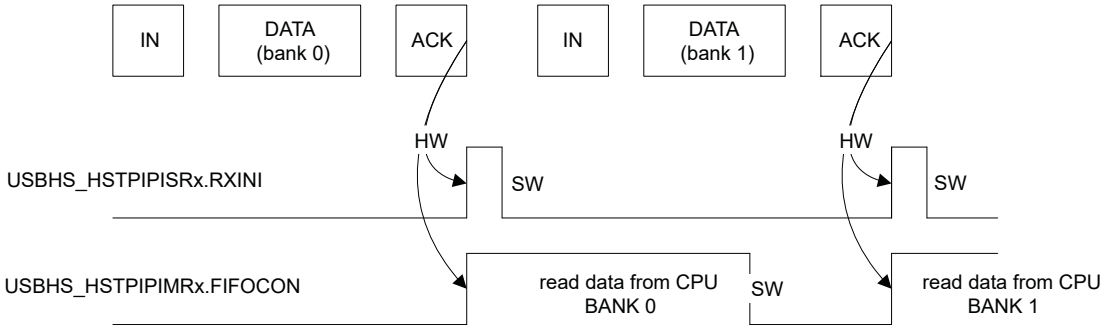


Figure 39-20. Example of an IN Pipe with two Data Banks



39.5.3.11 Management of OUT Pipes

OUT packets are sent by the host. All data which acknowledges or not the bank can be written when it is full.

The pipe must be configured and unfrozen first.

The Transmitted OUT Data Interrupt (USBHS_HSTPIPISRx.TXOUTI) bit is set at the same time as USBHS_HSTPIPIMRx.FIFOCON when the current bank is free. This triggers a PEP_x interrupt if the Transmitted OUT Data Interrupt Enable (USBHS_HSTPIPIMRx.TXOUTE) bit is one.

USBHS_HSTPIPISRx.TXOUTI is cleared by software (by writing a one to the Transmitted OUT Data Interrupt Clear (USBHS_HSTPIPIDRx.TXOUTIC) bit to acknowledge the interrupt, which has no effect on the pipe FIFO.

The user then writes into the FIFO and clears the USBHS_HSTPIPIDRx.FIFOCON bit to allow the USBHS to send the data. If the OUT pipe is composed of multiple banks, this also switches to the next bank. The USBHS_HSTPIPISRx.TXOUTI and USBHS_HSTPIPIMRx.FIFOCON bits are updated in accordance with the status of the next bank.

USBHS_HSTPIPISRx.TXOUTI is always cleared before clearing USBHS_HSTPIPIMRx.FIFOCON.

The USBHS_HSTPIPISRx.RWALL bit is set when the current bank is not full, i.e., when the software can write further data into the FIFO.

Note:

1. If the user decides to switch to the Suspend state (by writing a zero to the USBHS_HSTCTRL.SOFE bit) while a bank is ready to be sent, the USBHS automatically exits this state and the bank is sent.
2. In High-speed operating mode, the host controller automatically manages the PING protocol to maximize the USB bandwidth. The user can tune the PING protocol by handling the Ping Enable

Bit 17 – CTRLDIR Control Direction

Value	Description
0	Cleared after a SETUP packet to indicate that the following packet is an OUT packet.
1	Set after a SETUP packet to indicate that the following packet is an IN packet.

Bit 16 – RWALL Read/Write Allowed
This bit is set for IN endpoints when the current bank is not full, i.e., the user can write further data into the FIFO.

This bit is set for OUT endpoints when the current bank is not empty, i.e., the user can read further data from the FIFO.

This bit is never set if USBHS_DEVEPTIMRx.STALLRQ = 1 or in case of error.

This bit is cleared otherwise.

This bit should not be used for control endpoints.

Bits 15:14 – CURRBK[1:0] Current Bank
This bit is set for non-control endpoints, to indicate the current bank:

This field may be updated one clock cycle after the RWALL bit changes, so the user should not poll this field as an interrupt bit.

Value	Name	Description
0	BANK0	Current bank is bank0
1	BANK1	Current bank is bank1
2	BANK2	Current bank is bank2
3	Reserved	

Bits 13:12 – NBUSYBK[1:0] Number of Busy Banks
This field is set to indicate the number of busy banks:

For IN endpoints, it indicates the number of banks filled by the user and ready for IN transfer. When all banks are free, this triggers a PEP_x interrupt if NBUSYBKE = 1.

For OUT endpoints, it indicates the number of banks filled by OUT transactions from the host. When all banks are busy, this triggers a PEP_x interrupt if NBUSYBKE = 1.

When the USBHS_DEVEPTIMRx.FIFOCON bit is cleared (by writing a one to the USBHS_DEVEPTIMRx.FIFOCONC bit) to validate a new bank, this field is updated two or three clock cycles later to calculate the address of the next bank.

A PEP_x interrupt is triggered if:

Value	Name	Description
0	0_BUSY	0 busy bank (all banks free)
1	1_BUSY	1 busy bank
2	2_BUSY	2 busy banks
3	3_BUSY	3 busy banks • for IN endpoint, USBHS_DEVEPTIMRx.NBUSYBKE = 1 and all the banks are free;

Enable register (TWIHS_IER). If the slave acknowledges the byte, the data written in the TWIHS_THR is then shifted in the internal shifter and transferred. When an acknowledge is detected, the TXRDY bit is set until a new write in the TWIHS_THR.

TXRDY is used as Transmit Ready for the DMA transmit channel.

While no new data is written in the TWIHS_THR, the serial clock line is tied low. When new data is written in the TWIHS_THR, the SCL is released and the data is sent. Setting the STOP bit in TWIHS_CR generates a STOP condition.

After a master write transfer, the serial clock line is stretched (tied low) as long as no new data is written in the TWIHS_THR or until a STOP command is performed.

To clear the TXRDY flag, first set the bit TWIHS_CR.MSDIS, then set the bit TWIHS_CR.MSEN.

See the figures below.

Figure 43-4. Master Write with One Data Byte

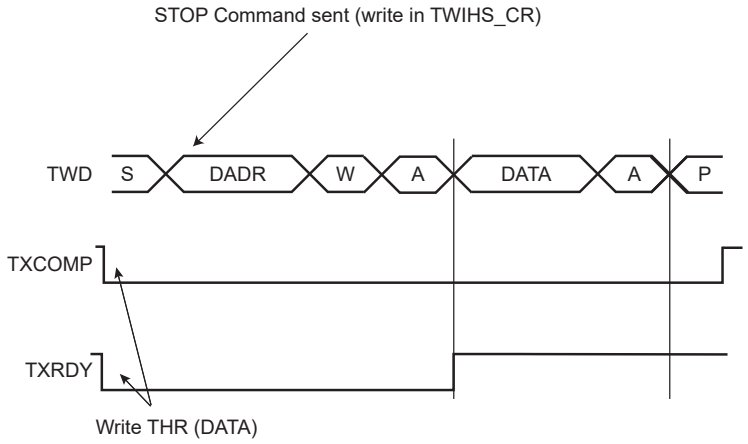


Figure 43-5. Master Write with Multiple Data Bytes

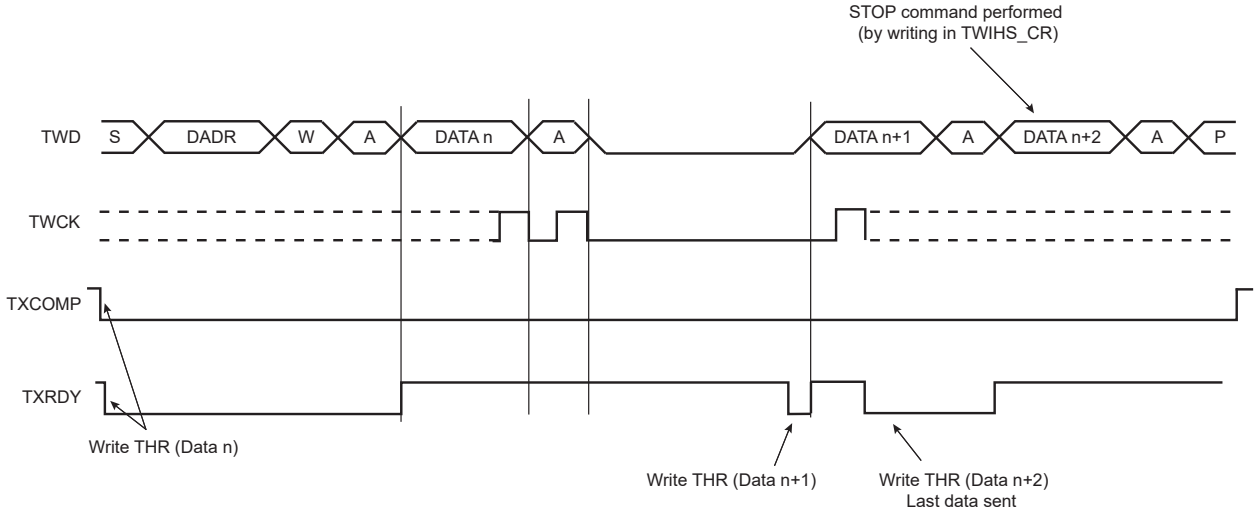


Figure 46-46. Master Node Configuration, NACT = SUBSCRIBE

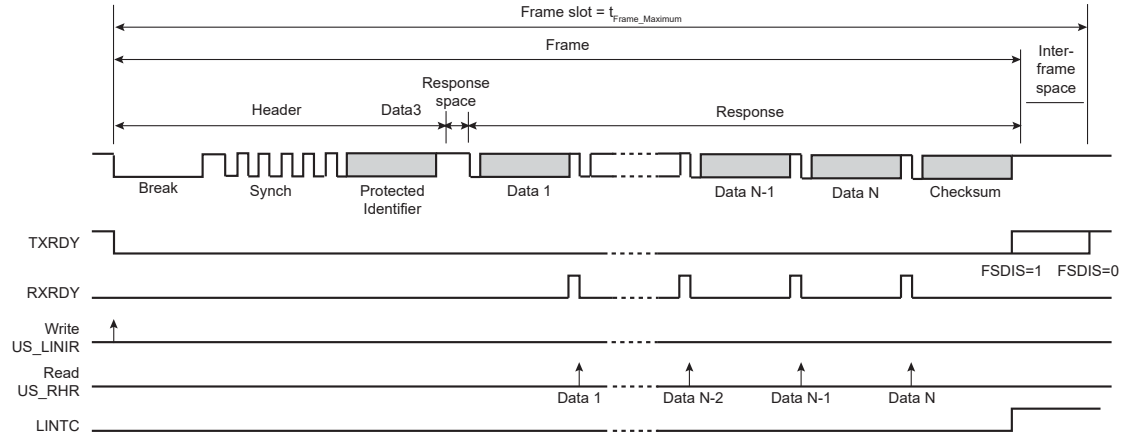
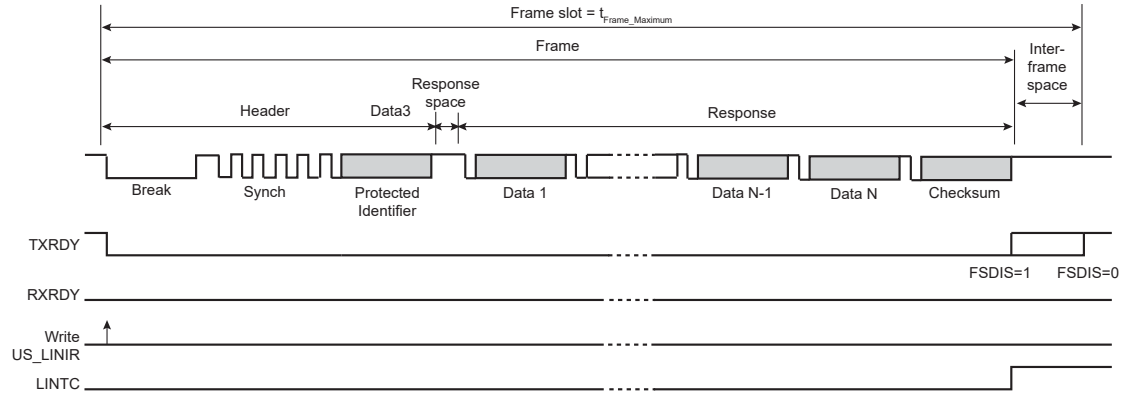


Figure 46-47. Master Node Configuration, NACT = IGNORE



46.6.9.15.2 Slave Node Configuration

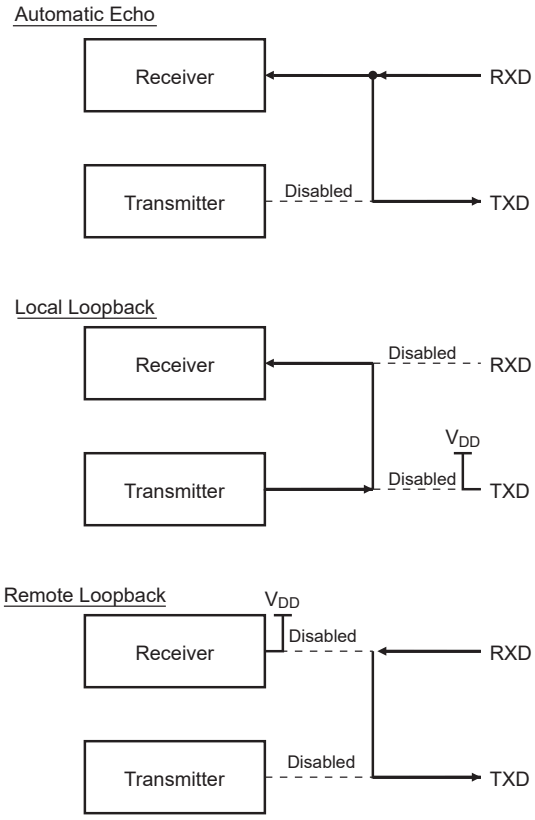
- Write TXEN and RXEN in US_CR to enable both the transmitter and the receiver.
- Write USART_MODE in US_MR to select the LIN mode and the slave node configuration.
- Write CD and FP in US_BRGR to configure the baud rate.
- Wait until LINID in US_CSR rises.
- Check LINISFE and LINPE errors.
- Read IDCHR in US_RHR.
- Write NACT, PARDIS, CHKDIS, CHKTYPE, DLCM and DLC in US_LINMR to configure the frame transfer.

IMPORTANT: If the NACT configuration for this frame is PUBLISH, the US_LINMR must be written with NACT = PUBLISH even if this field is already correctly configured, in order to set the TXREADY flag and the corresponding write transfer request.

What comes next depends on the NACT configuration:

- Case 1: NACT = PUBLISH, the LIN controller sends the response
  - Wait until TXRDY in US_CSR rises.
  - Write TCHR in US_THR to send a byte.
  - If all the data have not been written, redo the two previous steps.
  - Wait until LINTC in US_CSR rises.
  - Check the LIN errors.

Figure 47-14. Test Modes



48.7.14 HBI Channel Busy 1 Register

Name: MLB_HCBR1
Offset: 0x09C
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	CHB: Bitwise Channel Busy Bit [63[31:24]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CHB: Bitwise Channel Busy Bit [63[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CHB: Bitwise Channel Busy Bit [63[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CHB: Bitwise Channel Busy Bit [63[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CHB: Bitwise Channel Busy Bit [63[31:0] 32]
CHB[n] = 1 indicates that channel n is busy.

49.6.6 MCAN RAM Watchdog Register

Name: MCAN_RWD
Offset: 0x14
Reset: 0x00000000
Property: Read/Write

The RAM Watchdog monitors the Message RAM response time. A Message RAM access via the MCAN's Generic Master Interface starts the Message RAM Watchdog Counter with the value configured by MCAN_RWD.WDC. The counter is reloaded with MCAN_RWD.WDC when the Message RAM signals successful completion by activating its READY output. In case there is no response from the Message RAM until the counter has counted down to zero, the counter stops and interrupt flag MCAN_IR.WDI is set. The RAM Watchdog Counter is clocked by the system bus clock (peripheral clock).

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	WDV[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WDC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:8 – WDV[7:0] Watchdog Value (read-only)
Watchdog Counter Value for the current message located in RAM.

Bits 7:0 – WDC[7:0] Watchdog Configuration (read/write)
Start value of the Message RAM Watchdog Counter. The counter is disabled when WDC is cleared.

49.6.20 MCAN Global Filter Configuration

Name: MCAN_GFC
Offset: 0x80
Reset: 0x00000000
Property: Read/Write

Global settings for Message ID filtering. The Global Filter Configuration controls the filter path for standard and extended messages as illustrated in Standard Message ID Filter Path and Extended Message ID Filter Path.

This register can only be written if the bits CCE and INIT are set in MCAN CC Control Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			ANFS[1:0]		ANFE[1:0]		RRFS	RRFE
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bits 5:4 – ANFS[1:0] Accept Non-matching Frames Standard
Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated.

Value	Name	Description
0	RX_FIFO_0	Accept in Rx FIFO 0
1	RX_FIFO_1	Accept in Rx FIFO 1
2-3	REJECTED	Message rejected

Bits 3:2 – ANFE[1:0] Accept Non-matching Frames Extended
Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated.

Value	Name	Description
0	RX_FIFO_0	Accept in Rx FIFO 0
1	RX_FIFO_1	Accept in Rx FIFO 1
2-3	REJECTED	Message rejected

Bit 7 – ETRGS External Trigger Status (cleared on read)

Value	Description
0	External trigger has not occurred since the last read of the Status Register.
1	External trigger has occurred since the last read of the Status Register.

Bit 6 – LDRBS RB Loading Status (cleared on read)

Value	Description
0	RB Load has not occurred since the last read of the Status Register or TC_CMRx.WAVE = 1.
1	RB Load has occurred since the last read of the Status Register, if TC_CMRx.WAVE = 0.

Bit 5 – LDRAS RA Loading Status (cleared on read)

Value	Description
0	RA Load has not occurred since the last read of the Status Register or TC_CMRx.WAVE = 1.
1	RA Load has occurred since the last read of the Status Register, if TC_CMRx.WAVE = 0.

Bit 4 – CPCS RC Compare Status (cleared on read)

Value	Description
0	RC Compare has not occurred since the last read of the Status Register.
1	RC Compare has occurred since the last read of the Status Register.

Bit 3 – CPBS RB Compare Status (cleared on read)

Value	Description
0	RB Compare has not occurred since the last read of the Status Register or TC_CMRx.WAVE = 0.
1	RB Compare has occurred since the last read of the Status Register, if TC_CMRx.WAVE = 1.

Bit 2 – CPAS RA Compare Status (cleared on read)

Value	Description
0	RA Compare has not occurred since the last read of the Status Register or TC_CMRx.WAVE = 0.
1	RA Compare has occurred since the last read of the Status Register, if TC_CMRx.WAVE = 1.

Bit 1 – LOVRS Load Overrun Status (cleared on read)

Value	Description
0	Load overrun has not occurred since the last read of the Status Register or TC_CMRx.WAVE = 1.
1	RA or RB have been loaded at least twice without any read of the corresponding register since the last read of the Status Register, if TC_CMRx.WAVE = 0.

Bit 0 – COVFS Counter Overflow Status (cleared on read)

If the waveform is center-aligned, then the output waveform period depends on the channel counter source clock and can be calculated:

– By using the PWM peripheral clock divided by a given prescaler value “X” (where X = 2^{PREA} is 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, or 1024). The resulting period formula is:

$$\frac{(2 \times X \times \mathrm{CPRDUPD})}{f_{\mathrm{peripheral\ clock}}}$$

– By using the PWM peripheral clock divided by a given prescaler value “X” (see above) and by either the DIVA or the DIVB divider. The formula becomes, respectively:

$$\frac{(2 \times X \times \mathrm{CPRDUPD} \times \mathrm{DIVA})}{f_{\mathrm{peripheral\ clock}}} \text{ or } \frac{(2 \times X \times \mathrm{CPRDUPD} \times \mathrm{DIVB})}{f_{\mathrm{peripheral\ clock}}}$$

52.7.24 AFEC Sample & Hold Mode Register

Name: AFEC_SHMR
Offset: 0xA0
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the AFEC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					DUAL11	DUAL10	DUAL9	DUAL8
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DUAL7	DUAL6	DUAL5	DUAL4	DUAL3	DUAL2	DUAL1	DUAL0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 – DUALx Dual Sample & Hold for Channel x

Value	Description
0	Single Sample-and-Hold mode.
1	Dual Sample-and-Hold mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Gain = 2		±2.1		
		Gain = 4		±2.5		
DNL	Differential Non-Linearity	–	-6	±2	6	LSB
Single-Ended Mode						
INL	Integral Non-Linearity	Gain = 1	-12	±2	12	LSB
		Gain = 2		±2.6		
		Gain = 4		±2.7		
DNL	Differential Non-Linearity	–	-6	±2	6	LSB

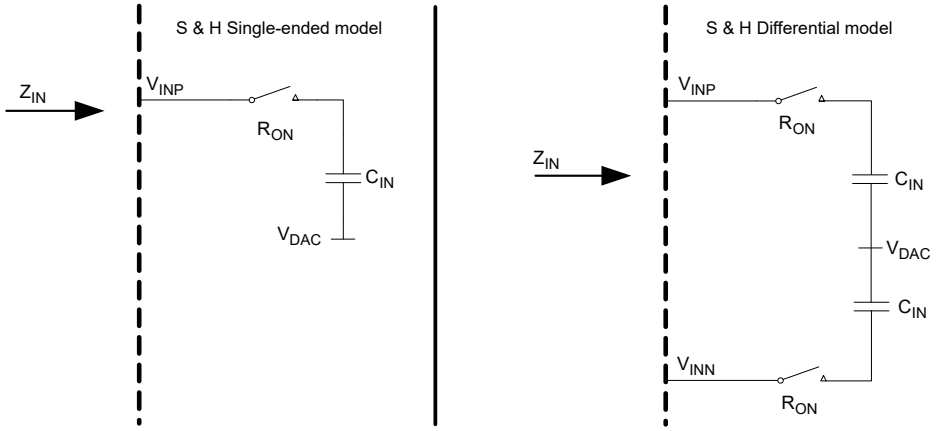
Note: INL/DNL given inside the linear range of the AFE: 2% to 98% of VREFP.

Table 59-36. AFE Offset and Gain Error, V_{VREFP} = 1.7V to 3.3V

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Unit
Differential Mode						
E_O	Differential Offset Error (see **Note 1**)	Gain=1	-20	–	35	LSB
E_G	Differential Gain Error	Gain=1	-0.3	0	0.7	%
		Gain=2	-0.3	0.3	1.4	
		Gain=4	-0.3	0.7	3.3	
Single-Ended Mode						
E_O	Single-ended Offset Error (see **Note 1**)	Gain=1	-20	–	35	LSB
E_G	Single-ended Gain Error	Gain=1	0.3	0.7	1.8	%
		Gain=2	0.3	1.3	3.6	
		Gain=4	0.3	1.7	4.7	

59.8.6 AFE Channel Input Impedance

Figure 59-15. Input Channel Model



Date	Changes
	Section 18.12.10 “Write Protection Status Register”: in WPVS bit description, replaced two instances of “since the last read of the MATRIX_WPSR” with “since the last write of the MATRIX_WPMR”.
	Section 21. “Enhanced Embedded Flash Controller (EEFC)” Section 21.4.3.2 “Write Commands”: added information on DMA write accesses.
	Section 30. “Power Management Controller (PMC)” Section 30.9 “Asynchronous Partial Wake-up”: inserted new sub-section “Asynchronous Partial Wake-up in Wait Mode (SleepWalking)” to better describe SleepWalking. Section 30.10 “Free-Running Processor Clock”: removed reference to MCK.
	Section 31. “Parallel Input/Output Controller (PIO)” Section 31.2 “Embedded Characteristics”: added bullet on Programmable I/O Drive. Added Section 31.5.12 “Programmable I/O Drive”. Section 31.5.15.4 “Programming Sequence”: “With DMA”: in fifth step, replaced reference to BTCx with ‘DMA status flag to indicate that the buffer transfer is complete’ Table 31-5 “Register Mapping”: added PIO_DRIVER register at offset 0x0118 and added Section 31.6.49 “PIO I/O Drive Register”.
	Section 35. “DMA Controller (XDMAC)” Added Section 35.3 “DMA Controller Peripheral Connections”.
	Section 37. “USB High-Speed Interface (USBHS)” Table 37-1 “Description of USB Pipes/Endpoints“; corrected data in columns ‘DMA’ and ‘High Bandwidth’. Modified signal names to HSDM/DM and HSDP/DP in Figure 37-1 “USBHS Block Diagram” and Table 37-2 “Signal Description”. Updated descriptions. Removed Section 37.3.1 “Application Block Diagram” and Figures 37-2, 37-3 and 37-4. Removed Section 37.4.1 “I/O Lines”. Modified Section 37.5.3.3 “Device Detection”. Section 37.6.2 “General Status Register”, Section 37.6.3 “General Status Clear Register”, Section 37.6.4 “General Status Set Register”: removed bit VBUSRQ and bit description. Bit 9 now reserved in these registers.
24-Feb-15	Section 38. “Ethernet MAC (GMAC)” Section 38.8.13 “GMAC Interrupt Mask Register”: corrected general bit description (swapped definitions provided for 0: and 1:)
	Section 40. “Quad SPI Interface (QSPI)” Section 40.5.4 “Direct Memory Access Controller (DMA)”: added Note on 32-bit aligned DMA write accesses. Figure 40-9 “Instruction Transmission Flow Diagram”: modified text if TFRTYP = 0