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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv70n20b-cb

19.4.3 Bus Matrix Priority Registers A For Slaves

Name: MATRIX_PRASx
Offset: 0x80 + x*0x08 [x=0..8]
Reset: 0x00000222
Property: Read/Write

This register can only be written if the WPE bit is cleared in the Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
			M7PR[1:0]				M6PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	23	22	21	20	19	18	17	16
			M5PR[1:0]				M4PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	15	14	13	12	11	10	9	8
			M3PR[1:0]				M2PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			1	0

Bit	7	6	5	4	3	2	1	0
			M1PR[1:0]				M0PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			1	0			1	0

Bits 0:1, 4:5, 8:9, 12:13, 16:17, 20:21, 24:25, 28:29 – MxPR Master x Priority
Fixed priority of Master x for accessing the selected slave. The higher the number, the higher the priority.

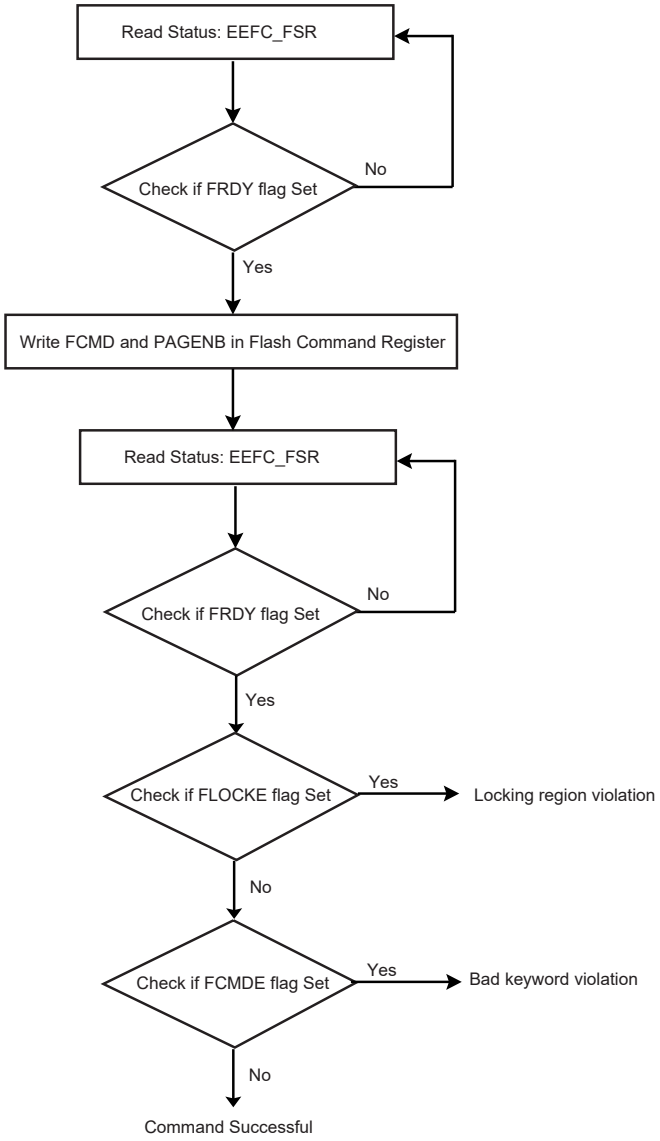
All the masters programmed with the same MxPR value for the slave make up a priority pool.

Round-robin arbitration is used in the lowest (MxPR = 0) and highest (MxPR = 3) priority pools.

Fixed priority is used in intermediate priority pools (MxPR = 1) and (MxPR = 2).

See “Arbitration Priority Scheme” for details.

Figure 22-7. Command State Chart



22.4.3.1 Get Flash Descriptor Command

This command provides the system with information on the Flash organization. The system can take full advantage of this information. For instance, a device could be replaced by one with more Flash capacity, and so the software is able to adapt itself to the new configuration.

To get the embedded Flash descriptor, the application writes the GETD command in EEFC_FCR. The first word of the descriptor can be read by the software application in EEFC_FRR as soon as the FRDY flag in EEFC_FSR rises. The next reads of EEFC_FRR provide the following word of the descriptor. If extra read operations to EEFC_FRR are done after the last word of the descriptor has been returned, the EEFC_FRR value is 0 until the next valid command.

28.5 Register Summary

Offset	Name	Bit Pos.								
0x00	RTT_MR	7:0	RTPRES[7:0]							
		15:8	RTPRES[15:8]							
		23:16				RTTDIS		RTTRST	RTTINCIEN	ALMIEN
		31:24								RTC1HZ
0x04	RTT_AR	7:0	ALMV[7:0]							
		15:8	ALMV[15:8]							
		23:16	ALMV[23:16]							
		31:24	ALMV[31:24]							
0x08	RTT_VR	7:0	CRTV[7:0]							
		15:8	CRTV[15:8]							
		23:16	CRTV[23:16]							
		31:24	CRTV[31:24]							
0x0C	RTT_SR	7:0							RTTINC	ALMS
		15:8								
		23:16								
		31:24								

Table 32-3. Programming Example

Register	Value to be Written
PIO_PER	0x0000_FFFF
PIO_PDR	0xFFFF_0000
PIO_OER	0x0000_00FF
PIO_ODR	0xFFFF_FF00
PIO_IFER	0x0000_0F00
PIO_IFDR	0xFFFF_F0FF
PIO_SODR	0x0000_0000
PIO_CODR	0x0FFF_FFFF
PIO_IER	0x0F00_0F00
PIO_IDR	0xF0FF_F0FF
PIO_MDER	0x0000_000F
PIO_MDDR	0xFFFF_FFF0
PIO_PUDR	0xFFF0_00F0
PIO_PUER	0x000F_FF0F
PIO_PPDDR	0xFF0F_FFFF
PIO_PPDER	0x00F0_0000
PIO_ABCDSR1	0xF0F0_0000
PIO_ABCDSR2	0xFF00_0000
PIO_OWER	0x0000_000F
PIO_OWDR	0x0FFF_FFF0

32.5.16 Register Write Protection

To prevent any single software error from corrupting PIO behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the PIO Write Protection Mode Register (PIO_WPMR).

If a write access to a write-protected register is detected, the WPVS flag in the PIO Write Protection Status Register (PIO_WPSR) is set and the field WPVSRC indicates the register in which the write access has been attempted.

The WPVS bit is automatically cleared after reading the PIO_WPSR.

The following registers can be write-protected:

- PIO Enable Register
- PIO Disable Register
- PIO Output Enable Register
- PIO Output Disable Register
- PIO Input Filter Enable Register

32.6.1.10 PIO Set Output Data Register

Name: PIO_SODR
Offset: 0x0030
Property: Write-only

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Set Output Data

Value	Description
0	No effect.
1	Sets the data to be driven on the I/O line.

32.6.1.34 PIO Output Write Disable Register

Name: PIO_OWDR
Offset: 0x00A4
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Output Write Disable

Value	Description
0	No effect.
1	Disables writing PIO_ODSR for the I/O line.

38.8.62 GMAC Multicast Frames Received Register

Name: GMAC_MFR
Offset: 0x160
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	MFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	MFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	MFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MFRX[31:0] Multicast Frames Received without Error
This register counts the number of multicast frames successfully received without error, excluding pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

Value	Description
0	Cleared when USBHS_HSTPIPICR.SHORTPACKETIC = 1.
1	Set when a short packet is received by the host controller (packet length inferior to the PSIZE programmed field).

Bit 6 – RXSTALLDI Received STALLed Interrupt
This bit is set when a STALL handshake has been received on the current bank of the pipe. The pipe is automatically frozen. This triggers an interrupt if USBHS_HSTPIPIMR.RXSTALLE = 1.

Value	Description
0	Cleared when USBHS_HSTPIPICR.RXSTALLDIC = 1.

Bit 5 – OVERFI Overflow Interrupt

Value	Description
0	Cleared when USBHS_HSTPIPICR.OVERFIC = 1.
1	Set when the current pipe has received more data than the maximum length of the current pipe. An interrupt is triggered if USBHS_HSTPIPIMR.OVERFIE = 1.

Bit 4 – NAKEDI NAKed Interrupt

Value	Description
0	Cleared when USBHS_HSTPIPICR.NAKEDIC = 1.
1	Set when a NAK has been received on the current bank of the pipe. This triggers an interrupt if USBHS_HSTPIPIMR.NAKEDE = 1.

Bit 3 – PERRI Pipe Error Interrupt

Value	Description
0	Cleared when the error source bit is cleared.
1	Set when an error occurs on the current bank of the pipe. This triggers an interrupt if the USBHS_HSTPIPIMR.PERRE bit is set. Refer to the USBHS_HSTPIPERRx register to determine the source of the error.

Bit 2 – TXSTPI Transmitted SETUP Interrupt

Value	Description
0	Cleared when USBHS_HSTPIPICR.TXSTPIC = 1.
1	Set, for control pipes, when the current SETUP bank is free and can be filled. This triggers an interrupt if USBHS_HSTPIPIMR.TXSTPE = 1.

Bit 1 – TXOUTI Transmitted OUT Data Interrupt

Value	Description
0	Cleared when USBHS_HSTPIPICR.TXOUTIC = 1.
1	Set when the current OUT bank is free and can be filled. This triggers an interrupt if USBHS_HSTPIPIMR.TXOUTE = 1.

Bit 0 – RXINI Received IN Data Interrupt

Bit 0 – RXINIC Received IN Data Interrupt Clear

Offset	Name	Bit Pos.								
0x38	SPI_CSR2	7:0	BITS[3:0]				CSAAT	CSNAAT	NCPHA	CPOL
		15:8	SCBR[7:0]							
		23:16	DLYBS[7:0]							
		31:24	DLYBCT[7:0]							
0x3C	SPI_CSR3	7:0	BITS[3:0]				CSAAT	CSNAAT	NCPHA	CPOL
		15:8	SCBR[7:0]							
		23:16	DLYBS[7:0]							
		31:24	DLYBCT[7:0]							
0x40 ... 0xE3	Reserved									
0xE4	SPI_WPMR	7:0						WPCREN	WPITEN	WPEN
		15:8	WPKEY[7:0]							
		23:16	WPKEY[15:8]							
		31:24	WPKEY[23:16]							
0xE8	SPI_WPSR	7:0								WPVS
		15:8	WPVSRC[7:0]							
		23:16								
		31:24								

46.7.46 USART Write Protection Mode Register

Name: US_WPMR
Offset: 0x00E4
Reset: 0x0
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	WPKEY[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	WPKEY[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	WPKEY[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
								WPEN
Access								
Reset								0

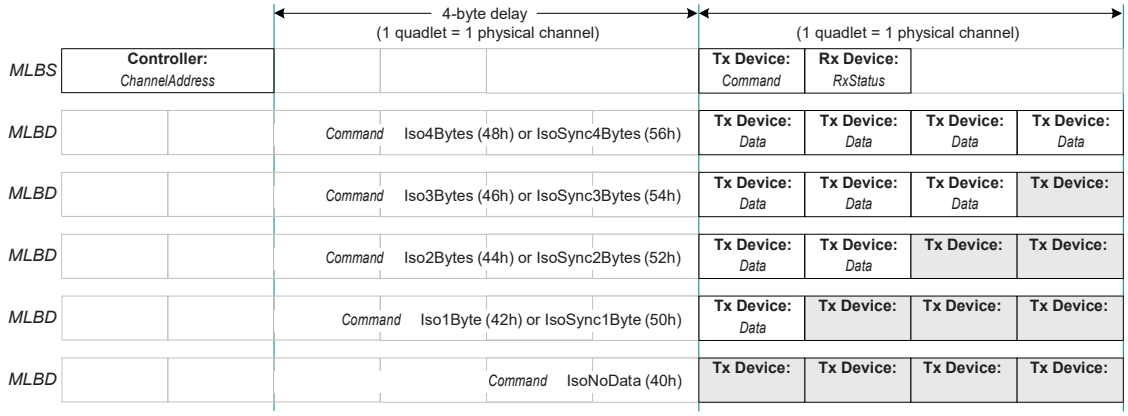
Bits 31:8 – WPKEY[23:0] Write Protection Key

Value	Name	Description
0x555341	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

Bit 0 – WPEN Write Protection Enable
See Section 7.12 “Register Write Protection” for the list of registers that can be write-protected.

Value	Description
0	Disables the write protection if WPKEY corresponds to 0x555341 (“USA” in ASCII).
1	Enables the write protection if WPKEY corresponds to 0x555341 (“USA” in ASCII).

Figure 48-13. MediaLB Isochronous Data Structure



The isochronous flow for a Tx Device is illustrated in Figure 48-14. The data transfer blocks (slanted rectangle shapes) occur only during a physical channel (PCn) associated with the logical channel defined by a single ChannelAddress. Similar to the synchronous flow, isochronous data immediately starts transmitting. When data exists from the application, the IsoSync?Bytes commands are used to indicate the start of a block, which provides alignment information to the Rx Device. The Iso?Bytes commands indicate the middle of a block of data. The definition of block for isochronous data is outside the scope of this document. For physical channels that transfer less than four bytes, the Rx Device must only use/ store the number of valid bytes, and ignore the unused portion.

The isochronous flow for an Rx Device is illustrated in Figure 48-15. The NoData command indicates that the channel is not setup yet. Once an isochronous channel is setup, the Rx Device continually receives the channel data, similar to synchronous data. The only two valid responses for an isochronous channel are ReceiverBusy, and the default bus state of ReceiverReady. Although Rx Devices can respond with ReceiverBusy, its use should be minimized, since Tx Devices may not be able to store much isochronous data that gets backed up due to the ReceiverBusy responses. If any Rx Device uses ReceiverBusy, then only one Rx Device is allowed. If all targeted Rx Devices do not drive RxStatus (default ReceiverReady response), then the isochronous stream can support multiple Rx Devices (broadcast).

Field	No. of Bits	Description	Accessibility
		Reserved for synchronous and isochronous channels.	
MEP1	1	Most Ethernet Packet (MEP) indicator for ping buffer page: 0 = Not MEP 1 = MEP MEP1 only valid for the first page of a segmented buffer. Reserved for control, synchronous and isochronous channels.	Rsvd for Tx r,u (1),c0 (2) for Rx
MEP2	1	MEP packet indicator for pong buffer page: 0 = not MEP 1 = MEP MEP2 only valid for the first page of a segmented buffer. Reserved for control, synchronous and isochronous channels.	Reserved for Tx r,u (1),c0 (2) for Rx
BD1(2)	11 to 13	Buffer depth for ping buffer page: 11 or 12-bits for asynchronous and control channels. 13-bits for synchronous and isochronous channels.	r,w
BD2(2)	11 to 13	Buffer depth for pong buffer page: 11 or 12-bits for asynchronous and control channels. 13-bits for synchronous and isochronous channels.	r,w
BA1	32	Buffer base address for ping buffer page	r,w
BA2	32	Buffer base address for pong buffer page	r,w
Reserved	varies	Software writes a zero to all Reserved bits when the entry is initialized. The reserved bits are Read-only after initialization.	r,w,u (1)

Note:

1. “u” means “Updated periodically by hardware”.
2. “c0” means “Cleared by writing a 0”.
3. The buffer depth (BD1 and BD2) for synchronous channels must consider if Multi-Frame per Sub-buffer mode is enabled.

Data exchange across the AHB interface can be configured as Little Endian (LE = 1) or Big Endian (LE = 0). The following figure provides an overview of the endian options, chosen by an ADT descriptor field.

48.7.7 MediaLB Control 1 Register

Name: MLB_MLBC1
Offset: 0x03C
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	NDA[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CLKM	LOCK						
Access								
Reset	0	0						

Bits 15:8 – NDA[7:0] Node Device Address
Used for system commands directed to individual MediaLB nodes.

Bit 7 – CLKM MediaLB Clock Missing Status (cleared by writing a 0)
Set when MLBCLK (MediaLB clock) is not toggling at the pin; cleared by software.

Bit 6 – LOCK MediaLB Lock Error Status (cleared by writing a 0)
Set when MediaLB is unlocked; cleared by software.

51.7.14 PWM Interrupt Enable Register 2

Name: PWM_IER2
Offset: 0x34
Reset: –
Property: Write-only

This register can only be written if bits WPSWS1 and WPHWS1 are cleared in the PWM Write Protection Status Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CMPU7	CMPU6	CMPU5	CMPU4	CMPU3	CMPU2	CMPU1	CMPU0
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bit	15	14	13	12	11	10	9	8
	CMPM7	CMPM6	CMPM5	CMPM4	CMPM3	CMPM2	CMPM1	CMPM0
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–

Bit	7	6	5	4	3	2	1	0
					UNRE			WRDY
Access					W			W
Reset					–			–

Bits 16, 17, 18, 19, 20, 21, 22, 23 – CMPUx Comparison x Update Interrupt Enable

Bits 8, 9, 10, 11, 12, 13, 14, 15 – CMPMx Comparison x Match Interrupt Enable

Bit 3 – UNRE Synchronous Channels Update Underrun Error Interrupt Enable

Bit 0 – WRDY Write Ready for Synchronous Channels Update Interrupt Enable

55.6.2 ICM Control Register

Name: ICM_CTRL
Offset: 0x04
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RMEN[3:0]				RMDIS[3:0]			
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	–	0	0	0	–

Bit	7	6	5	4	3	2	1	0
	REHASH[3:0]					SWRST	DISABLE	ENABLE
Access	W	W	W	W		W	W	W
Reset	0	0	0	–		–	–	–

Bits 15:12 – RMEN[3:0] Region Monitoring Enable
Monitoring is activated by default.

Value	Description
0	No effect
1	When bit RMEN[i] is set to one, the monitoring of region with identifier i is activated.

Bits 11:8 – RMDIS[3:0] Region Monitoring Disable

Value	Description
0	No effect
1	When bit RMDIS[i] is set to one, the monitoring of region with identifier i is disabled.

Bits 7:4 – REHASH[3:0] Recompute Internal Hash

Value	Description
0	No effect
1	When REHASH[i] is set to one, Region i digest is re-computed. This bit is only available when region monitoring is disabled.

Bit 2 – SWRST Software Reset

Table 58-14. Typical Sleep Mode Current Consumption vs. Master Clock (MCK) Variation with Fast RC

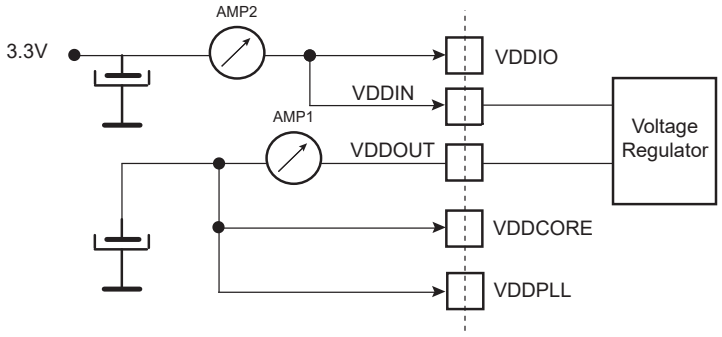
Core Clock/MCK (MHz)	VDDCORE Consumption (AMP1)	Total Consumption (AMP2)	Unit	Wakeup Time	Unit
12	2.0	2.0	mA	12	µs
8	1.5	1.5		18	
4	1.0	1.1		31	
2	0.8	0.8		62	
1	0.6	0.7		123	
0.5	0.6	0.6		247	
0.25	0.5	0.5		494	

58.3.3 Wait Mode Current Consumption and Wakeup Time

The Wait mode configuration and measurements are defined as follows:

- Core clock and Master clock stopped
- Current measurement as shown below
- All peripheral clocks deactivated
- BOD disabled
- RTT enabled

Figure 58-7. Measurement Setup for Wait Mode



The following tables give current consumption and wakeup time(1) in Wait mode.

Table 58-15. Typical Current Consumption in Wait Mode

Wait Mode Consumption	Typical Value				Unit
	at 25°C		at 85°C	at 105°C	
	VDDIO = 3.3V		VDDIO = 3.3V	VDDIO = 3.3V	
Conditions	VDDOUT Consumption AMP1	Total Consumption AMP2	Total Consumption AMP2	Total Consumption AMP2	
No activity on the I/Os of the device	–	0.3	3.8	7.5	mA

Figure 58-11. Single-ended Mode AFE

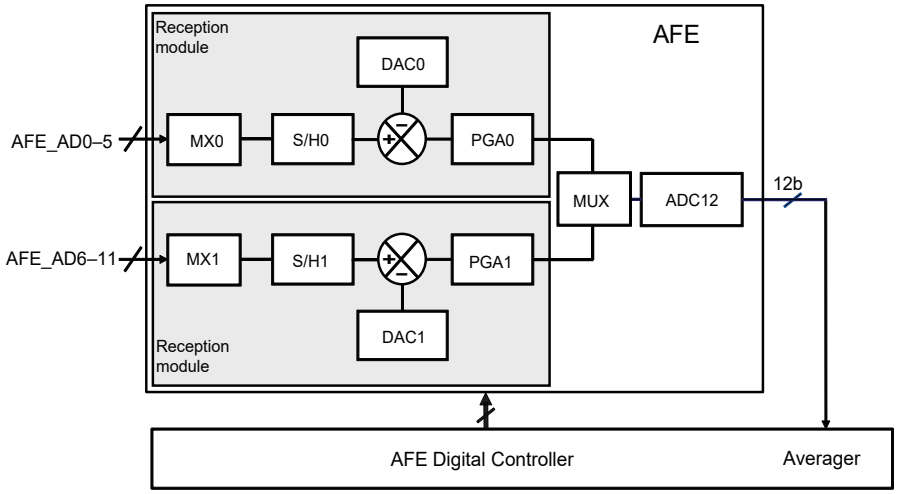
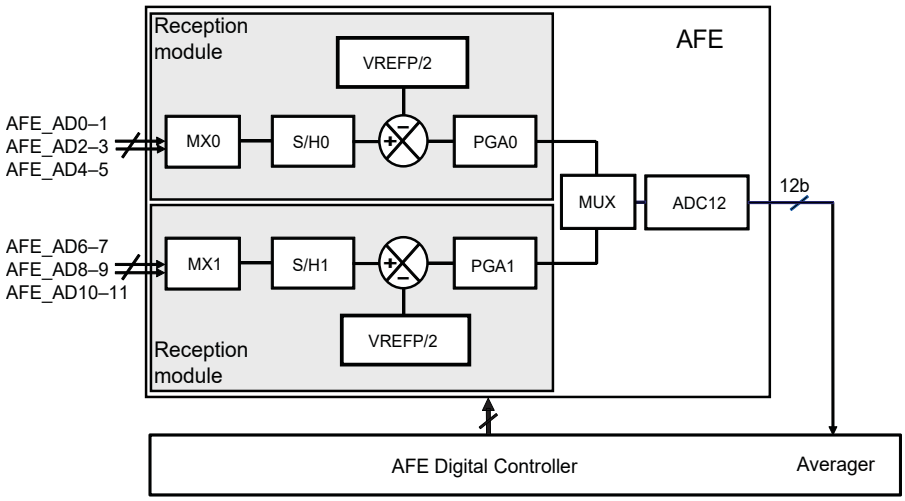


Figure 58-12. Differential Mode AFE



58.8.1 AFE Power Supply

58.8.1.1 Power Supply Characteristics

Table 58-29. Power Supply Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VDDIN}	Analog Current Consumption	Sleep mode (see **Note 2**)	–	2	–	µA
		Fast wake-up mode (see **Note 3**)		0.4		mA
		Normal mode, single sampling		3.4		mA
		Normal mode, dual sampling		4.2		mA
$I_{VDDCORE}$	Digital Current Consumption	Sleep mode (see **Note 2**)	-	1	-	µA
		Normal mode		80		

Note:

1. Current consumption is measured with AFEC_ACR.IBCTL=10.

- n depends on the expected accuracy
- R_{ON}= 2 kOhm

Table 59-39. Number of Tau:n

Resolution (bits)	12	13	14	15	16
RES	0	2	3	4	5
n	8	9	10	11	12

The AFEC already includes a tracking time of 15 $t_{AFE\ Clock}$.

59.8.6.2 AFE DAC Offset Compensation

Table 59-40. DAC Static Performances (see Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N	Resolution (see **Note 2**)	–	–	9	10	LSB
INL	Integral Non Linearity	–	-2.5	±0.7	2	LSB
DNL	Differential Non Linearity	–	-3	±0.5	1.8	LSB

Note:

1. DAC Offset is included in the AFE EO performances.
2. 10 bits LSB relative to V_{REFP} scale, LSB = V_{VREFP} / 210 = 2.93 mV, with V_{VREFP} = 3V.

59.9 Analog Comparator Characteristics

Table 59-41. Analog Comparator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IR}	Input Voltage Range	–	GND + 0.2	–	VDDIN - 0.2	V
V_{IO}	Input Offset Voltage	Comparator only	–	–	10	mV
I_{VDDIN}	Current Consumption (VDDIN)	Low-power option (ACC_ACR.ISEL = 0)	–	20	–	µA
		High-speed option (ACC_ACR.ISEL = 1)	–	120	–	
V_{hys}	Hysteresis	ACC_ACR.HYST = 1 or 2 ACC_ACR.ISEL = 0	–	20	–	mV
		ACC_ACR.HYST = 3 ACC_ACR.ISEL = 0	–	40	–	
		ACC_ACR.HYST = 1 or 2 ACC_ACR.ISEL = 1	–	25	–	mV
		ACC_ACR.HYST = 3 ACC_ACR.ISEL = 1	–	45	–	

Table 59-47. Static Performance Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
INL	Integral Non-linearity (see **Note 1**)	No R_{LOAD}	-10	±2	10	LSB
		C_{LOAD} = 50 pF				
		DACC_ACR.IBTLCHx = 3				
DNL	Differential Non-linearity (see **Note 1**)	No R_{LOAD}	-4	±2	4	LSB
		C_{LOAD} = 50 pF				
		DACC_ACR.IBTLCHx = 3				
E_O	Offset Error (see **Note 2**)	–	-8	1	8	mV
E_G	Gain Error	No R_{LOAD}	-1	–	1	%.FSR
		C_{LOAD} = 50 pF				
		DACC_ACR.IBTLCHx = 3				

Note:

1. Best-fit Curve from 0x080 to 0xF7F.
2. Difference between DACx at 0x800 and V_{VREFP}/2.

Table 59-48. Dynamic Performance Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{START}	Startup Time	From DAC on (CHER.CHx) to DAC ready to convert (CHSR.DACRDYx)	–	10	–	µs
t_S	Settling Time Code to Code; i.e., code(n-1) to code(n) ± 0.5 LSB	R_{LOAD} = 5 Kohm C_{LOAD} = 50 pF	–	0.5	–	µs
	Settling Time Full-scale; i.e., 0x000 to 0xFFF ±0.5 LSB	DACC_ACR.IBCTLCHx = 3 FS = 1 MSps	–	1	–	µs
Slew Rate		–	3	–	V/µs	

Table 59-49. Analog Outputs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{LOAD}	Output Resistor Load	Output load resistor	5	–	–	kOhm
C_{LOAD}	Output Capacitor Load	Output load capacitor	–	–	50	pF
V_{DACx_MIN}	Minimum Output Voltage on DACx	Code = 0x000 No R_{LOAD}, C_{LOAD} = 50 pF, DACC_ACR.IBCTLCHx =3	–	0.1	0.5	%. V_{VREFP}