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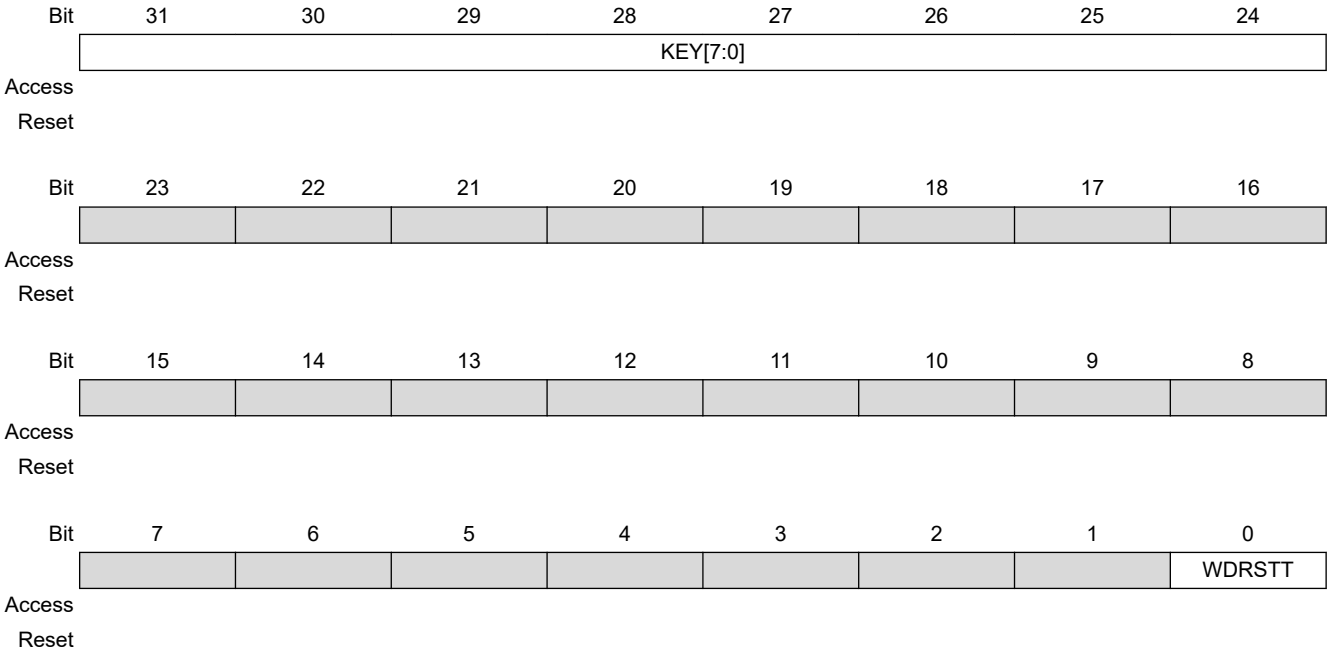
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv70n20b-cbt

25.5.1 Reinforced Safety Watchdog Timer Control Register

Name: RSWDT_CR
Offset: 0x00
Property: Write-only



Bits 31:24 – KEY[7:0] Password

Value	Name	Description
0xC4	PASSWD	Writing any other value in this field aborts the write operation.

Bit 0 – WDRSTT Watchdog Restart

Value	Description
0	No effect.
1	Restarts the watchdog.

30.4.1 Slow RC Oscillator (32 kHz typical)

By default, the Slow RC oscillator is enabled and selected as a source of SLCK.

Compared to the 32.768 kHz crystal oscillator, this oscillator offers a faster startup time and is less exposed to the external environment, as it is fully integrated. However, its output frequency is subject to larger variations with supply voltage, temperature and manufacturing process. Therefore, the user must take these variations into account when this oscillator is used as a time base (startup counter, frequency monitor, etc.). Refer to the section “Electrical Characteristics”.

This oscillator is disabled by clearing the SUPC_CR.XTALSEL.

Related Links

58. Electrical Characteristics for SAM V70/V71
59. Electrical Characteristics for SAM E70/S70

30.4.2 32.768 kHz Crystal Oscillator

By default, the 32.768 kHz oscillator is disabled. To use this oscillator, the XIN32 and XOUT32 pins must be connected to a 32.768 kHz crystal or to a ceramic resonator. Refer to the section “Electrical Characteristics” for appropriate loading capacitors selection on XIN32 and XOUT32.

Note that the user is not obliged to use the 32.768 kHz crystal oscillator and can use the Slow RC oscillator instead. Using the 32.768 kHz crystal oscillator provides a more accurate frequency than the Slow RC oscillator.

To select the 32.768 kHz crystal oscillator as the source of SLCK, the bit SUPC_CR.XTALSEL must be set. This results in a sequence which first configures the PIO lines multiplexed with XIN32 and XOUT32 to be driven by the crystal oscillator, then enables the 32.768 kHz crystal oscillator and then disables the Slow RC oscillator to save power. The switch of SLCK source is glitch-free.

Reverting to the Slow RC oscillator is only possible by shutting down the VDDIO power supply. If the user does not need the 32.768 kHz crystal oscillator, the XIN32 and XOUT32 pins can be left unconnected since by default the XIN32 and XOUT32 system I/O pins are in PIO input mode with pullup after reset.

The user can also set the 32.768 kHz crystal oscillator in Bypass mode instead of connecting a crystal. In this case, the user must provide the external clock signal on XIN32. For input characteristics of the XIN32 pin, refer to the section “Electrical Characteristics”. To enter Bypass mode, the OSCBYPASS bit of the Supply Controller Mode register (SUPC_MR) must be set prior to setting SUPC_CR.XTALSEL.

Related Links

58. Electrical Characteristics for SAM V70/V71
59. Electrical Characteristics for SAM E70/S70

30.5 Main Clock

The Main clock (MAINCK) has two sources:

- A Main RC oscillator (4/8/12 MHz) with a fast startup time and that is selected by default to start the system
- A Main crystal oscillator with Bypass mode

31.20.14 PMC Interrupt Enable Register

Name: PMC_IER
Offset: 0x0060
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			XT32KERR			CFDEV	MOSCRCS	MOSCSELS
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
		PCKRDY6	PCKRDY5	PCKRDY4	PCKRDY3	PCKRDY2	PCKRDY1	PCKRDY0
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		LOCKU			MCKRDY		LOCKA	MOSCXTS
Access								
Reset								

Bit 21 – XT32KERR 32.768 kHz Crystal Oscillator Error Interrupt Enable

Bit 18 – CFDEV Clock Failure Detector Event Interrupt Enable

Bit 17 – MOSCRCS Main RC Oscillator Status Interrupt Enable

Bit 16 – MOSCSELS Main Clock Source Oscillator Selection Status Interrupt Enable

Bits 8, 9, 10, 11, 12, 13, 14 – PCKRDY Programmable Clock Ready x Interrupt Enable

Bit 6 – LOCKU UTMI PLL Lock Interrupt Enable

Bit 3 – MCKRDY Master Clock Ready Interrupt Enable

Bit 1 – LOCKA PLLA Lock Interrupt Enable

Bit 0 – MOSCXTS Main Crystal Oscillator Status Interrupt Enable

Peripheral Name	Transfer Type	HW Interface Number (XDMAC_CC.PERID)
I2SC0	Receive Left	45
I2SC1	Transmit Left	46
I2SC1	Receive Left	47
I2SC0	Transmit Right	48
I2SC0	Receive Right	49
I2SC1	Transmit Right	50
I2SC1	Receive Right	51

36.5 Functional Description

36.5.1 Basic Definitions

Source Peripheral: Slave device, memory mapped on the interconnection network, from where the XDMAC reads data. The source peripheral teams up with a destination peripheral to form a channel. A data read operation is scheduled when the peripheral transfer request is asserted.

Destination Peripheral: Slave device, memory mapped on the interconnection network, to which the XDMAC writes. A write data operation is scheduled when the peripheral transfer request is asserted.

Channel: The data movement between source and destination creates a logical channel.

Transfer Type: The transfer is hardware-synchronized when it is paced by the peripheral hardware request, otherwise the transfer is self-triggered (memory to memory transfer).

36.5.2 Transfer Hierarchy Diagram

XDMAC Master Transfer: The Master Transfer is composed of a linked list of blocks. The channel address, control and configuration registers can be modified at the inter block boundary. The descriptor structure modifies the channel registers conditionally. Interrupts can be generated on a per block basis or when the end of linked list event occurs.

XDMAC Block: An XDMAC block is composed of a programmable number of microblocks. The channel configuration registers remain unchanged at the inter microblock boundary. The source and destination addresses are conditionally updated with a programmable signed number.

XDMAC Microblock: The microblock is composed of a programmable number of data. The channel configuration registers remain unchanged at the data boundary. The data address may be fixed (a FIFO location, a peripheral transmit or receive register), incrementing (a memory-mapped area) by a programmable signed number.

XDMAC Burst and Incomplete Burst: In order to improve the overall performance when accessing dynamic external memory, burst access is mandatory. Each data of the microblock is considered as a part of a memory burst. The programmable burst value indicates the largest memory burst allowed on a per channel basis. When the microblock length is not an integral multiple of the burst size, an incomplete burst is performed to read or write the last trailing bytes.

XDMAC Chunk and Incomplete Chunk: When a peripheral synchronized transfer is activated, the microblock splits into a number of data chunks. The chunk size is programmable. The larger the chunk is,

36.9.20 XDMAC Channel x Interrupt Mask Register [x = 0..23]

Name: XDMAC_CIM
Offset: 0x58 + n*0x40 [n=0..23]
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
Access		R	R	R	R	R	R	R
Reset		0	0	0	0	0	0	0

Bit 6 – ROIM Request Overflow Error Interrupt Mask Bit

Value	Description
0	Request overflow interrupt is masked.
1	Request overflow interrupt is activated.

Bit 5 – WBEIM Write Bus Error Interrupt Mask Bit

Value	Description
0	Bus error interrupt is masked.
1	Bus error interrupt is activated.

Bit 4 – RBEIM Read Bus Error Interrupt Mask Bit

Value	Description
0	Bus error interrupt is masked.
1	Bus error interrupt is activated.

Bit 3 – FIM End of Flush Interrupt Mask Bit

Value	Description
0	End of flush interrupt is masked.
1	End of flush interrupt is activated.

38.8.63 GMAC Pause Frames Received Register

Name: GMAC_PFR
Offset: 0x164
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PFRX[15:0] Pause Frames Received Register
This register counts the number of pause frames received without error.

38.8.71 GMAC Undersized Frames Received Register

Name: GMAC_UFR
Offset: 0x184
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
							UFRX[9:8]	
Access							R	R
Reset							0	0

Bit	7	6	5	4	3	2	1	0
	UFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 9:0 – UFRX[9:0] Undersize Frames Received
This bit field counts the number of frames received less than 64 bytes in length (10/100 mode, full duplex) that do not have either a CRC error or an alignment error.

Bit 5 – END_BF_ST End of Channel Buffer Status
Valid until the CHANN_ENB flag is cleared at the end of the next buffer transfer.

Value	Description
0	Cleared automatically when read by software.
1	Set by hardware when the BUFF_COUNT count-down reaches zero.

Bit 4 – END_TR_ST End of Channel Transfer Status
Valid until the CHANN_ENB flag is cleared at the end of the next buffer transfer.

Value	Description
0	Cleared automatically when read by software.
1	Set by hardware when the last packet transfer is complete, if the USBHS device has ended the transfer.

Bit 1 – CHANN_ACT Channel Active Status
When a packet transfer is ended, this bit is automatically reset.

When a packet transfer cannot be completed due to an END_BF_ST, this flag stays set during the next channel descriptor load (if any) and potentially until completion of a USBHS packet transfer, if allowed by the new descriptor.

Value	Description
0	The DMA channel is no longer trying to source the packet data.
1	The DMA channel is currently trying to source packet data, i.e., selected as the highest-priority requesting channel.

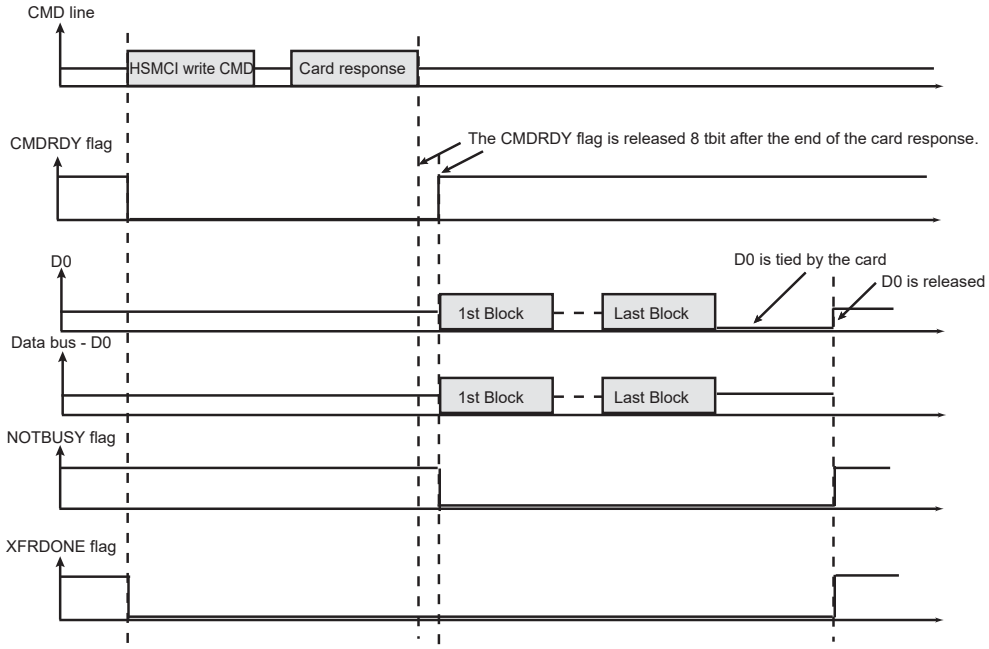
Bit 0 – CHANN_ENB Channel Enable Status
When any transfer is ended either due to an elapsed byte count or to completion of a USBHS device-initiated transfer, this bit is automatically reset.

This bit is normally set or cleared by writing into the USBHS_DEVDMACONTROLx.CHANN_ENB bit field either by software or descriptor loading.

If a channel request is currently serviced when the USBHS_DEVDMACONTROLx.CHANN_ENB bit is cleared, the DMA FIFO buffer is drained until it is empty, then this status bit is cleared.

Value	Description
0	If cleared, the DMA channel no longer transfers data, and may load the next descriptor if the USBHS_DEVDMACONTROLx.LDNXT_DSC bit is set.
1	If set, the DMA channel is currently enabled and transfers data upon request.

Figure 40-12. XFRDONE During a Write Access



40.13 Register Write Protection

To prevent any single software error from corrupting HSMCI behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the HSMCI Write Protection Mode Register (HSMCI_WPMR).

If a write access to a write-protected register is detected, the WPVS bit in the HSMCI Write Protection Status Register (HSMCI_WPSR) is set and the field WPVSRC indicates the register in which the write access has been attempted.

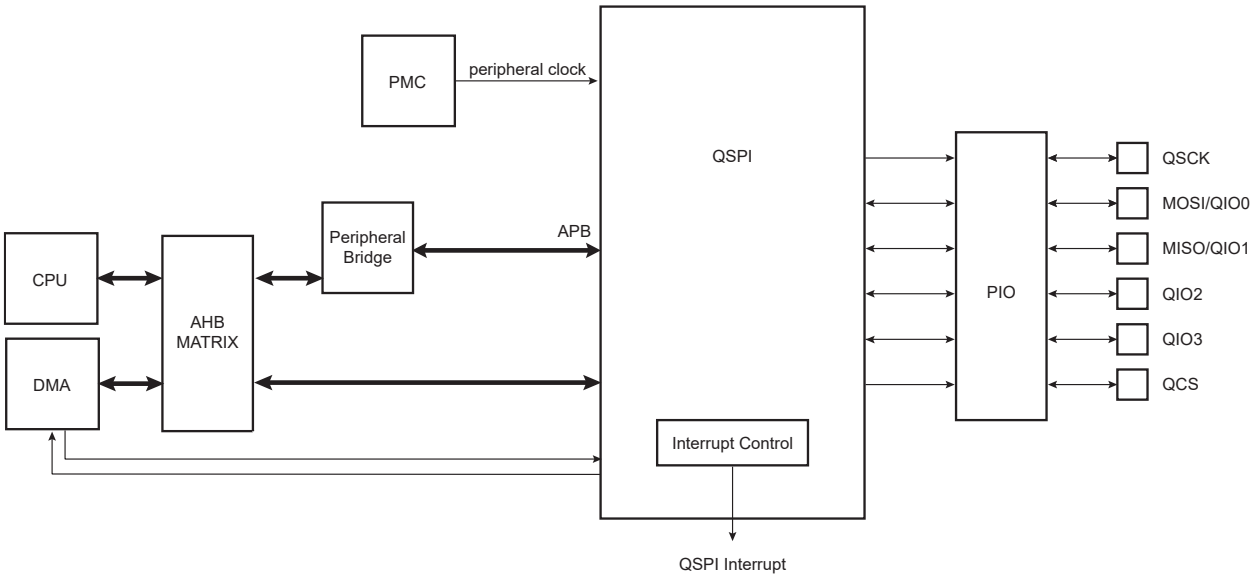
The WPVS bit is automatically cleared after reading the HSMCI_WPSR.

The following registers can be protected:

- HSMCI Mode Register
- HSMCI Data Timeout Register
- HSMCI SDCard/SDIO Register
- HSMCI Completion Signal Timeout Register
- HSMCI DMA Configuration Register
- HSMCI Configuration Register

42.3 Block Diagram

Figure 42-1. Block Diagram



42.4 Signal Description

Table 42-1. Signal Description

Pin Name	Pin Description	Type
QSCK	Serial Clock	Output
MOSI (QIO0) (1)(2)	Data Output (Data Input Output 0)	Output (Input/Output)
MISO (QIO1) (1)(2)	Data Input (Data Input Output 1)	Input (Input/Output)
QIO2 (3)	Data Input Output 2	Input/Output
QIO3 (3)	Data Input Output 3	Input/Output
QCS	Peripheral Chip Select	Output

Note:

1. MOSI and MISO are used for single-bit SPI operation.
2. QIO0–QIO1 are used for Dual SPI operation.
3. QIO0–QIO3 are used for Quad SPI operation.

42.5 Product Dependencies

42.5.1 I/O Lines

The pins used for interfacing the compliant external devices may be multiplexed with PIO lines. The programmer must first program the PIO controllers to assign the QSPI pins to their peripheral functions.

In this mode, the device never initiates and never completes the transmission (START, REPEATED_START and STOP conditions are always provided by the master).

43.6.5.2 Programming Slave Mode

The following fields must be programmed before entering Slave mode:

1. TWIHS_SMR.SADR: The slave device address is used in order to be accessed by master devices in Read or Write mode.
2. (Optional) TWIHS_SMR.MASK can be set to mask some SADR address bits and thus allow multiple address matching.
3. TWIHS_CR.MSDIS: Disables the Master mode.
4. TWIHS_CR.SVEN: Enables the Slave mode.

As the device receives the clock, values written in TWIHS_CWGR are ignored.

43.6.5.3 Receiving Data

After a START or REPEATED START condition is detected, and if the address sent by the master matches the slave address programmed in the SADR (Slave Address) field, the SVACC (Slave Access) flag is set and SVREAD (Slave Read) indicates the direction of the transfer.

SVACC remains high until a STOP condition or a REPEATED START is detected. When such a condition is detected, the EOSACC (End Of Slave Access) flag is set.

43.6.5.3.1 Read Sequence

In the case of a read sequence (SVREAD is high), the TWIHS transfers data written in the TWIHS_THR until a STOP condition or a REPEATED_START + an address different from SADR is detected. Note that at the end of the read sequence TXCOMP (Transmission Complete) flag is set and SVACC reset.

As soon as data is written in the TWIHS_THR, TXRDY (Transmit Holding Register Ready) flag is reset, and it is set when the internal shifter is empty and the sent data acknowledged or not. If the data is not acknowledged, the NACK flag is set.

Note that a STOP or a REPEATED START always follows a NACK.

To clear the TXRDY flag, first set TWIHS_CR.SVDIS, then set TWIHS_CR.SVEN.

See Read Access Ordered by a Master.

43.6.5.3.2 Write Sequence

In the case of a write sequence (SVREAD is low), the RXRDY (Receive Holding Register Ready) flag is set as soon as a character has been received in TWIHS_RHR. RXRDY is reset when reading TWIHS_RHR.

The TWIHS continues receiving data until a STOP condition or a REPEATED_START + an address different from SADR is detected. Note that at the end of the write sequence, the TXCOMP flag is set and SVACC is reset.

See Write Access Ordered by a Master.

43.6.5.3.3 Clock Stretching Sequence

If TWIHS_THR or TWIHS_RHR is not written/read in time, the TWIHS performs a clock stretching.

Clock stretching information is given by the SCLWS (Clock Wait State) bit.

See Clock Stretching in Read Mode and Clock Stretching in Write Mode.

Note: Clock stretching can be disabled by configuring the SCLWSDIS bit in TWIHS_SMR. In that case, the UNRE and OVRE flags indicate an underrun (when TWIHS_THR is not filled on time) or an overrun (when TWIHS_RHR is not read on time).

44.9 Register Summary

Note: Offsets 0x100–0x128 are reserved for PDC registers.

Offset	Name	Bit Pos.								
0x00	SSC_CR	7:0							RXDIS	RXEN
		15:8	SWRST						TXDIS	TXEN
		23:16								
		31:24								
0x04	SSC_CMR	7:0	DIV[7:0]							
		15:8					DIV[11:8]			
		23:16								
		31:24								
0x08 ... 0x0F	Reserved									
0x10	SSC_RCMR	7:0	CKG[1:0]		CKI	CKO[2:0]			CKS[1:0]	
		15:8				STOP	START[3:0]			
		23:16	STTDLY[7:0]							
		31:24	PERIOD[7:0]							
0x14	SSC_RFMR	7:0	MSBF		LOOP	DATLEN[4:0]				
		15:8					DATNB[3:0]			
		23:16		FSOS[2:0]			FSLEN[3:0]			
		31:24	FSLEN_EXT[3:0]							FSEDGE
0x18	SSC_TCMR	7:0	CKG[1:0]		CKI	CKO[2:0]			CKS[1:0]	
		15:8					START[3:0]			
		23:16	STTDLY[7:0]							
		31:24	PERIOD[7:0]							
0x1C	SSC_TFMR	7:0	MSBF		DATDEF	DATLEN[4:0]				
		15:8					DATNB[3:0]			
		23:16	FSDEN	FSOS[2:0]			FSLEN[3:0]			
		31:24	FSLEN_EXT[3:0]							FSEDGE
0x20	SSC_RHR	7:0	RDAT[7:0]							
		15:8	RDAT[15:8]							
		23:16	RDAT[23:16]							
		31:24	RDAT[31:24]							
0x24	SSC_THR	7:0	TDAT[7:0]							
		15:8	TDAT[15:8]							
		23:16	TDAT[23:16]							
		31:24	TDAT[31:24]							
0x28 ... 0x2F	Reserved									
0x30	SSC_RSHR	7:0	RSDAT[7:0]							
		15:8	RSDAT[15:8]							
		23:16								
		31:24								

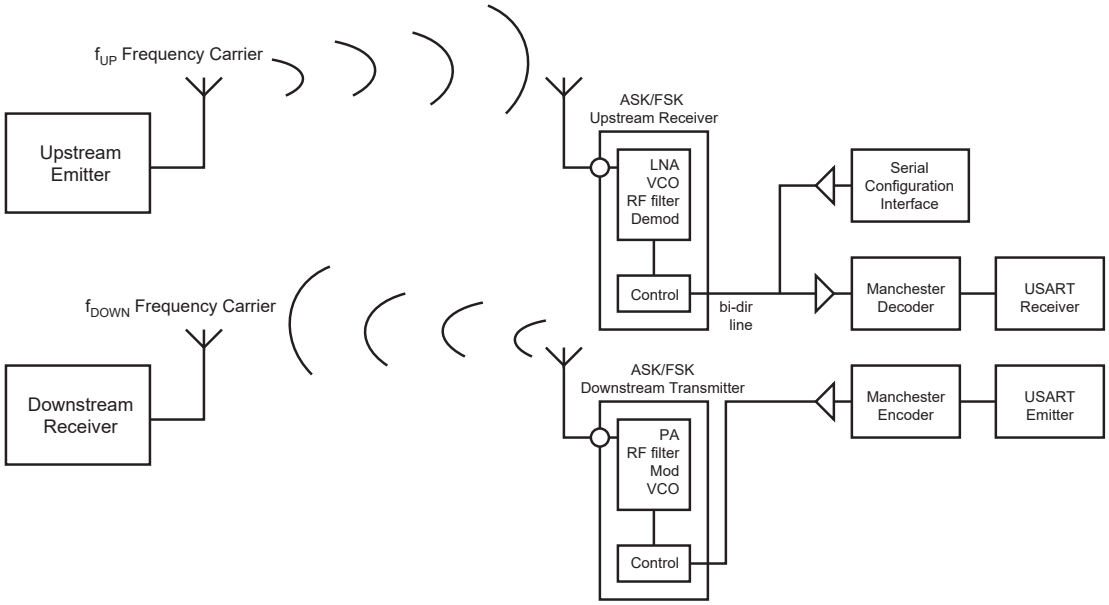
As the decoder is setup to be used in Unipolar mode, the first bit of the frame has to be a zero-to-one transition.

46.6.3.5 Radio Interface: Manchester Encoded USART Application

This section describes low data rate RF transmission systems and their integration with a Manchester encoded USART. These systems are based on transmitter and receiver ICs that support ASK and FSK modulation schemes.

The goal is to perform full duplex radio transmission of characters using two different frequency carriers. See the configuration in Figure 46-16.

Figure 46-16. Manchester Encoded Characters RF Transmission



The USART peripheral is configured as a Manchester encoder/decoder. Looking at the downstream communication channel, Manchester encoded characters are serially sent to the RF emitter. This may also include a user defined preamble and a start frame delimiter. Mostly, preamble is used in the RF receiver to distinguish between a valid data from a transmitter and signals due to noise. The Manchester stream is then modulated. See Figure 46-17 for an example of ASK modulation scheme. When a logic one is sent to the ASK modulator, the power amplifier, referred to as PA, is enabled and transmits an RF signal at downstream frequency. When a logic zero is transmitted, the RF signal is turned off. If the FSK modulator is activated, two different frequencies are used to transmit data. When a logic one is sent, the modulator outputs an RF signal at frequency F0 and switches to F1 if the data sent is a zero. See Figure 46-18.

From the receiver side, another carrier frequency is used. The RF receiver performs a bit check operation examining demodulated data stream. If a valid pattern is detected, the receiver switches to Receiving mode. The demodulated stream is sent to the Manchester decoder. Because of bit checking inside RF IC, the data transferred to the microcontroller is reduced by a user-defined number of bits. The Manchester preamble length is to be defined in accordance with the RF IC configuration.

Value	Description
0	The USART does not filter the receive line.
1	The USART filters the receive line using a three-sample filter (1/16-bit clock) (2 over 3 majority).

Bits 26:24 – MAX_ITERATION[2:0] Maximum Number of Automatic Iteration

Value	Description
0-7	Defines the maximum number of iterations in ISO7816 mode, protocol T = 0.

Bit 23 – INVDATA Inverted Data

Value	Description
0	The data field transmitted on TXD line is the same as the one written in US_THR or the content read in US_RHR is the same as RXD line. Normal mode of operation.
1	The data field transmitted on TXD line is inverted (voltage polarity only) compared to the value written on US_THR or the content read in US_RHR is inverted compared to what is received on RXD line (or ISO7816 IO line). Inverted mode of operation, useful for contactless card application. To be used with configuration bit MSBF.

Bit 22 – VAR_SYNC Variable Synchronization of Command/Data Sync Start Frame Delimiter

Value	Description
0	User defined configuration of command or data sync field depending on MODSYNC value.
1	The sync field is updated when a character is written into US_THR.

Bit 21 – DSNACK Disable Successive NACK

Value	Description
0	NACK is sent on the ISO line as soon as a parity error occurs in the received character (unless INACK is set).
1	Successive parity errors are counted up to the value specified in the MAX_ITERATION field. These parity errors generate a NACK on the ISO line. As soon as this value is reached, no additional NACK is sent on the ISO line. The flag ITER is asserted. Note: MAX_ITERATION field must be set to 0 if DSNACK is cleared.

Bit 20 – INACK Inhibit Non Acknowledge

Value	Description
0	The NACK is generated.
1	The NACK is not generated.

Bit 19 – OVER Oversampling Mode

Value	Description
0	16X Oversampling
1	8X Oversampling

Bit 18 – CLKO Clock Output Select

48.7.1 MediaLB Control 0 Register

Name: MLB_MLBC0
Offset: 0x000
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset							0	0

Bit	15	14	13	12	11	10	9	8
Access								
Reset	0	0		0				

Bit	7	6	5	4	3	2	1	0
Access								
Reset	0		0	0	0	0		0

Bits 17:15 – FCNT[2:0] The number of frames per sub-buffer for synchronous channels

Value	Name	Description
0	1_FRAME	1 frame per sub-buffer (Operation is the same as Standard mode.)
1	2_FRAMES	2 frames per sub-buffer
2	4_FRAMES	4 frames per sub-buffer
3	8_FRAMES	8 frames per sub-buffer
4	16_FRAMES	16 frames per sub-buffer
5	32_FRAMES	32 frames per sub-buffer
6	64_FRAMES	64 frames per sub-buffer

Bit 14 – CTLRETRY Control Tx Packet Retry

Value	Description
0	A control packet that is flagged with a Break or ProtocolError by the receiver is skipped.
1	A control packet that is flagged with a Break or ProtocolError by the receiver is retransmitted.

Bit 12 – ASYRETRY Asynchronous Tx Packet Retry

Figure 50-8. WAVSEL = 00 without Trigger

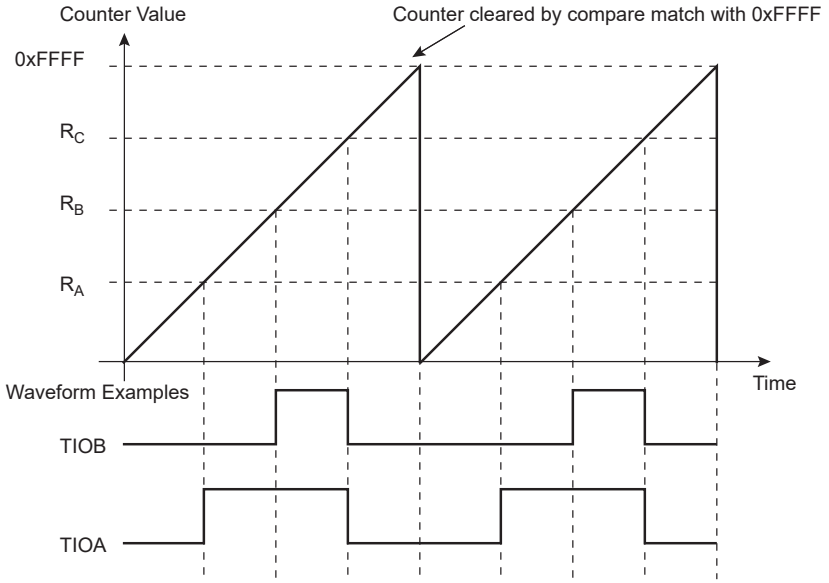
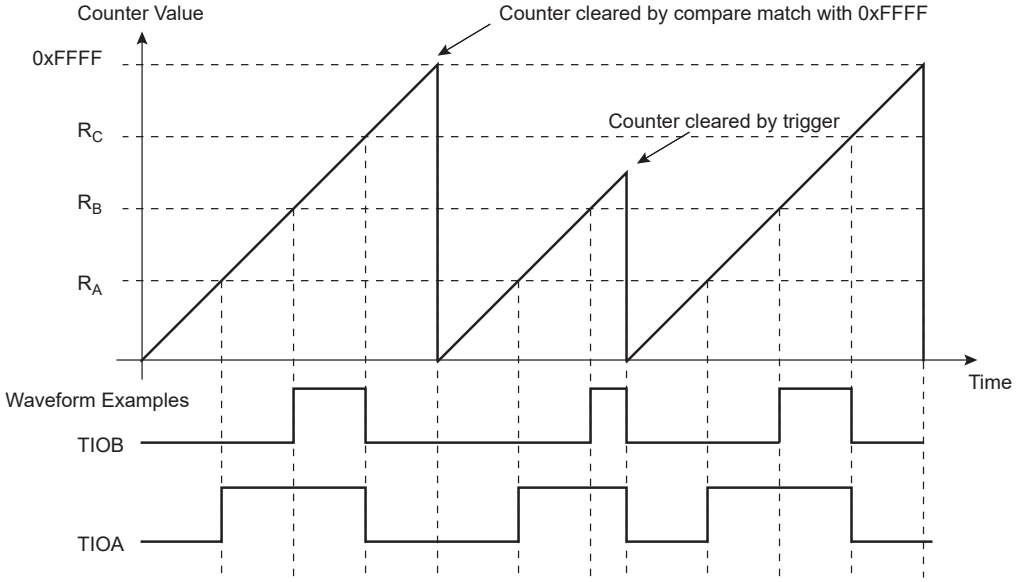


Figure 50-9. WAVSEL = 00 with Trigger



50.6.12.2 WAVSEL = 10

When WAVSEL = 10, the value of TC_CV is incremented from 0 to the value of RC, then automatically reset on a RC Compare. Once the value of TC_CV has been reset, it is then incremented and so on.

It is important to note that TC_CV can be reset at any time by an external event or a software trigger if both are programmed correctly.

Refer to the figures below.

In addition, RC Compare can stop the counter clock (CPCSTOP = 1 in TC_CMR) and/or disable the counter clock (CPCDIS = 1 in TC_CMR).

51.7.17 PWM Interrupt Status Register 2

Name: PWM_ISR2
Offset: 0x40
Reset: 0x00000000
Property: Read-only

Reading PWM_ISR2 automatically clears flags WRDY, UNRE and CMPSx.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CMPU7	CMPU6	CMPU5	CMPU4	CMPU3	CMPU2	CMPU1	CMPU0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CMPM7	CMPM6	CMPM5	CMPM4	CMPM3	CMPM2	CMPM1	CMPM0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
					UNRE			WRDY
Access					R			R
Reset					0			0

Bits 16, 17, 18, 19, 20, 21, 22, 23 – CMPUx Comparison x Update

Value	Description
0	The comparison x has not been updated since the last read of the PWM_ISR2 register.
1	The comparison x has been updated at least one time since the last read of the PWM_ISR2 register.

Bits 8, 9, 10, 11, 12, 13, 14, 15 – CMPMx Comparison x Match

Value	Description
0	The comparison x has not matched since the last read of the PWM_ISR2 register.
1	The comparison x has matched at least one time since the last read of the PWM_ISR2 register.

Bit 3 – UNRE Synchronous Channels Update Underrun Error

Value	Description
0	No Synchronous Channels Update Underrun has occurred since the last read of the PWM_ISR2 register.
1	At least one Synchronous Channels Update Underrun has occurred since the last read of the PWM_ISR2 register.

In Bypass mode, the maximum sample rate and the power consumption of the DAC are lowered.

53.6.2 Conversion Results

When a conversion is completed, the resulting analog value is available at the selected DAC channel output. The EOC bit in the DACC Interrupt Status Register (DACC_ISR) is set.

Reading DACC_ISR clears the EOC bit.

53.6.3 Analog Output Mode Selection

The analog outputs can be set to either Single-ended or Differential mode with the DIFF bit in the DACC_MR.

When set to Single-ended mode (DIFF = 0), each DAC channel can be configured independently.

When set to Differential mode (DIFF = 1), the analog outputs DACP and DACN are located on DAC0 and DAC1 outputs, respectively. All operations are driven by channel 0 and activating this channel automatically activates channel 1. Sending a value on channel 0 (DACP) automatically generates the complementary signal to be sent to channel 1 (DACN). The signal sent to the DAC is centered around 2048. For example, sending 3000 = 2048 + 952 to the DAC0 channel will automatically send 1096 = 2048 - 952 to the DAC1 channel.

53.6.4 Conversion Modes

The conversion modes available in the DACC are described below.

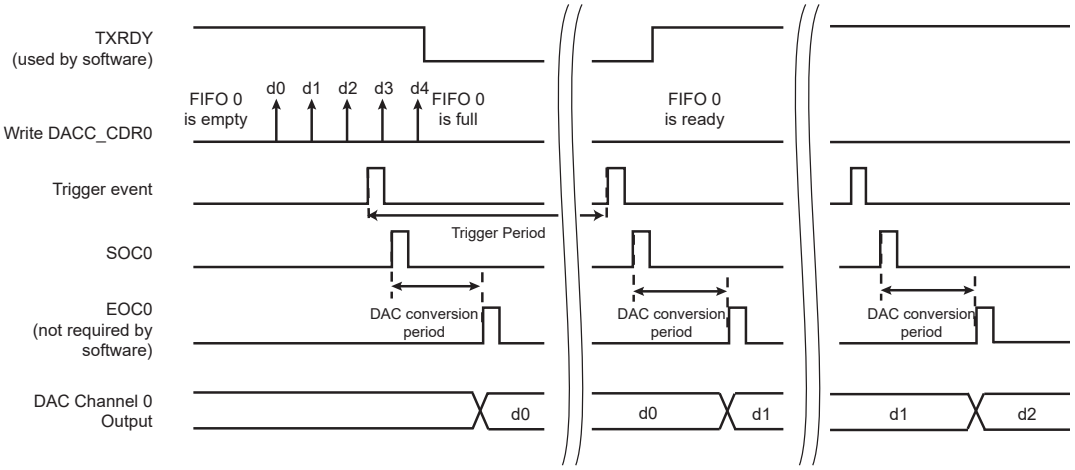
53.6.4.1 Trigger Mode

Trigger mode is enabled by setting DACC_TRIGR.TRGENx.

The conversion waits for a rising edge on the selected trigger to send the data to the DAC. In this mode, the maximum data rate (i.e., the maximum trigger event frequency) cannot exceed 12 DAC clock periods plus 2 cycles of resynchronization stage.

Note: Disabling Trigger mode (TRGENx = 0) automatically sets the DACC in Free-running or Max speed mode depending on the status of DACC_MR.MAXSx.

Figure 53-2. Conversion Sequence in Trigger Mode



53.6.4.2 Free-Running Mode

Free-running mode is enabled by clearing DACC_TRIGR.TRGENx and DACC_MR.MAXSx.

The conversion starts as soon as at least one channel is enabled. Once data is written in the DACC Conversion Data Register (DACC_CDRx), 12 DAC clock periods later, the converted data is available at

60. Schematic Checklist

The schematic checklist provides the user with the requirements regarding the different pin connections that must be considered before starting any new board design. It also provides information on the minimum hardware resources required to quickly develop an application with the SAM E70/S70/V70/V71 device. It does not consider PCB layout constraints.

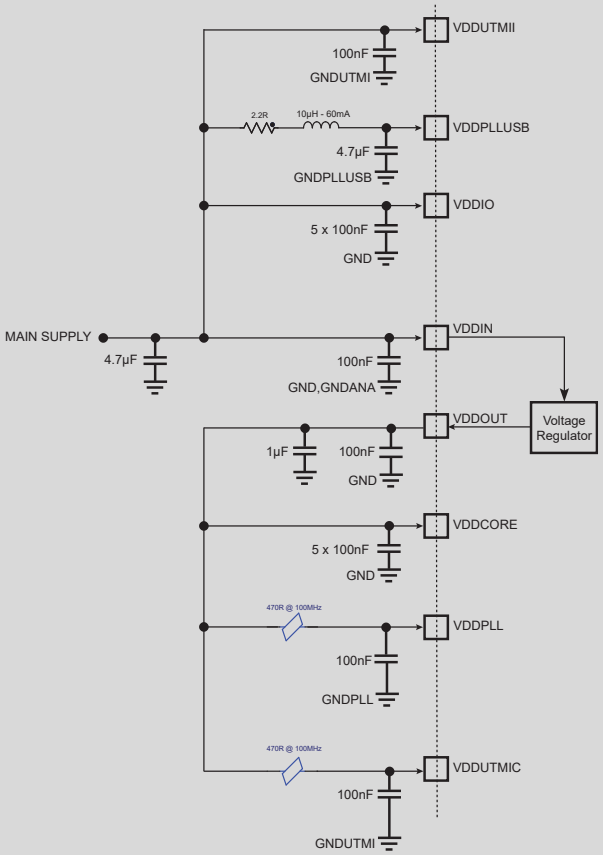
This information is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible. The checklist contains a column for use by designers, making it easy to track and verify each line item.

60.1 Power Supplies

60.1.1 Supplying the Device With Only One Supply

⚠ CAUTION To guarantee reliable operation of the device, the board design must comply with powerup and powerdown sequence guidelines provided in the "Power Considerations" chapter.

Power Supplies Schematic Example with Internal Regulator Use



Note: Component values are given only as a typical example.

Note:

Date	Changes
	Updated Figure 35-5, “NAND Flash Signal Multiplexing on SMC Pins” and added Note 1 below the figure. Section 35.10 “Scrambling/Unscrambling Function”: added details on access for SMC_KEY1 and SMC_KEY2 registers. In Table 35-10 “Register Mapping” and register table sections: SMC OCMS Mode Register now ”“SMC Off-Chip Memory Scrambling Register”. SMC OCMS Key1 Register now ”“SMC Off-Chip Memory Scrambling Key1 Register”. SMC OCMS Key2 Register now “SMC Off-Chip Memory Scrambling Key2 Register”. Section 35.16.5 “SMC Off-Chip Memory Scrambling Register”: corrected bits 8 to 11 to ‘CSxSE’ (were reserved). Section 35.16.6 “SMC Off-Chip Memory Scrambling Key1 Register” and Section 35.16.7 “SMC Off-Chip Memory Scrambling Key2 Register”: added Note (1) to clarify Write-once access.
	Section 36. “DMA Controller (XDMAC)” Updated TC peripheral names and added I2SC in Table 36-1 “Peripheral Hardware Requests”. Section 36.2 “Embedded Characteristics”: added FIFO size. Updated Figure 36-1, “DMA Controller (XDMAC) Block Diagram”. Section 36.5.4.1 “Single Block With Single Microblock Transfer”: in Step 6, deleted sub-step to activate a secure channel. Table 36-3 “Register Mapping“: corrected access of XDMAC_GTYPE, XDMAC_GWAC, XDMAC_CIM. Section 36.9.6 “XDMAC Global Interrupt Mask Register”: corrected access to Read-only. Section 36.9.28 “XDMAC Channel x [x = 0..23] Configuration Register”: bit 5 now reserved (was PROT). Deleted PROT bit description. Updated PERIF field description. Modified INITD bit description.
	Section 38. “USB High-Speed Interface (USBHS)” Table 38-1 “Description of USB Pipes/Endpoints”: corrected value in ‘High Bandwidth’ column for Pipe/Endpoint 1. Added Section 38.4.1 “I/O Lines”. Updated Figure 38-2, “General States”. Updated Section 38.5.3.3 “Device Detection” and added Note on VBUS supply. Section 38.6.1 “General Control Register”: added bit 8, VBUSHWC. Section 38.6.4 “General Status Set Register”: added bit 9, VBUSRQS. Section 38.6.12 “Device Endpoint Register”: bit 9 changed from ‘reserved’ to EPEN9. Bit 25 changed from ‘reserved’ to EPRST9. Bits 10 and 11 now reserved in registers: