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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv70q19b-cb

15. ARM Cortex-M7 (ARM)

Refer to ARM reference documents *Cortex-M7 Processor User Guide* (ARM DUI 0644) and *Cortex-M7 Technical Reference Manual* (ARM DDI 0489), available on www.arm.com.

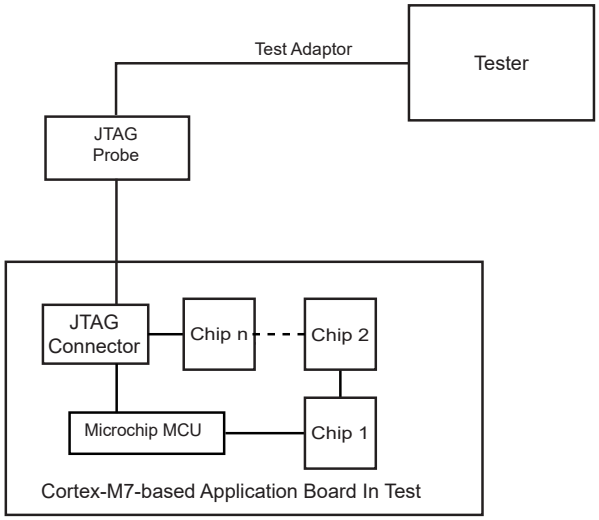
15.1 ARM Cortex-M7 Configuration

The following table provides the configuration for the ARM Cortex-M7 processor in SAM E70/S70/V70/V71 devices.

Table 15-1. ARM Cortex-M7 Configuration

Features	Configuration
Debug	
Comparator set	Full comparator set: 4 DWT and 8 FPB comparators
ETM support	Instruction ETM interface
Internal Trace support (ITM)	ITM and DWT trace functionality implemented
CTI and WIC	Not embedded
TCM	
ITCM max size	128 KB
DTCM max size	256 KB
Cache	
Cache size	16 KB for instruction cache, 16 KB for data cache
Number of sets	256 for instruction cache, 128 for data cache
Number of ways	2 for instruction cache, 4 for data cache
Number of words per cache line	8 words (32 bytes)
ECC on Cache	Embedded
NVIC	
IRQ number	74
IRQ priority levels	8
MPU	
Number of regions	16
FPU	
FPU precision	Single and double precision
AHB Port	
AHBP addressing size	512 MB

Figure 16-3. Application Test Environment Example



16.7 Functional Description

16.7.1 Test Pin

The TST pin is used for JTAG Boundary Scan Manufacturing Test or Fast Flash Programming mode. The TST pin integrates a permanent pulldown resistor of about 15 kΩ to GND, so that it can be left unconnected for normal operations. To enable Fast Flash Programming mode, refer to 18. Fast Flash Programming Interface (FFPI).

16.7.2 Debug Architecture

Figure 16-4 shows the debug architecture used. The Cortex-M7 embeds six functional units for debug:

- Serial Wire Debug Port (SW-DP) debug access
- FPB (Flash Patch Breakpoint)
- DWT (Data Watchpoint and Trace)
- ITM (Instrumentation Trace Macrocell)
- 6-pin Embedded Trace Macrocell (ETM) for instruction trace stream, including CoreSight Trace Port Interface Unit (TPIU)
- IEEE1149.1 JTAG Boundary scan on all digital pins

The debug architecture information that follows is mainly dedicated to developers of SW-DP Emulators/ Probes and debugging tool vendors for Cortex-M7-based microcontrollers. For further details on SW-DP, see the Cortex - M7 Technical Reference Manual.

31.20.34 PMC SleepWalking Activity Status Register 0

Name: PMC_SLPWK_ASR0
Offset: 0x0120
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	PID31	PID30	PID29	PID28	PID27	PID26	PID25	PID24
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PID23	PID22	PID21	PID20	PID19	PID18	PID17	PID16
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PID7							
Access								
Reset	0							

Bits 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – PIDx
Peripheral x Activity Status
Only the following PIDs can be configured with asynchronous partial wake-up: UARTx and TWIHSx.
All other PIDs are always read at ‘0’.

Value	Description
0	The peripheral x is not currently active. The asynchronous partial wake-up (SleepWalking) function can be activated.
1	The peripheral x is currently active. The asynchronous partial wake-up (SleepWalking) function must not be activated. **Note:** “PIDx” refers to identifiers as defined in the section “Peripheral Identifiers”.

32.6.1.42 PIO Falling Edge/Low-Level Select Register

Name: PIO_FELLSR
Offset: 0x00D0
Property: Write-only

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Falling Edge/Low-Level Interrupt Selection

Value	Description
0	No effect.
1	The interrupt source is set to a falling edge detection or low-level detection event, depending on PIO_ELSR.

34.7.7 SDRAMC Interrupt Mask Register

Name: SDRAMC_IMR
Offset: 0x1C
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								RES
Access								R
Reset								0

Bit 0 – RES Refresh Error Interrupt Mask

Value	Description
0	The refresh error interrupt is disabled.
1	The refresh error interrupt is enabled.

36. DMA Controller (XDMAC)

36.1 Description

The DMA Controller (XDMAC) is a AHB-protocol central direct memory access controller. It performs peripheral data transfer and memory move operations over one or two bus ports through the unidirectional communication channel. Each channel is fully programmable and provides both peripheral or memory-to-memory transfers. The channel features are configurable at implementation.

36.2 Embedded Characteristics

- 2 AHB Master Interfaces
- 24 DMA Channels
- 43 Hardware Requests
- 3.1 Kbytes Embedded FIFO
- Supports Peripheral-to-Memory, Memory-to-Peripheral, or Memory-to-Memory Transfer Operations
- Peripheral DMA Operation Runs on Bytes (8-bit), Half-Word (16-bit) and Word (32-bit)
- Memory DMA Operation Runs on Bytes (8 bit), Half-Word (16-bit) and Word (32 -bit)
- Supports Hardware and Software Initiated Transfers
- Supports Linked List Operations
- Supports Incrementing or Fixed Addressing Mode
- Supports Programmable Independent Data Striding for Source and Destination
- Supports Programmable Independent Microblock Striding for Source and Destination
- Configurable Priority Group and Arbitration Policy
- Programmable AHB Burst Length
- Configuration Interface Accessible through APB Interface
- XDMAC Architecture Includes Multiport FIFO
- Supports Multiple View Channel Descriptor
- Automatic Flush of Channel Trailing Bytes
- Automatic Coarse-Grain and Fine-Grain Clock Gating
- Hardware Acceleration of Memset Pattern

36.9.8 XDMAC Global Channel Enable Register

Name: XDMAC_GE
Offset: 0x1C
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	EN23	EN22	EN21	EN20	EN19	EN18	EN17	EN16
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bit	15	14	13	12	11	10	9	8
	EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bit	7	6	5	4	3	2	1	0
	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 – EN XDMAC Channel x Enable

Value	Description
0	This bit has no effect.
1	Enables channel n. This operation is permitted if the Channel x Status bit (XDMAC_GS.STx) was read as '0'.

- Set ISI_DMA_C_CTRL.C_FETCH.
- Configure ISI_DMA_C_DSCR.C_DSCR with the descriptor address.
- Write a one to the bit ISI_DMA_CHER.C_CH_EN.

Table 37-11. Memory Mapping for 8-bit Grayscale Mode

31	30	29	28	27	26	25	24
Pixel 3							
23	22	21	20	19	18	17	16
Pixel 2							
15	14	13	12	11	10	9	8
Pixel 1							
7	6	5	4	3	2	1	0
Pixel 0							

37.5.4.4 FIFO and DMA Features

Both preview and codec datapaths contain FIFOs. These asynchronous buffers are used to safely transfer formatted pixels from the pixel clock domain to the AHB clock domain. A video arbiter is used to manage FIFO thresholds and triggers a relevant DMA request through the AHB master interface. Thus, depending on the FIFO state, a specified length burst is asserted. Regarding AHB master interface, it supports Scatter DMA mode through linked list operation. This mode of operation improves flexibility of image buffer location and allows the user to allocate two or more frame buffers. The destination frame buffers are defined by a series of Frame Buffer Descriptors (FBD). Each FBD controls the transfer of one entire frame and then optionally loads a further FBD to switch the DMA operation at another frame buffer address. The FBD is defined by a series of three words. The first word defines the current frame buffer address (named DMA_X_ADDR register), the second defines control information (named DMA_X_CTRL register) and the third defines the next descriptor address (named DMA_X_DSCR). DMA Transfer mode with linked list support is available for both codec and preview datapaths. The data to be transferred described by an FBD requires several burst accesses. In the following example, the use of two ping-pong frame buffers is described.

Example:

The first FBD, stored at address 0x00030000, defines the location of the first frame buffer. This address is programmed in the ISI user interface DMA_P_DSCR. To enable the descriptor fetch operation, the value 0x00000001 must be written to the DMA_P_CTRL register. LLI_0 and LLI_1 are the two descriptors of the linked list.

Destination address: frame buffer ID0 0x02A000 (LLI_0.DMA_P_ADDR)

Transfer 0 Control Information, fetch and writeback: 0x00000003 (LLI_0.DMA_P_CTRL)

Next FBD address: 0x00030010 (LLI_0.DMA_P_DSCR)

The second FBD, stored at address 0x00030010, defines the location of the second frame buffer.

Destination address: frame buffer ID1 0x0003A000 (LLI_1.DMA_P_ADDR)

Transfer 1 Control information fetch and writeback: 0x00000003 (LLI_1.DMA_P_CTRL)

The third FBD address: 0x00030000, wrapping to first FBD (LLI_1.DMA_P_DSCR)

38.8.65 GMAC 65 to 127 Byte Frames Received Register

Name: GMAC_TBFR127
Offset: 0x16C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	NFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFRX[31:0] 65 to 127 Byte Frames Received without Error
This bit field counts the number of 65 to 127 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

38.8.101 GMAC Interrupt Status Register Priority Queue x

Name: GMAC_ISRPQx
Offset: 0x0400 + x*0x04 [x=0..4]
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					HRESP	ROVR		
Access								
Reset					0	0		

Bit	7	6	5	4	3	2	1	0
	TCOMP	TFC	RLEX			RXUBR	RCOMP	
Access								
Reset	0	0	0			0	0	

Bit 11 – HRESP HRESP Not OK

Bit 10 – ROVR Receive Overrun

Bit 7 – TCOMP Transmit Complete

Bit 6 – TFC Transmit Frame Corruption Due to AHB Error
Transmit frame corruption due to AHB error—set if an error occurs whilst midway through reading transmit frame from the AHB, including HRESP errors and buffers exhausted mid frame.

Bit 5 – RLEX Retry Limit Exceeded or Late Collision

Bit 2 – RXUBR RX Used Bit Read

Bit 1 – RCOMP Receive Complete

39.6.27 Device DMA Channel x Next Descriptor Address Register

Name: USBHS_DEVDMANXTDSCx
Offset: 0x0300 + x*0x10 [x=0..6]
Reset: 0
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	NXT_DSC_ADD[31:24]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NXT_DSC_ADD[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NXT_DSC_ADD[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NXT_DSC_ADD[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NXT_DSC_ADD[31:0] Next Descriptor Address
This field points to the next channel descriptor to be processed. This channel descriptor must be aligned, so bits 0 to 3 of the address must be equal to zero.

40.8.2 Data Transfer Operation

The High Speed MultiMedia Card allows several read/write operations (single block, multiple blocks, stream, etc.). These kinds of transfer can be selected setting the Transfer Type (TRTYP) field in the HSMCI Command Register (HSMCI_CMDR).

In all cases, the block length (BLKLEN field) must be defined either in the HSMCI Mode Register (HSMCI_MR) or in the HSMCI Block Register (HSMCI_BLKR). This field determines the size of the data block.

Consequent to MMC Specification 3.1, two types of multiple block read (or write) transactions are defined (the host can use either one at any time):

- Open-ended/Infinite Multiple block read (or write):
  The number of blocks for the read (or write) multiple block operation is not defined. The card will continuously transfer (or program) data blocks until a stop transmission command is received.
- Multiple block read (or write) with predefined block count (since version 3.1 and higher):
  The card will transfer (or program) the requested number of data blocks and terminate the transaction. The stop command is not required at the end of this type of multiple block read (or write), unless terminated with an error. In order to start a multiple block read (or write) with predefined block count, the host must correctly program the HSMCI Block Register (HSMCI_BLKR). Otherwise the card will start an open-ended multiple block read. The BCNT field of the HSMCI_BLKR defines the number of blocks to transfer (from 1 to 65535 blocks). Programming the value 0 in the BCNT field corresponds to an infinite block transfer.

40.8.3 Read Operation

The following flowchart shows how to read a single block with or without use of DMAC facilities. In this example, a polling method is used to wait for the end of read. Similarly, the user can configure the HSMCI Interrupt Enable Register (HSMCI_IER) to trigger an interrupt at the end of read.

44.9.4 SSC Receive Frame Mode Register

Name: SSC_RFMR
Offset: 0x14
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the SSC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	FSLEN_EXT[3:0]							FSEDGE
Access	R/W	R/W	R/W	R/W				R/W
Reset	0	0	0	0				0

Bit	23	22	21	20	19	18	17	16
		FSOS[2:0]			FSLEN[3:0]			
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
					DATNB[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MSBF		LOOP	DATLEN[4:0]				
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W
Reset	0		0	0	0	0	0	0

Bits 31:28 – FSLEN_EXT[3:0] FSLEN Field Extension
Extends FSLEN field. For details, see FSLEN: Receive Frame Sync Length.

Bit 24 – FSEDGE Frame Sync Edge Detection
Determines which edge on Frame Sync will generate the interrupt RXSYN in the SSC Status Register.

Value	Name	Description
0	POSITIVE	Positive Edge Detection
1	NEGATIVE	Negative Edge Detection

Bits 22:20 – FSOS[2:0] Receive Frame Sync Output Selection

Value	Name	Description
0	NONE	None, RF pin is an input
1	NEGATIVE	Negative Pulse, RF pin is an output
2	POSITIVE	Positive Pulse, RF pin is an output
3	LOW	Driven Low during data transfer, RF pin is an output
4	HIGH	Driven High during data transfer, RF pin is an output
5	TOGGLING	Toggling at each start of data transfer, RF pin is an output

Table 48-5. MediaLB RxStatus Responses

Value (see Note)	Command	Description
Normal Commands (TX Device sends in non-system channels):		
00h	NoData	No data to send out in this physical channel.
02h...0Eh	rsvd	Reserved
10h	SyncData	Tx Device sends out SyncData command to indicate synchronous stream data.
12h...1Eh	rsvd	Reserved
20h	AsyncStart	Asynchronous logical channel. Start of a packet.
22h	AsyncContinue	Asynchronous logical channel. Middle of a packet.
24h	AsyncEnd	Asynchronous logical channel. End of a packet.
26h	AsyncBreak	Asynchronous logical channel. Indicates a packet stop. No valid data present on the MLBD line.
28h...2Eh	rsvd	Reserved
30h	ControlStart	Control logical channel. Start of a message.
32h	ControlContinue	Control logical channel. Middle of a message.
34h	ControlEnd	Control logical channel. End of a message.
36h	ControlBreak	Control logical channel. Indicates a message stop. No valid data present on the MLBD line.
38h...3Eh	rsvd	Reserved
40h	IsoNoData	Isochronous logical channel, no data valid.
42h	Iso1Byte	Isochronous logical channel, one data byte valid. First byte (MSB) transmitted/received is valid. Last three bytes in physical channel are empty.
44h	Iso2Bytes	Isochronous logical channel, first two data bytes valid. First byte transmitted/received is the MSB. Last two bytes in physical channel are empty.
46h	Iso3Bytes	Isochronous logical channel, first three data bytes valid. First byte transmitted/received is the MSB. Last byte in physical channel is empty.
48h	Iso4Bytes	Isochronous logical channel, all four data bytes valid. First byte transmitted/received is the MSB.
4Ah...4Eh	rsvd	Reserved
50h	IsoSync1Byte	Isochronous logical channel, one data byte valid and start of a block. First byte transmitted/received is valid. Last three bytes in physical channel are empty.

50.7.2 TC Channel Mode Register: Capture Mode

Name: TC_CMRx
Offset: 0x04 + x*0x40 [x=0..2]
Reset: 0x00000000
Property: Read/Write

This register can be written only if the WPEN bit is cleared in the TC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
		SBSMPLR[2:0]			LDRB[1:0]		LDRA[1:0]	
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	WAVE	CPCTRG				ABETRG	ETRGEDG[1:0]	
Access	R/W	R/W				R/W	R/W	R/W
Reset	0	0				0	0	0

Bit	7	6	5	4	3	2	1	0
	LDBDIS	LDBSTOP	BURST[1:0]		CLKI	TCCLKS[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 22:20 – SBSMPLR[2:0] Loading Edge Subsampling Ratio

Value	Name	Description
0	ONE	Load a Capture register each selected edge.
1	HALF	Load a Capture register every 2 selected edges.
2	FOURTH	Load a Capture register every 4 selected edges.
3	EIGHTH	Load a Capture register every 8 selected edges.
4	SIXTEENTH	Load a Capture register every 16 selected edges.

Bits 19:18 – LDRB[1:0] RB Loading Edge Selection

Value	Name	Description
0	NONE	None
1	RISING	Rising edge of TIOAx
2	FALLING	Falling edge of TIOAx
3	EDGE	Each edge of TIOAx

Bits 17:16 – LDRA[1:0] RA Loading Edge Selection

53.7.13 DACC Write Protection Mode Register

Name: DACC_WPMR
Offset: 0xE4
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	WPKEY[23:16]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	WPKEY[15:8]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	WPKEY[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	–
Bit	7	6	5	4	3	2	1	0
								WPEN
Access								R/W
Reset								0

Bits 31:8 – WPKEY[23:0] Write Protect Key

Value	Name	Description
0x444143	PASSWD	Writing any other value in this field aborts the write operation of bit WPEN. Always reads as 0.

Bit 0 – WPEN Write Protection Enable
See Register Write Protection for list of write-protected registers.

Value	Description
0	Disables the write protection if WPKEY corresponds to 0x444143 (“DAC” in ASCII).
1	Enables the write protection if WPKEY corresponds to 0x444143 (“DAC” in ASCII).

55.5 Functional Description

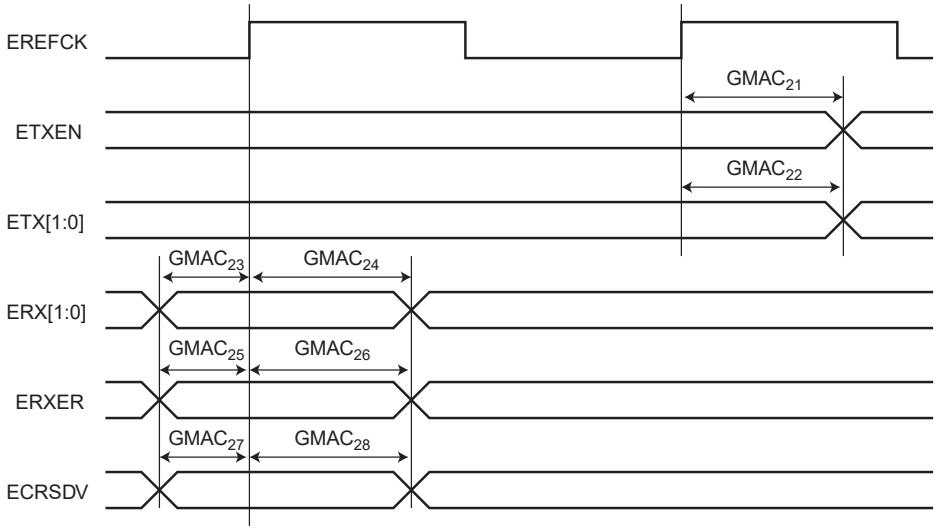
55.5.1 Overview

The Integrity Check Monitor (ICM) is a DMA controller that performs SHA-based memory hashing over memory regions. As shown in figure Integrity Check Monitor Block Diagram, it integrates a DMA interface, a Monitoring Finite State Machine (FSM), an integrity scheduler, a set of context registers, a SHA engine, an interface for configuration and status registers.

The ICM integrates a Secure Hash Algorithm engine (SHA). This engine requires a message padded according to FIPS180-2 specification when used as a SHA calculation unit only. Otherwise, if the ICM is used as integrated check for memory content, the padding is not mandatory. The SHA module produces an N-bit message digest each time a block is read and a processing period ends. N is 160 for SHA1, 224 for SHA224, 256 for SHA256.

When the ICM module is enabled, it sequentially retrieves a circular list of region descriptors from the memory (Main List described in figure ICM Region Descriptor and Hash Areas). Up to four regions may be monitored. Each region descriptor is composed of four words indicating the layout of the memory region (see figure Region Descriptor). It also contains the hashing engine configuration on a per-region basis. As soon as the descriptor is loaded from the memory and context registers are updated with the data structure, the hashing operation starts. A programmable number of blocks (see TRSIZE field of the ICM_RCTRL structure member) is transferred from the memory to the SHA engine. When the desired number of blocks have been transferred, the digest is either moved to memory (Write Back function) or compared with a digest reference located in the system memory (Compare function). If a digest mismatch occurs, an interrupt is triggered if unmasked. The ICM module passes through the region descriptor list until the end of the list marked by an end of list marker (WRAP or EOM bit in ICM_RCFG structure member set to one). To continuously monitor the list of regions, the WRAP bit must be set to one in the last data structure and EOM must be cleared.

Figure 58-32. GMAC RMII Mode Signals



58.13.1.14 SSC Timings

58.13.1.14.1 Timing Conditions

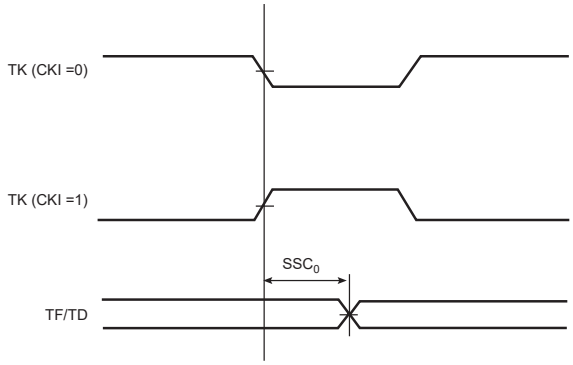
Timings are given assuming the load capacitance in the following table.

Table 58-73. Load Capacitance

Supply	C_L Max
3.3V	30 pF
1.8V	20 pF

58.13.1.14.2 Timing Extraction

Figure 58-33. SSC Transmitter, TK and TF in Output

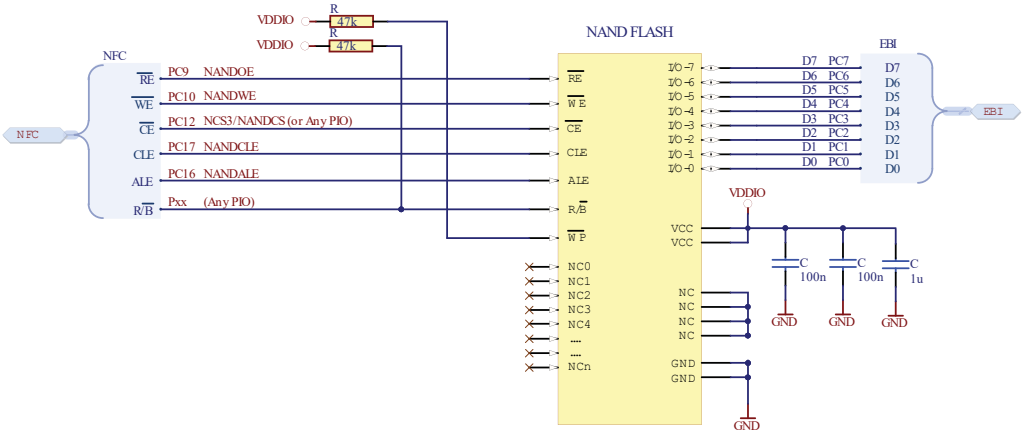


Symbol	VDDIO Supply	1.8V Domain	3.3V Domain	1.8V Domain	3.3V Domain	Unit
	Parameter	Min		Max		
SMC_4	Data Hold after NRD High	0	0	–	–	ns
HOLD or NO HOLD Settings (NRD_HOLD ≠ 0, NRD_HOLD = 0)						
SMC_5	A0–A22 Valid before NRD High	(NRD_SETUP + NRD_PULSE) × t_{CPMCK} - 5.1	(NRD_SETUP + NRD_PULSE) × t_{CPMCK} - 4.3	–	–	ns
SMC_6	NCS low before NRD High	(NRD_SETUP + NRD_PULSE - NCS_RD_SETUP) × t_{CPMCK} - 3.5	(NRD_SETUP + NRD_PULSE - NCS_RD_SETUP) × t_{CPMCK} - 2.4	–	–	ns
SMC_7	NRD Pulse Width	NRD_PULSE × t_{CPMCK} - 0.7	NRD_PULSE × t_{CPMCK} - 0.3	–	–	ns

Table 59-59. SMC Read Signals - NCS Controlled (READ_MODE = 0)

Symbol	VDDIO Supply	1.8V Domain	3.3V Domain	1.8V Domain	3.3V Domain	Unit
	Parameter	Min		Max		
NO HOLD Settings (NCS_RD_HOLD = 0)						
SMC_8	Data Setup before NCS High	24.9	21.4	–	–	ns
SMC_9	Data Hold after NCS High	0	0	–	–	ns
HOLD Settings (NCS_RD_HOLD ≠ 0)						
SMC_{10}	Data Setup before NCS High	13.4	11.7	–	–	ns
SMC_{11}	Data Hold after NCS High	0	0	–	–	ns
HOLD or NO HOLD Settings (NCS_RD_HOLD ≠ 0, NCS_RD_HOLD = 0)						
SMC_{12}	A0–A22 valid before NCS High	(NCS_RD_SETUP + NCS_RD_PULSE) × t_{CPMCK} - 4.0	(NCS_RD_SETUP + NCS_RD_PULSE) × t_{CPMCK} - 3.9	–	–	ns
SMC_{13}	NRD low before NCS High	(NCS_RD_SETUP + NCS_RD_PULSE -	(NCS_RD_SETUP + NCS_RD_PULSE -	–	–	ns

Figure 60-5. Schematic Example with a 2 Gb/8-bit NAND Flash

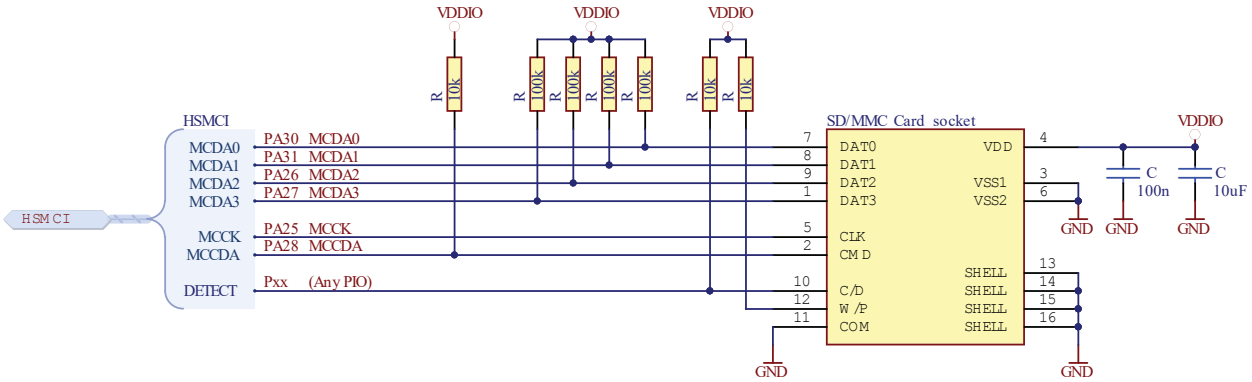


Note: For more details on the pin configuration of the EBI, refer to Table 33-3.

60.2.10 High-Speed Multimedia Card Interface (HSMCI)

Signal Name	Recommended Pin Connection	Description
MCCK	Application dependent	Multimedia Card Clock Pulled-up input (100 kOhm) to VDDIO at reset.
MCCDA	Application dependent (Pullup at VDDIO)	Multimedia Card Slot A Command Pulled-up input (100 kOhm) to VDDIO at reset.
MCDA0–MCDA3	Application dependent (Pullup at VDDIO)	Multimedia Card Slot A Data Pulled-up inputs (100 kOhm) to VDDIO at reset.

Figure 60-6. Schematic Example with SD/MMC Card Interface



60.2.11 QSPI Interface

Signal Name	Recommended Pin Connection	Description
QSCK	Application dependent.	QSPI Serial Clock Pulled-up input (100 kOhm) to VDDIO at reset.
QCS	Application dependent.	QSPI Chip Select