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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv70q20b-aab

19.4.9 Dynamic Clock Gating Register

Name: CCFG_DYNCKG
Offset: 0x011C
Reset: 0
Property: Read/Write

Note: Clearing this register optimizes the power consumption of the system bus circuitry.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						EFCCKG	BRIDCKG	MATCKG
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – EFCCKG EFC Dynamic Clock Gating Enable

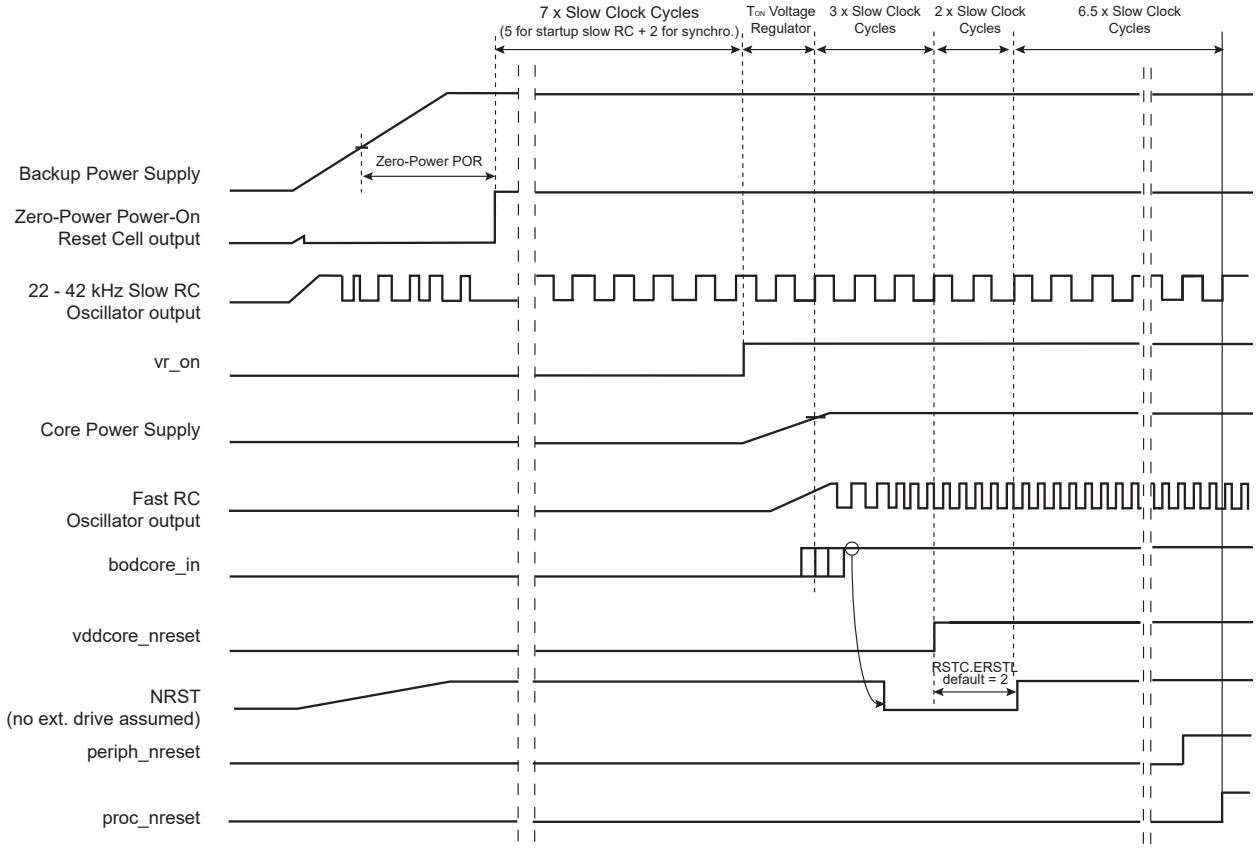
Value	Description
0	EFC dynamic clock gating enabled. The Embedded Flash Controller circuitry is driven by the clock only when an access to the Flash memory is being performed. Power consumption is optimized.
1	EFC dynamic clock gating disabled. The Embedded Flash Controller is always driven by the clock in Active mode.

Bit 1 – BRIDCKG Bridge Dynamic Clock Gating Enable

Value	Description
0	Bridge dynamic clock gating enabled. The peripheral bridge circuitry is driven by the clock only when a transfer to/from any peripheral located on the APB bus is being performed. Power consumption is optimized.
1	Bridge dynamic clock gating disabled. The peripheral bridge circuitry is always driven by the clock in Active mode.

Bit 0 – MATCKG MATRIX Dynamic Clock Gating

Figure 23-6. Raising the VDDIO Power Supply



Note: After “proc_nreset” rising, the core starts fetching instructions from Flash.

23.4.7 Core Reset

The Supply Controller manages the vddcore_nreset signal to the Reset Controller, as described in the "Backup Power Supply Reset" section. The vddcore_nreset signal is normally asserted before shutting down the core power supply and released as soon as the core power supply is correctly regulated.

There are two additional sources which can be programmed to activate vddcore_nreset:

- a supply monitor detection
- a brownout detection

23.4.7.1 Supply Monitor Reset

The supply monitor is capable of generating a reset of the system. This is enabled by setting SUPC_SMMR.SMRSTEN.

If SUPC_SMMR.SMRSTEN is set and if a supply monitor detection occurs, the vddcore_nreset signal is immediately activated for a minimum of one slow clock cycle.

23.4.7.2 Brownout Detector Reset

The brownout detector provides the bodcore_in signal to the SUPC. This signal indicates that the voltage regulation is operating as programmed. If this signal is lost for longer than 1 slow clock period while the voltage regulator is enabled, the SUPC asserts vddcore_nreset if SUPC_MR.BODRSTEN is written to ‘1’.

If SUPC_MR.BODRSTEN is set and the voltage regulation is lost (output voltage of the regulator too low), the vddcore_nreset signal is asserted for a minimum of one slow clock cycle and then released if bodcore_in has been reactivated. SUPC_SR.BODRSTS indicates the source of the last reset.

26.4.5.3 RSTC Mode Register

Name: RSTC_MR
Offset: 0x08
Reset: 0x00000001
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the System Controller Write Protection Mode Register (SYSC_WPMR).

Bit	31	30	29	28	27	26	25	24
	KEY[7:0]							
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					ERSTL[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
				URSTIEN				URSTEN
Access				R/W				R/W
Reset				0				1

Bits 31:24 – KEY[7:0] Write Access Password

Value	Name	Description
0xA5	PASSWD	Writing any other value in this field aborts the write operation. Always reads as 0.

Bits 11:8 – ERSTL[3:0] External Reset Length
This field defines the external reset length. The external reset is asserted during a time of $2^{(ERSTL+1)}$ SLCK cycles. This allows assertion duration to be programmed between 60 µs and 2 seconds. Note that synchronization cycles must also be considered when calculating the actual reset length as previously described.

Bit 4 – URSTIEN User Reset Interrupt Enable

Value	Description
0	RSTC_SR.USRTS at ‘1’ has no effect on the RSTC interrupt line.
1	RSTC_SR.USRTS at ‘1’ asserts the RSTC interrupt line if URSTEN = 0.

Bit 0 – URSTEN User Reset Enable

31.15 Main Crystal Oscillator Failure Detection

The Main crystal oscillator failure detector monitors the Main crystal oscillator against the Slow RC oscillator and provides an automatic switchover of the MAINCK source to the Main RC oscillator in case of failure detection.

The failure detector can be enabled or disabled by configuring the CKGR_MOR.CFDEN, and it can also be disabled in either of the following cases:

- After a VDDCORE reset
- When the Main crystal oscillator is disabled (MOSCXTEN = 0)

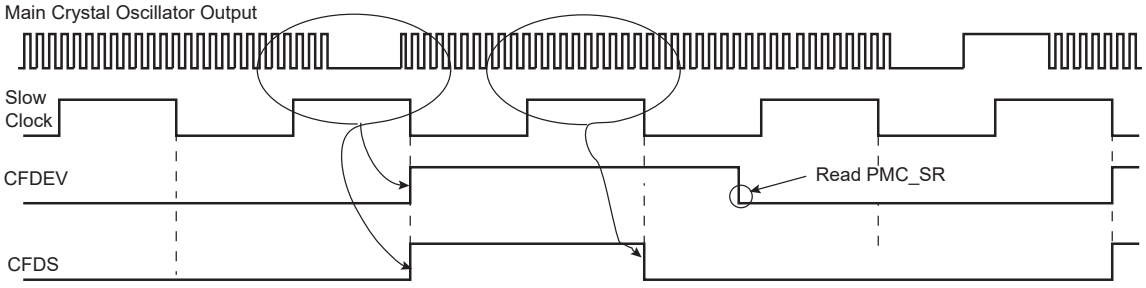
A failure is detected by means of a counter incrementing on the Main crystal oscillator output and detection logic is triggered by the Slow RC oscillator which is automatically enabled when CFDEN = 1.

The counter is cleared when the Slow RC oscillator clock signal is low and enabled when the signal is high. Thus, the failure detection time is one Slow RC oscillator period. If, during the high level period of the Slow RC oscillator clock signal, less than eight Main crystal oscillator clock periods have been counted, then a failure is reported. Note that when enabling the failure detector, up to two cycles of the Slow RC oscillator are needed to detect a failure of the Main crystal oscillator.

If a failure of Main crystal oscillator is detected, PMC_SR.CFDEV and PMC_SR.FOS both indicate a failure event. PMC_SR.CFDEV is cleared on read of PMC_SR, and PMC_SR.FOS is cleared by writing a ‘1’ to the FOCLR bit in the PMC Fault Output Clear Register (PMC_FOCR).

Only PMC_SR.CFDEV can generate an interrupt if the corresponding interrupt source is enabled in PMC_IER. The current status of the clock failure detection can be read at any time from PMC_SR.CFDS.

Figure 31-5. Clock Failure Detection Example



Note: Ratio of clock periods is for illustration purposes only.

If the Main crystal oscillator is selected as the source clock of MAINCK (CKGR_MOR.MOSCSEL = 1), and if the MCK source is PLLACK or UPLLCKDIV (CSS = 2 or 3), a clock failure detection automatically forces MAINCK to be the source clock for MCK. Then, regardless of the PMC configuration, a clock failure detection automatically forces the Main RC oscillator to be the source clock for MAINCK. If the Main RC oscillator is disabled when a clock failure detection occurs, it is automatically re-enabled by the clock failure detection mechanism.

Two Slow RC oscillator clock cycles are necessary to detect and switch from the Main crystal oscillator to the Main RC oscillator if the source of MCK is MAINCK, or three Slow RC oscillator clock cycles if the source of MCK is PLLACK or UPLLCKDIV.

A clock failure detection activates a fault output that is connected to the Pulse Width Modulator (PWM) Controller. With this connection, the PWM controller is able to force its outputs and to protect the driven device, if a clock failure is detected.

31.20.15 PMC Interrupt Disable Register

Name: PMC_IDR
Offset: 0x0064
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			XT32KERR			CFDEV	MOSCRCS	MOSCSELS
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
		PCKRDY6	PCKRDY5	PCKRDY4	PCKRDY3	PCKRDY2	PCKRDY1	PCKRDY0
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
		LOCKU			MCKRDY		LOCKA	MOSCXTS
Access								
Reset								

Bit 21 – XT32KERR 32.768 kHz Crystal Oscillator Error Interrupt Disable

Bit 18 – CFDEV Clock Failure Detector Event Interrupt Disable

Bit 17 – MOSCRCS Main RC Status Interrupt Disable

Bit 16 – MOSCSELS Main Clock Source Oscillator Selection Status Interrupt Disable

Bits 8, 9, 10, 11, 12, 13, 14 – PCKRDY Programmable Clock Ready x Interrupt Disable

Bit 6 – LOCKU UTMI PLL Lock Interrupt Disable

Bit 3 – MCKRDY Master Clock Ready Interrupt Disable

Bit 1 – LOCKA PLLA Lock Interrupt Disable

Bit 0 – MOSCXTS Main Crystal Oscillator Status Interrupt Disable

Figure 35-24. TDF Optimization Disabled (TDF Mode = 0): TDF wait states between 2 read accesses on different chip selects

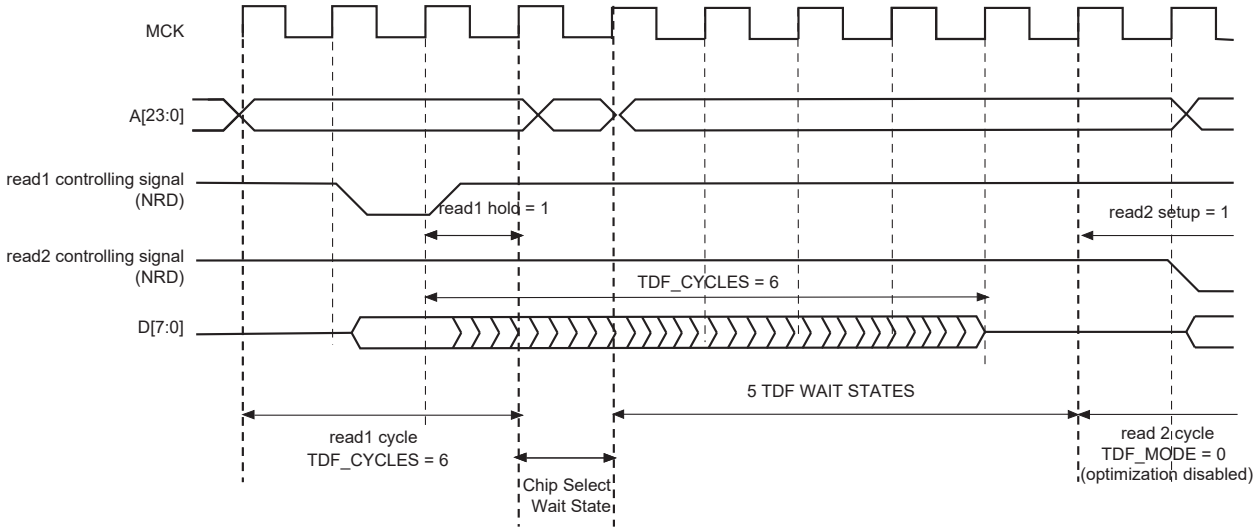
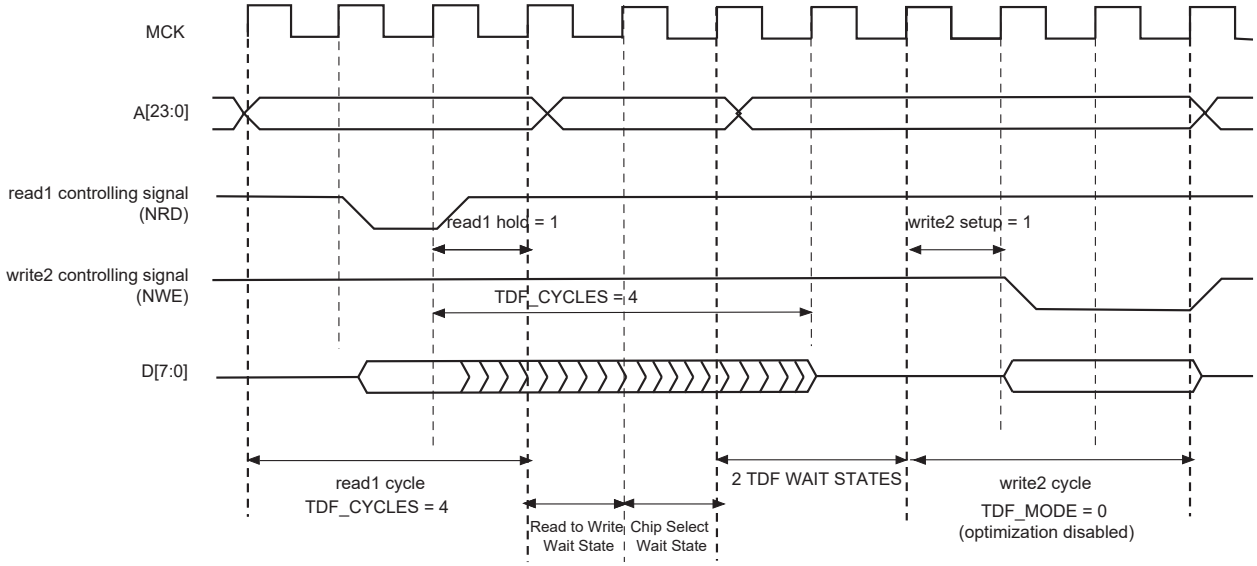


Figure 35-25. TDF Mode = 0: TDF wait states between a read and a write access on different chip selects



35.16.1.1 SMC Setup Register

Name: SMC_SETUP[0..3]
Offset: 0x00
Reset: 0
Property: R/W

This register can only be written if the WPEN bit is cleared in the “SMC Write Protection Mode Register” .

Bit	31	30	29	28	27	26	25	24
			NCS_RD_SETUP[5:0]					
Access								
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
			NRD_SETUP[5:0]					
Access								
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
			NCS_WR_SETUP[5:0]					
Access								
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			NWE_SETUP[5:0]					
Access								
Reset			0	0	0	0	0	0

Bits 29:24 – NCS_RD_SETUP[5:0] NCS Setup Length in READ Access
In read access, the NCS signal setup length is defined as:

NCS setup length = (128* NCS_RD_SETUP[5] + NCS_RD_SETUP[4:0]) clock cycles

Bits 21:16 – NRD_SETUP[5:0] NRD Setup Length
The NRD signal setup length is defined in clock cycles as:

NRD setup length = (128* NRD_SETUP[5] + NRD_SETUP[4:0]) clock cycles

Bits 13:8 – NCS_WR_SETUP[5:0] NCS Setup Length in WRITE Access
In write access, the NCS signal setup length is defined as:

NCS setup length = (128* NCS_WR_SETUP[5] + NCS_WR_SETUP[4:0]) clock cycles

Bits 5:0 – NWE_SETUP[5:0] NWE Setup Length
The NWE signal setup length is defined as:

NWE setup length = (128* NWE_SETUP[5] + NWE_SETUP[4:0]) clock cycles

38.6.12 VLAN Support

The following table describes an Ethernet encoded 802.1Q VLAN tag.

Table 38-5. 802.1Q VLAN Tag

TPID (Tag Protocol Identifier) 16 bits	TCI (Tag Control Information) 16 bits
0x8100	First 3 bits priority, then CFI bit, last 12 bits VID

The VLAN tag is inserted at the 13th byte of the frame adding an extra four bytes to the frame. To support these extra four bytes, the GMAC can accept frame lengths up to 1536 bytes by setting bit 8 in the Network Configuration register.

If the VID (VLAN identifier) is null (0x000) this indicates a priority-tagged frame.

The following bits in the receive buffer descriptor status word give information about VLAN tagged frames:-

- Bit 21 set if receive frame is VLAN tagged (i.e., type ID of 0x8100).
- Bit 20 set if receive frame is priority tagged (i.e., type ID of 0x8100 and null VID). (If bit 20 is set, bit 21 will be set also.)
- Bit 19, 18 and 17 set to priority if bit 21 is set.
- Bit 16 set to CFI if bit 21 is set.

The GMAC can be configured to reject all frames except VLAN tagged frames by setting the discard non-VLAN frames bit in the Network Configuration register.

38.6.13 Wake on LAN Support

The receive block supports Wake on LAN by detecting the following events on incoming receive frames:

- Magic packet
- Address Resolution Protocol (ARP) request to the device IP address
- Specific address 1 filter match
- Multicast hash filter match

These events can be individually enabled through bits [19:16] of the Wake on LAN register. Also, for Wake on LAN detection to occur, receive enable must be set in the Network Control register, however a receive buffer does not have to be available.

In case of an ARP request, specific address 1 or multicast filter events will occur even if the frame is errored. For magic packet events, the frame must be correctly formed and error free.

A magic packet event is detected if all of the following are true:

- Magic packet events are enabled through bit 16 of the Wake on LAN register
- The frame's destination address matches specific address 1
- The frame is correctly formed with no errors
- The frame contains at least 6 bytes of 0xFF for synchronization
- There are 16 repetitions of the contents of Specific Address 1 register immediately following the synchronization

An ARP request event is detected if all of the following are true:

- ARP request events are enabled through bit 17 of the Wake on LAN register
- Broadcasts are allowed by bit 5 in the Network Configuration register

38.8.27 GMAC Stacked VLAN Register

Name: GMAC_SVLAN
Offset: 0x0C0
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	ESVLAN							
Access								
Reset	0							

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	VLAN_TYPE[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	VLAN_TYPE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – ESVLAN Enable Stacked VLAN Processing Mode
0: Disable the stacked VLAN processing mode

1: Enable the stacked VLAN processing mode

Value	Description
0	Stacked VLAN Processing disabled
1	Stacked VLAN Processing enabled

Bits 15:0 – VLAN_TYPE[15:0] User Defined VLAN_TYPE Field
When Stacked VLAN is enabled (ESVLAN=1), the first VLAN tag in a received frame will only be accepted if the VLAN type field is equal to this user defined VLAN_TYPE, OR equal to the standard VLAN type (0x8100).
Note: The second VLAN tag of a Stacked VLAN packet will only be matched correctly if its VLAN_TYPE field equals 0x8100.

40.14.16 HSMCI DMA Configuration Register

Name: HSMCI_DMA
Offset: 0x50
Reset: 0x0
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the HSMCI Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								DMAEN
Reset								0

Bit	7	6	5	4	3	2	1	0
Access		CHKSIZE[2:0]						
Reset		0	0	0				

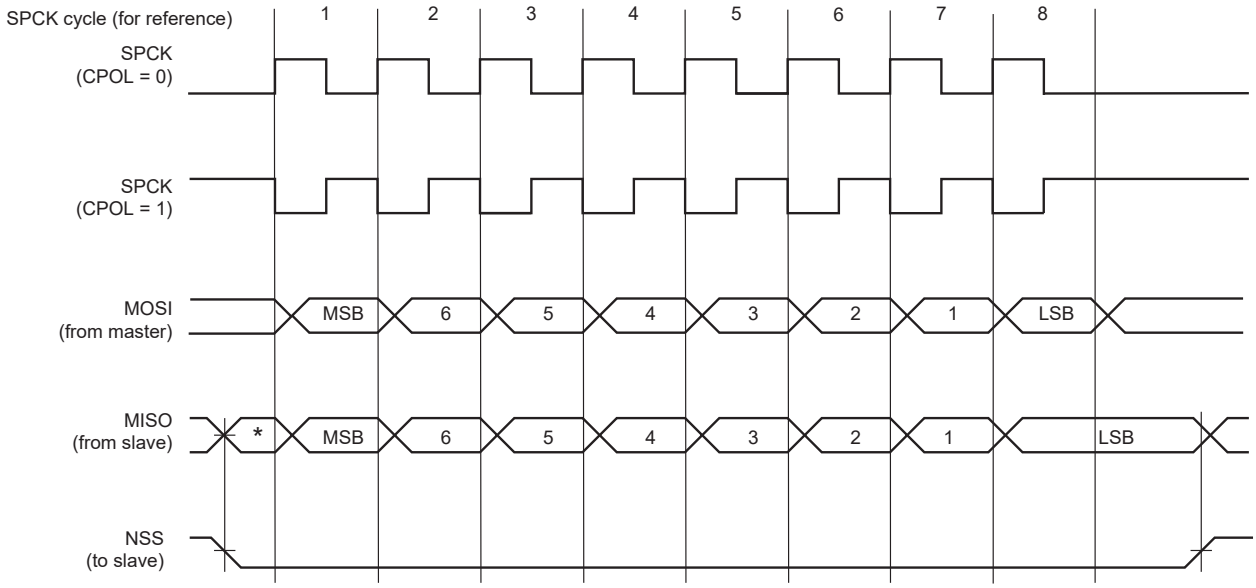
Bit 8 – DMAEN DMA Hardware Handshaking Enable

Value	Description
0	DMA interface is disabled.
1	DMA Interface is enabled. Note: To avoid unpredictable behavior, DMA hardware handshaking must be disabled when CPU transfers are performed.

Bits 324:4 – CHKSIZE[320:0] DMA Channel Read and Write Chunk Size
The CHKSIZE field indicates the number of data available when the DMA chunk transfer request is asserted.

Value	Name	Description
0	1	1 data available
1	2	2 data available
2	4	4 data available
3	8	8 data available
4	16	16 data available

Figure 41-4. SPI Transfer Format (NCPHA = 0, 8 bits per transfer)



* Not defined.

41.7.3 Master Mode Operations

When configured in Master mode, the SPI operates on the clock generated by the internal programmable baud rate generator. It fully controls the data transfers to and from the slave(s) connected to the SPI bus. The SPI drives the chip select line to the slave and the serial clock signal (SPCK).

The SPI features two holding registers, the Transmit Data Register (SPI_TDR) and the Receive Data Register (SPI_RDR), and a single shift register. The holding registers maintain the data flow at a constant rate.

After enabling the SPI, a data transfer starts when the processor writes to SPI_TDR. The written data is immediately transferred into the internal shift register and the transfer on the SPI bus starts. While the data in the shift register is shifted on the MOSI line, the MISO line is sampled and shifted into the shift register. Data cannot be loaded in SPI_RDR without transmitting data. If there is no data to transmit, dummy data can be used (SPI_TDR filled with ones). If SPI_MR.WDRBT is set, transmission can occur only if SPI_RDR has been read. If Receiving mode is not required, for example when communicating with a slave receiver only (such as an LCD), the receive status flags in the SPI Status register (SPI_SR) can be discarded.

Before writing SPI_TDR, SPI_MR.PCS must be set in order to select a slave.

If new data is written in SPI_TDR during the transfer, it is kept in SPI_TDR until the current transfer is completed. Then, the received data is transferred from the shift register to SPI_RDR, the data in SPI_TDR is loaded in the shift register and a new transfer starts.

As soon as SPI_TDR is written, the Transmit Data Register Empty (TDRE) flag in SPI_SR is cleared. When the data written in SPI_TDR is loaded into the shift register, TDRE in SPI_SR is set. The TDRE flag is used to trigger the Transmit DMA channel.

See the figure below.

46.7.14 USART Interrupt Mask Register (SPI_MODE)

Name: US_IMR (SPI_MODE)
Offset: 0x0010
Reset: 0x0
Property: Read-only

This configuration is relevant only if USART_MODE = 0xE or 0xF in the USART Mode Register.

The following configuration values are valid for all listed bit names of this register:

0: The corresponding interrupt is not enabled.

1: The corresponding interrupt is enabled.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset					0			

Bit	15	14	13	12	11	10	9	8
Access								
Reset						0	0	

Bit	7	6	5	4	3	2	1	0
Access								
Reset			0				0	0

Bit 19 – NSSE NSS Line (Driving CTS Pin) Rising or Falling Edge Event Interrupt Mask

Bit 10 – UNRE SPI Underrun Error Interrupt Mask

Bit 9 – TXEMPTY TXEMPTY Interrupt Mask

Bit 5 – OVRE Overrun Error Interrupt Mask

Bit 1 – TXRDY TXRDY Interrupt Mask

Bit 0 – RXRDY RXRDY Interrupt Mask

46.7.44 USART LON IDT Rx Register

Name: US_IDTRX
Offset: 0x0084
Reset: 0x0
Property: Read/Write

This register is relevant only if USART_MODE = 0x9 in the USART Mode Register.

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	IDTRX[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	IDTRX[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IDTRX[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – IDTRX[23:0] LON Indeterminate Time after Reception (comm_type = 1 mode only)

Value	Description
0–16777215	LON indeterminate time after reception in t_{bit}.

49.6.18 MCAN Interrupt Line Select Register

Name: MCAN_ILS
Offset: 0x58
Reset: 0x00000000
Property: Read/Write

The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the Interrupt Register to one of the two module interrupt lines.

0: Interrupt assigned to interrupt line MCAN_INT0.

1: Interrupt assigned to interrupt line MCAN_INT1.

Bit	31	30	29	28	27	26	25	24
			ARAL	PEDL	PEAL	WDIL	BOL	EWL
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	EPL	ELOL			DRXL	TOOL	MRAFL	TSWL
Access	R/W	R/W			R/W	R/W	R/W	R/W
Reset	0	0			0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TEFLL	TEFFL	TEFWL	TEFNL	TFEL	TCFL	TCL	HPML
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RF1LL	RF1FL	RF1WL	RF1NL	RF0LL	RF0FL	RF0WL	RF0NL
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 29 – ARAL Access to Reserved Address Line

Bit 28 – PEDL Protocol Error in Data Phase Line

Bit 27 – PEAL Protocol Error in Arbitration Phase Line

Bit 26 – WDIL Watchdog Interrupt Line

Bit 25 – BOL Bus_Off Status Interrupt Line

Bit 24 – EWL Warning Status Interrupt Line

Bit 23 – EPL Error Passive Interrupt Line

Bit 22 – ELOL Error Logging Overflow Interrupt Line

Bit 19 – DRXL Message stored to Dedicated Receive Buffer Interrupt Line

50. Timer Counter (TC)

50.1 Description

A Timer Counter (TC) module includes three identical TC channels. The number of implemented TC modules is device-specific.

Each TC channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

Each channel has three external clock inputs, five internal clock inputs and two multipurpose input/output signals which can be configured by the user. Each channel drives an internal interrupt signal which can be programmed to generate processor interrupts.

The TC embeds a quadrature decoder (QDEC) connected in front of the timers and driven by TIOA0, TIOB0 and TIOB1 inputs. When enabled, the QDEC performs the input lines filtering, decoding of quadrature signals and connects to the timers/counters in order to read the position and speed of the motor through the user interface.

The TC block has two global registers which act upon all TC channels:

- Block Control register (TC_BCR)—allows channels to be started simultaneously with the same instruction
- Block Mode register (TC_BMR)—defines the external clock inputs for each channel, allowing them to be chained

50.2 Embedded Characteristics

- Total of 12 Channels
- 16-bit Channel Size
- Wide Range of Functions Including:
  - Frequency measurement
  - Event counting
  - Interval measurement
  - Pulse generation
  - Delay timing
  - Pulse Width Modulation
  - Up/down capabilities
  - Quadrature decoder
  - 2-bit Gray up/down count for stepper motor
- Each Channel is User-Configurable and Contains:
  - Three external clock inputs
  - Five Internal clock inputs
  - Two multipurpose input/output signals acting as trigger event
  - Trigger/capture events can be directly synchronized by PWM signals
- Internal Interrupt Signal

- Configuration of the fault protection (FMOD and FFIL in PWM_FMR, PWM_FPV and PWM_FPE)
- Enable of the interrupts (writing CHIDx and FCHIDx in PWM_IER1, and writing WRDY, UNRE, CMPMx and CMPUx in PWM_IER2)
- Enable of the PWM channels (writing CHIDx in the PWM_ENA register)

51.6.6.2 Source Clock Selection Criteria

The large number of source clocks can make selection difficult. The relationship between the value in the PWM Channel Period Register (PWM_CPRDx) and the PWM Channel Duty Cycle Register (PWM_CDTYx) helps the user select the appropriate clock. The event number written in the Period Register gives the PWM accuracy. The Duty-Cycle quantum cannot be lower than 1/CPRDx value. The higher the value of PWM_CPRDx, the greater the PWM accuracy.

For example, if the user sets 15 (in decimal) in PWM_CPRDx, the user is able to set a value from between 1 up to 14 in PWM_CDTYx. The resulting duty-cycle quantum cannot be lower than 1/15 of the PWM period.

51.6.6.3 Changing the Duty-Cycle, the Period and the Dead-Times

It is possible to modulate the output waveform duty-cycle, period and dead-times.

To prevent unexpected output waveform, the user must use the PWM Channel Duty Cycle Update Register (PWM_CDTYUPDx), the PWM Channel Period Update Register (PWM_CPRDUPDx) and the PWM Channel Dead Time Update Register (PWM_DTUPDx) to change waveform parameters while the channel is still enabled.

- If the channel is an asynchronous channel (SYNCx = 0 in PWM Sync Channels Mode Register (PWM_SCM)), these registers hold the new period, duty-cycle and dead-times values until the end of the current PWM period and update the values for the next period.
- If the channel is a synchronous channel and update method 0 is selected (SYNCx = 1 and UPDM = 0 in PWM_SCM register), these registers hold the new period, duty-cycle and dead-times values until the bit UPDULOCK is written at ‘1’ (in PWM Sync Channels Update Control Register (PWM_SCUC)) and the end of the current PWM period, then update the values for the next period.
- If the channel is a synchronous channel and update method 1 or 2 is selected (SYNCx = 1 and UPDM = 1 or 2 in PWM_SCM register):
  - registers PWM_CPRDUPDx and PWM_DTUPDx hold the new period and dead-times values until the bit UPDULOCK is written at ‘1’ (in PWM_SCUC) and the end of the current PWM period, then update the values for the next period.
  - register PWM_CDTYUPDx holds the new duty-cycle value until the end of the update period of synchronous channels (when UPRCNT is equal to UPR in PWM Sync Channels Update Period Register (PWM_SCUP)) and the end of the current PWM period, then updates the value for the next period.
    Note: If the update registers PWM_CDTYUPDx, PWM_CPRDUPDx and PWM_DTUPDx are written several times between two updates, only the last written value is taken into account.

51.7.39 PWM Comparison x Mode Update Register

Name: PWM_CMPMUPDx
Offset: 0x013C + x*0x10 [x=0..7]
Reset: –
Property: W

This register acts as a double buffer for the CEN, CTR, CPR and CUPR values. This prevents an unexpected comparison x match.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					CUPRUPD[3:0]			
Access					W	W	W	W
Reset					0	0	0	–

Bit	15	14	13	12	11	10	9	8
					CPRUPD[3:0]			
Access					W	W	W	W
Reset					0	0	0	–

Bit	7	6	5	4	3	2	1	0
	CTRUPD[3:0]							CENUPD
Access	W	W	W	W				W
Reset	0	0	0	–				–

Bits 19:16 – CUPRUPD[3:0] Comparison x Update Period Update
Defines the time between each update of the comparison x mode and the comparison x value. This time is equal to CUPR+1 periods of the channel 0 counter.

Bits 11:8 – CPRUPD[3:0] Comparison x Period Update
CPR defines the maximum value of the comparison x period counter (CPRCNT). The comparison x value is performed periodically once every CPR+1 periods of the channel 0 counter.

Bits 7:4 – CTRUPD[3:0] Comparison x Trigger Update
The comparison x is performed when the value of the comparison x period counter (CPRCNT) reaches the value defined by CTR.

Bit 0 – CENUPD Comparison x Enable Update

Value	Description
0	The comparison x is disabled and can not match.
1	The comparison x is enabled and can match.

The DATA code in AFEC_CDR is up to 16-bit positive integer or two's complement (signed integer).

The code does not exceed 4095 when the field AFEC_EMR.RES=0 (12-bit mode, no averaging).

59.8.4.1 Differential Mode (12-bit mode)

A differential input voltage $V_{IN} = V_{INP} - V_{INN}$ can be applied between two selected differential pins, e.g. AFE0_AD0 and AFE0_AD1.The ideal code C_i is calculated by using the following formula and rounding the result to the nearest positive integer.

$$C_i = \frac{4096}{V_{\mathrm{VREFP}}} \times V_{\mathrm{IN}} \times \mathrm{Gain} + (2047)$$

For the other resolution defined by RES, the code C_i is extended to the corresponding resolution.

The table below is a computation example for the above formula, where V_{VREFP} = 3V.

Table 59-32. Input Voltage Values in Differential Mode, Nonsigned Output

C_i		Gain		
Signed	Nonsigned	1	2	4
-2048	0	-3	-1.5	-0.75
0	2047	0	0	0
2047	4095	3	1.5	0.75

59.8.4.2 Single-ended Mode (12-bit mode)

A single input voltage V_{IN} can be applied to selected pins, e.g. AFE0_AD0 or AFE0_AD1. The ideal code C_i is calculated using the following formula and rounding the result to the nearest positive integer.

The single-ended ideal code conversion formula is:

$$C_i = \frac{4096}{V_{\mathrm{VREFP}}} \times (V_{\mathrm{IN}} - V_{\mathrm{DAC}}) \times \mathrm{Gain} + 2047$$

For the other resolution defined by RES, the code C_i is extended to the corresponding resolution.

The table below is a computation example for the above formula, where V_{VREFP} = 3V:

Table 59-33. Input Voltage Values in Single-ended Mode

C_i		Gain		
Signed	Nonsigned	1	2	4
-2048	0	0	0.75	1.125
0	2047	1.5	1.5	1.5
2047	4095	3	2.25	1.875

59.8.4.3 Example of LSB Computation

The LSB is relative to the analog scale V_{VREFP}.

The term LSB expresses the quantization step in volts, also used for one AFE code variation.

- Single-ended (SE) (ex: V_{VREFP} = 3.0V)
  - Gain = 1, LSB = (3.0V / 4096) = 732 µV
  - Gain = 2, LSB = (1.5V / 4096) = 366 µV

Date	Changes
	- Section 63.1.1 ”AFE Controller (AFEC)”: “AFE max sampling frequency is 1.74 Msps” - Section 63.2.1 ”AFE Controller (AFEC)”: “AFE max sampling frequency is 1.74 Msps”
End	

Table 62-3. SAM E70/S70/V70/V71 Datasheet Rev. 44003D – Revision History

Date	Comments
01-June-16	“Introduction” AFE maximum sampling frequency now 1.7 Msps.
	“Features” Main RC oscillator default frequency changed to 12 MHz. AFE maximum sampling frequency now 1.7 Msps.
	Section 2. “Configuration Summary” Table 2-1 “Configuration Summary”: on QFN64 package, HS USB now supported.
	Table 4-1 “Signal Description List”: updated ‘Comments’ column for for signals PCK0–PCK2, TRACECLK,, URXDx, Timer Counter - TC and for CANTXx. Added comment on Programmable Clock Output for PCK7 and on I2SC for GCLK.
	Table 6-1 “144-lead Package Pinout”: CANRX1 now shown as not available on PD28. Added signal type for I2SC signals. Updated notes (5) and (10).
	Table 6-2 “100-lead Package Pinout”: Added signal type for I2SC signals. Updated notes (5) and (10).
	Table 6-3 “64-lead LQFP Package Pinout”: updated notes (4) and (9).
	Section 7.2.1 “Powerup”: updated equation for minimum VDDCORE slope.
	Table 14-1 “Peripheral Identifiers”: Added IDs 71, 72, 73.
	Section 19. “Bus Matrix (MATRIX)” Section 19.1 “Description”, Section 19.2 “Embedded Characteristics”: number of masters changed to 13. Table 19-1 “Bus Matrix Masters” and Table 19-3 “Master to Slave Access”: added Master 12: Cortex-M7. Table 19-3 “Master to Slave Access”: changed access for Master 0/Slave 6. Added Section 19.3.6 “Configuration of Automatic Clock-off Mode”. Table 19-4 “Register Mapping”: added register CCFG_DYNCFG at offset 0x011C and register CCFG_PCCR at offset 0x0118. Added Section 19.4.8 “Peripheral Clock Configuration Register”. Added Section 19.4.9 “Dynamic Clock Gating Register”.
	Section 21. “Chip Identifier (CHIPID)” Updated Table 21-1 “SAM V71 Chip ID Registers”. Added notes (1) and (2).

Date	Changes
	- Table 56-38 “VREFP Electrical Characteristics”: changed min and max values for I_{VREFP}. - Table 56-46 “Single-ended Output Offset Error”: added note on voltage application. - Table 56-47 “Single-ended Static Electrical Characteristics”: added conditions and values. - Table 56-49 “Differential Static Electrical Characteristics”: changed min and max values. Added Section 56.10 “Analog Comparator Characteristics”. Section 56.12 “12-bit DAC Characteristics” - Added note to Table 56-59 “Analog Power Supply Characteristics”. Added new conditions to Table 56-62 “Static Performance Characteristics”. and updated min and max values for INL, DNL and Gain Error. Section 56.13 “Timings for Worst-Case Conditions” - Table 56-68 “I/O Characteristics”: new conditions and the corresponding max values added. - Section 56.13.2 “Embedded Flash Characteristics”: in Table 56-87 “AC Flash Characteristics” changed Full Chip Erase values. Replaced two “Embedded Flash Wait State” tables with single Table 56-88 “Embedded Flash Wait State at 105°C“
	Section 56.14 “Timings for STH Conditions” - Table 56-92 “I/O Characteristics”: new conditions and the corresponding max values added. - Section 56.14.2 “Embedded Flash Characteristics”: replaced two “Embedded Flash Wait State” tables with single Table 56-112 “Embedded Flash Wait State at 105°C“
	Section 57. “Mechanical Characteristics” Deleted Section 57.6 “64-lead QFN Wettable Flanks Package”.
	Section 59. “Ordering Information”: updated ordering codes by appending trailing ‘T’. Removed Note 1 and cross-references. Changed conditioning to Tape & Reel.

Table 62-6. SAM E70/S70/V70/V71 Datasheet Rev. 44003A – Revision History

Date	Changes
15-Oct-13	First issue