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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv71n19b-aab

18.3.4.1 Write Handshaking

For details on the write handshaking sequence, refer to the following figure and table.

Figure 18-2. Parallel Programming Timing, Write Sequence

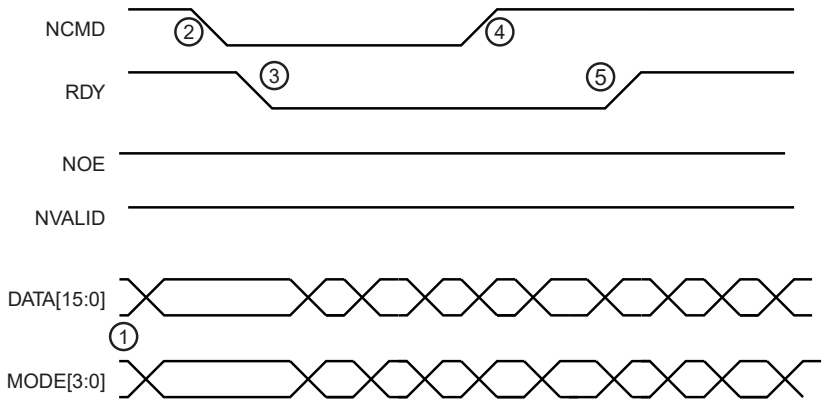


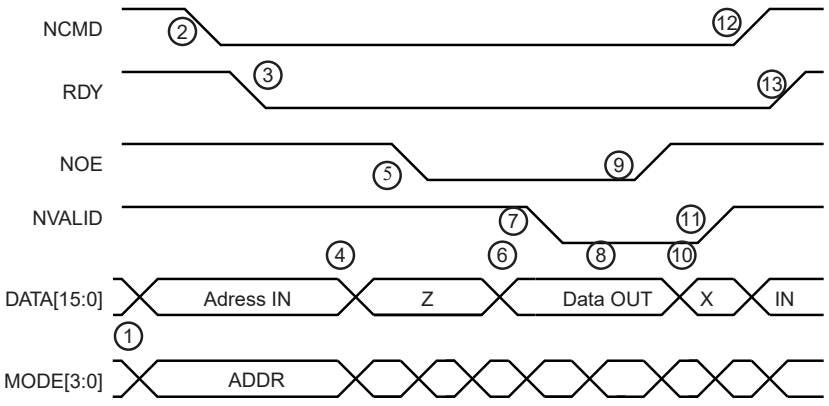
Table 18-4. Write Handshake

Step	Programmer Action	Device Action	Data I/O
1	Sets MODE and DATA signals	Waits for NCMD low	Input
2	Clears NCMD signal	Latches MODE and DATA	Input
3	Waits for RDY low	Clears RDY signal	Input
4	Releases MODE and DATA signals	Executes command and polls NCMD high	Input
5	Sets NCMD signal	Executes command and polls NCMD high	Input
6	Waits for RDY high	Sets RDY	Input

18.3.4.2 Read Handshaking

For details on the read handshaking sequence, refer to the following figure and table.

Figure 18-3. Parallel Programming Timing, Read Sequence



1. Round-robin Arbitration (default)
2. Fixed Priority Arbitration

Each algorithm may be complemented by selecting a default master configuration for each slave.

When re-arbitration is required, specific conditions apply. Refer to the "Arbitration Rules" section.

19.3.3.1 Arbitration Rules

Each arbiter has the ability to arbitrate between requests from two or more masters. To avoid burst breaking and to provide maximum throughput for slave interfaces, arbitration should take place during the following cycles:

- Idle cycles: When a slave is not connected to any master or is connected to a master which is not currently accessing it
- Single cycles: When a slave is performing a single access
- End of Burst cycles: When the current cycle is the last cycle of a burst transfer. For a defined length burst, predicted end of burst matches the size of the transfer but is managed differently for undefined length burst. Refer to the "Undefined Length Burst Arbitration" section.
- Slot cycle limit: When the slot cycle counter has reached the limit value indicating that the current master access is too long and must be broken. Refer to the "Slot Cycle Limit Arbitration" section.

19.3.3.1.1 Undefined Length Burst Arbitration

In order to prevent slave handling during undefined length bursts, the user can trigger the re-arbitration before the end of the incremental bursts. The re-arbitration period can be selected from the following Undefined Length Burst Type (ULBT) possibilities:

1. Unlimited: no predetermined end of burst is generated. This value enables 1-Kbyte burst lengths.
2. 1-beat bursts: predetermined end of burst is generated at each single transfer during the INCR transfer.
3. 4-beat bursts: predetermined end of burst is generated at the end of each 4-beat boundary during INCR transfer.
4. 8-beat bursts: predetermined end of burst is generated at the end of each 8-beat boundary during INCR transfer.
5. 16-beat bursts: predetermined end of burst is generated at the end of each 16-beat boundary during INCR transfer.
6. 32-beat bursts: predetermined end of burst is generated at the end of each 32-beat boundary during INCR transfer.
7. 64-beat bursts: predetermined end of burst is generated at the end of each 64-beat boundary during INCR transfer.
8. 128-beat bursts: predetermined end of burst is generated at the end of each 128-beat boundary during INCR transfer.

The use of undefined length16-beat bursts, or less, is discouraged since this decreases the overall bus bandwidth due to arbitration and slave latencies at each first access of a burst.

If the master does not permanently and continuously request the same slave or has an intrinsically limited average throughput, the ULBT should be left at its default unlimited value, knowing that the AHB specification natively limits all word bursts to 256 beats and double-word bursts to 128 beats because of its 1-Kbyte address boundaries.

Unless duly needed, the ULBT should be left at its default value of 0 for power saving.

This selection is made through the ULBT field of the Master Configuration Registers (MATRIX_MCFG).

31.20.2 PMC System Clock Disable Register

Name: PMC_SCDR
Offset: 0x0004
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PCK7	PCK6	PCK5	PCK4	PCK3	PCK2	PCK1	PCK0
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			USBCLK					
Access								
Reset								

Bits 8, 9, 10, 11, 12, 13, 14, 15 – PCK Programmable Clock x Output Disable

Value	Description
0	No effect.
1	Disables the corresponding Programmable Clock output.

Bit 5 – USBCLK Disable USB FS Clock

Value	Description
0	No effect.
1	Disables USB FS clock.

31.20.3 PMC System Clock Status Register

Name: PMC_SCSR
Offset: 0x0008
Reset: 0x00000001
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PCK7	PCK6	PCK5	PCK4	PCK3	PCK2	PCK1	PCK0
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
			USBCLK					HCLKS
Access								
Reset			0					1

Bits 8, 9, 10, 11, 12, 13, 14, 15 – PCK Programmable Clock x Output Status

Value	Description
0	The corresponding Programmable Clock output is disabled.
1	The corresponding Programmable Clock output is enabled.

Bit 5 – USBCLK USB FS Clock Status

Value	Description
0	The USB FS clock is disabled.
1	The USB FS clock is enabled.

Bit 0 – HCLKS HCLK Status

Value	Description
0	HCLK is disabled.
1	HCLK is enabled.

31.20.11 PMC Master Clock Register

Name: PMC_MCKR
Offset: 0x0030
Reset: 0x00000001
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

UPLLDIV2	UPLL Clock Division
0	UPLLCK frequency is divided by 1.
1	UPLLCK frequency is divided by 2.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access			UPLLDIV2				MDIV[1:0]	
Reset			0				0	0

Bit	7	6	5	4	3	2	1	0
Access		PRES[2:0]					CSS[1:0]	
Reset		0	0	0			0	1

Bit 13 – UPLLDIV2 UPLL Divider by 2

Bits 9:8 – MDIV[1:0] Master Clock Division

Value	Name	Description
0	EQ_PCK	MCK is FCLK divided by 1.
1	PCK_DIV2	MCK is FCLK divided by 2.
2	PCK_DIV4	MCK is FCLK divided by 4.
3	PCK_DIV3	MCK is FCLK divided by 3.

Bits 6:4 – PRES[2:0] Processor Clock Prescaler

Value	Name	Description
0	CLK_1	Selected clock
1	CLK_2	Selected clock divided by 2
2	CLK_4	Selected clock divided by 4

34.7.3 SDRAMC Configuration Register

Name: SDRAMC_CR
Offset: 0x08
Reset: 0x852372C0
Property: Read/Write

WARNING Bit 7 (DBW) must always be set when programming the SDRAMC_CR.

Bit	31	30	29	28	27	26	25	24
	TXSR[3:0]				TRAS[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	1	0	1

Bit	23	22	21	20	19	18	17	16
	TRCD[3:0]				TRP[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	1	1

Bit	15	14	13	12	11	10	9	8
	TRC_TRFC[3:0]				TWR[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	1	0	0	1	0

Bit	7	6	5	4	3	2	1	0
	DBW	CAS[1:0]		NB	NR[1:0]		NC[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	0	0	0	0	0	0

Bits 31:28 – TXSR[3:0] Exit Self-Refresh to Active Delay
Reset value is eight cycles.

This field defines the delay between SCKE set high and an Activate Command in number of cycles. Number of cycles is between 0 and 15.

Bits 27:24 – TRAS[3:0] Active to Precharge Delay
Reset value is five cycles.

This field defines the delay between an Activate Command and a Precharge Command in number of cycles. Number of cycles is between 0 and 15.

Bits 23:20 – TRCD[3:0] Row to Column Delay
Reset value is two cycles.

This field defines the delay between an Activate Command and a Read/Write Command in number of cycles. Number of cycles is between 0 and 15.

Bits 19:16 – TRP[3:0] Row Precharge Delay
Reset value is three cycles.

35.16.1.7 SMC Off-Chip Memory Scrambling Key2 Register

Name: SMC_KEY2
Offset: 0x88
Reset: 0x00000000
Property: Write-once

Notes: 1. ‘Write-once’ access indicates that the first write access after a system reset prevents any further modification of the value of this register.

Bit	31	30	29	28	27	26	25	24
	KEY2[31:24]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	KEY2[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	KEY2[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	KEY2[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – KEY2[31:0] Off-Chip Memory Scrambling (OCMS) Key Part 2
When off-chip memory scrambling is enabled, KEY1 and KEY2 values determine data scrambling.

36.9.16 XDMAC Global Channel Software Request Status Register

Name: XDMAC_GSWS
Offset: 0x3C
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	SWRS23	SWRS22	SWRS21	SWRS20	SWRS19	SWRS18	SWRS17	SWRS16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	SWRS15	SWRS14	SWRS13	SWRS12	SWRS11	SWRS10	SWRS9	SWRS8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	SWRS7	SWRS6	SWRS5	SWRS4	SWRS3	SWRS2	SWRS1	SWRS0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23 – SWRS XDMAC Channel x Software Request Status

Value	Description
0	Channel x source request is serviced.
1	Channel x source request is pending.

38.8.48 GMAC 512 to 1023 Byte Frames Transmitted Register

Name: GMAC_TBFT1023
Offset: 0x128
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	NFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFTX[31:0] 512 to 1023 Byte Frames Transmitted without Error
This register counts the number of 512 to 1023 byte frames successfully transmitted without error, i.e., no underrun and not too many retries.

38.8.105 GMAC Credit-Based Shaping Control Register

Name: GMAC_CBSCR
Offset: 0x4BC
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							QAE	QBE
Access								
Reset							0	0

Bit 1 – QAE Queue A CBS Enable

Value	Description
0	Credit-based shaping on the second highest priority queue (queue A) is disabled.
1	Credit-based shaping on the second highest priority queue (queue A) is enabled.

Bit 0 – QBE Queue B CBS Enable

Value	Description
0	Credit-based shaping on the highest priority queue (queue B) is disabled.
1	Credit-based shaping on the highest priority queue (queue B) is enabled.

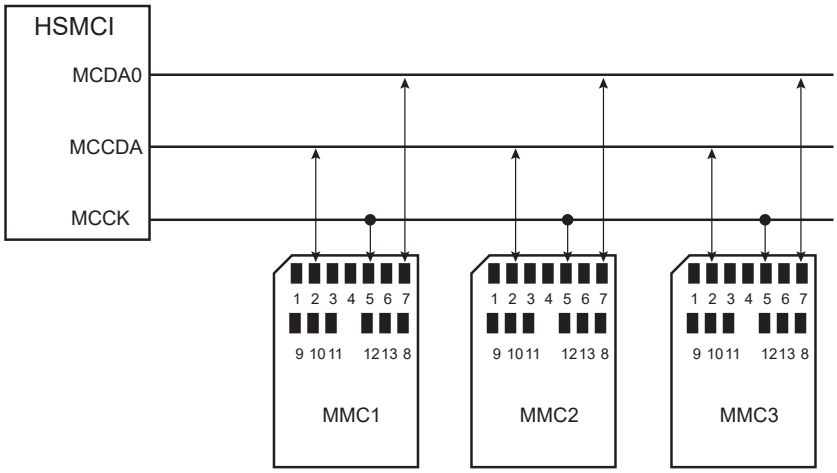
Table 40-2. Bus Topology

Pin Number	Name	Type[1]	Description	HSMCI Pin Name[2] (Slot z)
1	DAT[3]	I/O/PP	Data	MCDz3
2	CMD	I/O/PP/OD	Command/response	MCCDz
3	VSS1	S	Supply voltage ground	VSS
4	VDD	S	Supply voltage	VDD
5	CLK	I/O	Clock	MCCK
6	VSS2	S	Supply voltage ground	VSS
7	DAT[0]	I/O/PP	Data 0	MCDz0
8	DAT[1]	I/O/PP	Data 1	MCDz1
9	DAT[2]	I/O/PP	Data 2	MCDz2

Notes: 1. I: Input, O: Output, PP: Push/Pull, OD: Open Drain, S: Supply

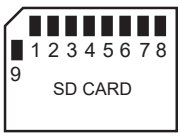
2. When several HSMCI (x HSMCI) are embedded in a product, MCCK refers to HSMCIx_CK, MCCDA to HSMCIx_CDA, MCDAy to HSMCIx_DAy.

Figure 40-4. MMC Bus Connections (One Slot)



Note: When several HSMCI (x HSMCI) are embedded in a product, MCCK refers to HSMCIx_CK, MCCDA to HSMCIx_CDA MCDAy to HSMCIx_DAy.

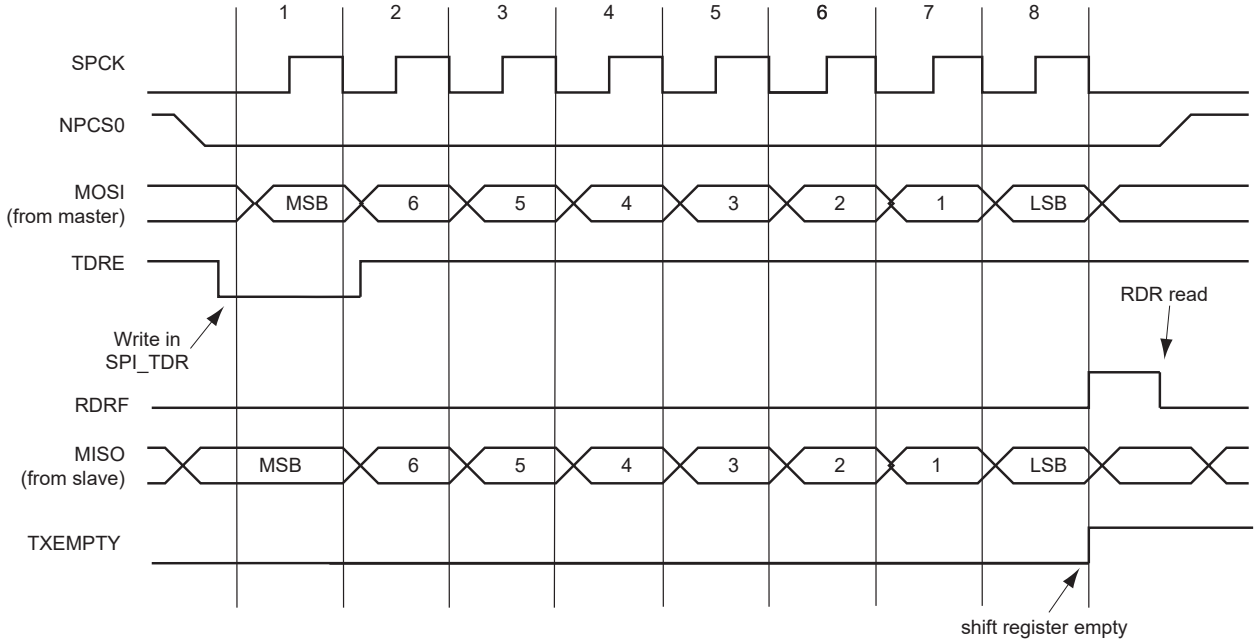
Figure 40-5. SD Memory Card Bus Topology



The SD Memory Card bus includes the signals listed in Table 1-6.

The figure below shows the behavior of Transmit Data Register Empty (TDRE), Receive Data Register (RDRF) and Transmission Register Empty (TXEMPTY) status flags within SPI_SR during an 8-bit data transfer in Fixed mode without the DMA involved.

Figure 41-8. Status Register Flags Behavior



41.7.3.3 Clock Generation

The SPI Baud rate clock is generated by dividing the peripheral clock by a value between 1 and 255.

If SPI_CSRx.SCBR is programmed to 1, the operating baud rate is peripheral clock (refer to the section “Electrical Characteristics” for the SPCK maximum frequency). Triggering a transfer while SPI_CSRx.SCBR is at 0 can lead to unpredictable results.

At reset, SPI_CSRx.SCBR=0 and the user has to program it to a valid value before performing the first transfer.

The divisor can be defined independently for each chip select, as it has to be programmed in SPI_CSRx.SCBR. This allows the SPI to automatically adapt the baud rate for each interfaced peripheral without reprogramming.

Related Links

58. Electrical Characteristics for SAM V70/V71

41.7.3.4 Transfer Delays

The following figure shows a chip select transfer change and consecutive transfers on the same chip select. Three delays can be programmed to modify the transfer waveforms:

- Delay between the chip selects—programmable only once for all chip selects by writing field SPI_MR.DLYBCS. The SPI slave device deactivation delay is managed through DLYBCS. If there is only one SPI slave device connected to the master, DLYBCS does not need to be configured. If several slave devices are connected to a master, DLYBCS must be configured depending on the highest deactivation delay. Refer to details on the SPI slave device in the section “Electrical Characteristics”.

41.8.3 SPI Receive Data Register

Name: SPI_RDR
Offset: 0x08
Reset: 0x0
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					PCS[3:0]			
Access					R	R	R	R
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 19:16 – PCS[3:0] Peripheral Chip Select
In Master mode only, these bits indicate the value on the NPCS pins at the end of a transfer. Otherwise, these bits are read as zero.

When using Variable Peripheral Select mode (PS = 1 in SPI_MR), it is mandatory to set SPI_MR.WDRBT bit if the PCS field must be processed in SPI_RDR.

Bits 15:0 – RD[15:0] Receive Data
Data received by the SPI Interface is stored in this register in a right-justified format. Unused bits are read as zero.

Bit 17 – ACMDIS Alternative Command Mode Disable

Value	Description
0	No effect.
1	Alternative Command mode disabled.

Bit 16 – ACMEN Alternative Command Mode Enable

Value	Description
0	No effect.
1	Alternative Command mode enabled.

Bit 15 – CLEAR Bus CLEAR Command

Value	Description
0	No effect.
1	If Master mode is enabled, sends a bus clear command.

Bit 14 – PECRQ PEC Request

Value	Description
0	No effect.
1	A PEC check or transmission is requested.

Bit 13 – PECDIS Packet Error Checking Disable

Value	Description
0	No effect.
1	SMBus PEC (CRC) generation and check disabled.

Bit 12 – PECEN Packet Error Checking Enable

Value	Description
0	No effect.
1	SMBus PEC (CRC) generation and check enabled.

Bit 11 – SMBDIS SMBus Mode Disabled

Value	Description
0	No effect.
1	SMBus mode disabled.

Bit 10 – SMBEN SMBus Mode Enabled

Value	Description
0	No effect.
1	If SMBDIS = 0, SMBus mode enabled.

Bit 9 – HSDIS TWIHS High-Speed Mode Disabled

Value	Description
0	No effect.
1	High-speed mode disabled.

44.8.3 Receive Operations

A receive frame is triggered by a start event and can be followed by synchronization data before data transmission.

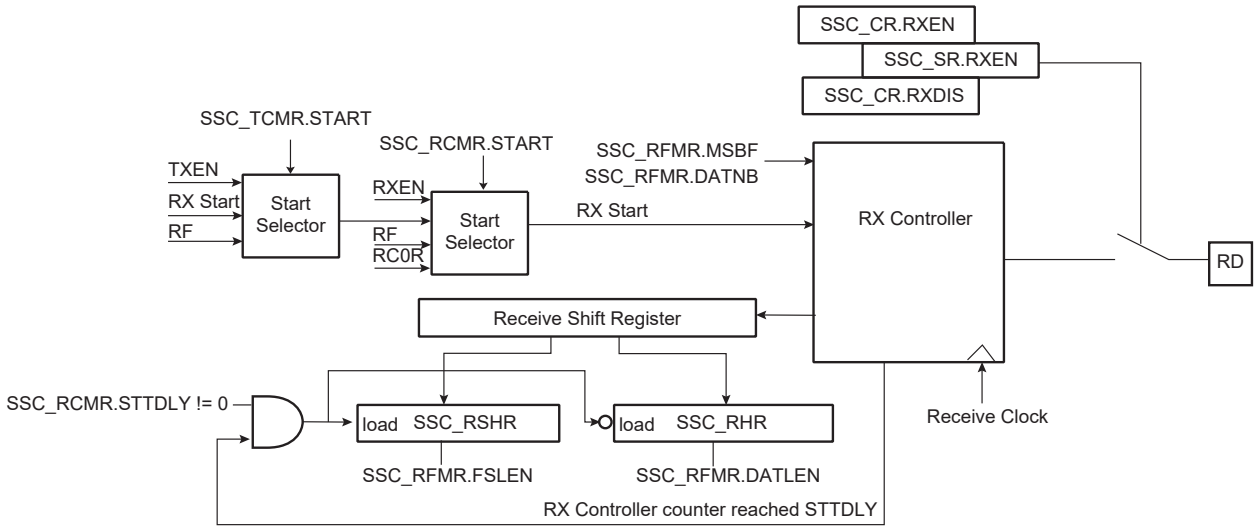
The start event is configured setting the Receive Clock Mode Register (SSC_RCMR). See Start.

The frame synchronization is configured by setting the Receive Frame Mode Register (SSC_RFMR). See Frame Synchronization.

The receiver uses a shift register clocked by the receive clock signal and the start mode selected in the SSC_RCMR. The data is transferred from the shift register depending on the data format selected.

When the receiver shift register is full, the SSC transfers this data in the holding register, the status flag RXRDY is set in the SSC_SR and the data can be read in the receiver holding register. If another transfer occurs before read of the Receive Holding Register (SSC_RHR), the status flag OVERUN is set in the SSC_SR and the receiver shift register is transferred in the SSC_RHR.

Figure 44-12. Receive Block Diagram



44.8.4 Start

The transmitter and receiver can both be programmed to start their operations when an event occurs, respectively in the Transmit Start Selection (START) field of SSC_TCMR and in the Receive Start Selection (START) field of SSC_RCMR.

Under the following conditions the start event is independently programmable:

- Continuous. In this case, the transmission starts as soon as a word is written in SSC_THR and the reception starts as soon as the receiver is enabled.
- Synchronously with the transmitter/receiver
- On detection of a falling/rising edge on TF/RF
- On detection of a low level/high level on TF/RF
- On detection of a level change or an edge on TF/RF

A start can be programmed in the same manner on either side of the Transmit/Receive Clock Register (SSC_RCMR/SSC_TCMR). Thus, the start could be on TF (Transmit) or RF (Receive).

Moreover, the receiver can start when data is detected in the bit stream with the Compare Functions.

Table 48-5. MediaLB RxStatus Responses

Value (see Note)	Command	Description
Normal Commands (TX Device sends in non-system channels):		
00h	NoData	No data to send out in this physical channel.
02h...0Eh	rsvd	Reserved
10h	SyncData	Tx Device sends out SyncData command to indicate synchronous stream data.
12h...1Eh	rsvd	Reserved
20h	AsyncStart	Asynchronous logical channel. Start of a packet.
22h	AsyncContinue	Asynchronous logical channel. Middle of a packet.
24h	AsyncEnd	Asynchronous logical channel. End of a packet.
26h	AsyncBreak	Asynchronous logical channel. Indicates a packet stop. No valid data present on the MLBD line.
28h...2Eh	rsvd	Reserved
30h	ControlStart	Control logical channel. Start of a message.
32h	ControlContinue	Control logical channel. Middle of a message.
34h	ControlEnd	Control logical channel. End of a message.
36h	ControlBreak	Control logical channel. Indicates a message stop. No valid data present on the MLBD line.
38h...3Eh	rsvd	Reserved
40h	IsoNoData	Isochronous logical channel, no data valid.
42h	Iso1Byte	Isochronous logical channel, one data byte valid. First byte (MSB) transmitted/received is valid. Last three bytes in physical channel are empty.
44h	Iso2Bytes	Isochronous logical channel, first two data bytes valid. First byte transmitted/received is the MSB. Last two bytes in physical channel are empty.
46h	Iso3Bytes	Isochronous logical channel, first three data bytes valid. First byte transmitted/received is the MSB. Last byte in physical channel is empty.
48h	Iso4Bytes	Isochronous logical channel, all four data bytes valid. First byte transmitted/received is the MSB.
4Ah...4Eh	rsvd	Reserved
50h	IsoSync1Byte	Isochronous logical channel, one data byte valid and start of a block. First byte transmitted/received is valid. Last three bytes in physical channel are empty.

49.5.5.4 Tx Queue

Tx Queue operation is configured by programming MCAN_TXBC.TFQM to '1'. Messages stored in the Tx Queue are transmitted starting with the message with the lowest Message ID (highest priority). In case that multiple Queue Buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

New messages have to be written to the Tx Buffer referenced by the Put Index MCAN_TXFQS.TFQPI. An Add Request cyclically increments the Put Index to the next free Tx Buffer. In case that the Tx Queue is full (MCAN_TXFQS.TFQF = '1'), the Put Index is not valid and no further message should be written to the Tx Queue until at least one of the requested messages has been sent out or a pending transmission request has been cancelled.

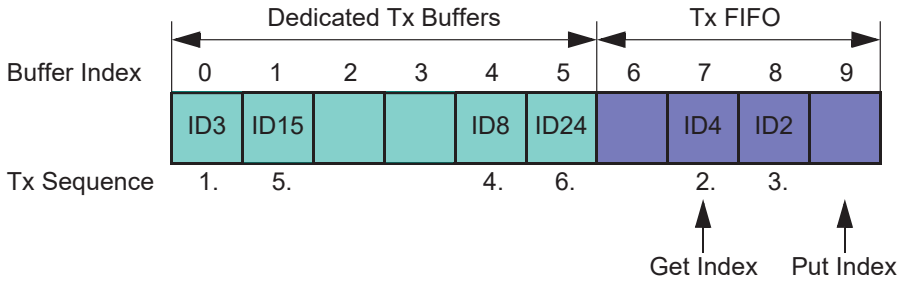
The application may use register MCAN_TXBRP instead of the Put Index and may place messages to any Tx Buffer without pending transmission request.

A Tx Queue Buffer allocates Element Size 32-bit words in the Message RAM (see the table Tx Buffer / FIFO / Queue Element Size). Therefore the start address of the next available (free) Tx Queue Buffer is calculated by adding Tx FIFO/Queue Put Index MCAN_TXFQS.TFQPI (0…31) × Element Size to the Tx Buffer Start Address MCAN_TXBC.TBSA.

49.5.5.5 Mixed Dedicated Tx Buffers / Tx FIFO

In this case the Tx Buffers section in the Message RAM is subdivided into a set of dedicated Tx Buffers and a Tx FIFO. The number of dedicated Tx Buffers is configured by MCAN_TXBC.NDTB. The number of Tx Buffers assigned to the Tx FIFO is configured by MCAN_TXBC.TFQS. In case MCAN_TXBC.TFQS is programmed to zero, only dedicated Tx Buffers are used.

Figure 49-10. Example of Mixed Configuration Dedicated Tx Buffers / Tx FIFO



Tx prioritization:

- Scan dedicated Tx Buffers and oldest pending Tx FIFO Buffer (referenced by MCAN_TXFS.TFGI)
- Buffer with lowest Message ID gets highest priority and is transmitted next

49.5.5.6 Mixed Dedicated Tx Buffers / Tx Queue

In this case the Tx Buffers section in the Message RAM is subdivided into a set of dedicated Tx Buffers and a Tx Queue. The number of dedicated Tx Buffers is configured by MCAN_TXBC.NDTB. The number of Tx Queue Buffers is configured by MCAN_TXBC.TFQS. In case MCAN_TXBC.TFQS is programmed to zero, only dedicated Tx Buffers are used.

52.7.6 AFEC Channel Enable Register

Name: AFEC_CHER
Offset: 0x14
Reset: –
Property: Write-only

This register can only be written if the WPEN bit is cleared in the AFEC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					CH11	CH10	CH9	CH8
Access					W	W	W	W
Reset					–	–	–	–

Bit	7	6	5	4	3	2	1	0
	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 – CHx Channel x Enable
If AFEC_MR.USEQ = 1, CHx corresponds to the xth channel of the sequence described in AFEC_SEQ1R, AFEC_SEQ2R.

Value	Description
0	No effect.
1	Enables the corresponding channel.

Offset	Name	Bit Pos.								
0x8C	AES_TAGR1	7:0	TAG[7:0]							
		15:8	TAG[15:8]							
		23:16	TAG[23:16]							
		31:24	TAG[31:24]							
0x90	AES_TAGR2	7:0	TAG[7:0]							
		15:8	TAG[15:8]							
		23:16	TAG[23:16]							
		31:24	TAG[31:24]							
0x94	AES_TAGR3	7:0	TAG[7:0]							
		15:8	TAG[15:8]							
		23:16	TAG[23:16]							
		31:24	TAG[31:24]							
0x98	AES_CTRR	7:0	CTR[7:0]							
		15:8	CTR[15:8]							
		23:16	CTR[23:16]							
		31:24	CTR[31:24]							
0x9C	AES_GCMHR0	7:0	H[7:0]							
		15:8	H[15:8]							
		23:16	H[23:16]							
		31:24	H[31:24]							
0xA0	AES_GCMHR1	7:0	H[7:0]							
		15:8	H[15:8]							
		23:16	H[23:16]							
		31:24	H[31:24]							
0xA4	AES_GCMHR2	7:0	H[7:0]							
		15:8	H[15:8]							
		23:16	H[23:16]							
		31:24	H[31:24]							
0xA8	AES_GCMHR3	7:0	H[7:0]							
		15:8	H[15:8]							
		23:16	H[23:16]							
		31:24	H[31:24]							

where, C_{PCB} is the capacitance of the printed circuit board (PCB) track layout from the crystal to the pin.

58.4.7 3 to 20 MHz Crystal Characteristics

Table 58-24. 3 to 20 MHz Crystal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistor	Fundamental at 3 MHz	–	–	150	Ohm
		Fundamental at 8 MHz			140	
		Fundamental at 12 MHz			120	
		Fundamental at 16 MHz			80	
		Fundamental at 20 MHz			50	
C_M	Motional capacitance	Fundamental at 3 MHz	3	–	8	fF
		Fundamental at 8–20 MHz	1.6	–	8	
C_{SHUNT}	Shunt capacitance	–	–	–	7	pF
$C_{CRYSTAL}$	Allowed Crystal Capacitance Load	From crystal specification	12.5	–	17.5	pF
P_{ON}	Drive Level	3 MHz	–	–	15	µW
		8 MHz	–	–	30	
		12 MHz, 20 MHz	–	–	50	

58.4.8 3 to 20 MHz XIN Clock Input Characteristics in Bypass Mode

Table 58-25. 3 to 20 MHz XIN Clock Input Characteristics in Bypass Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPXIN})$	XIN Clock Frequency	(see **Note 1**)	–	–	20	MHz
t_{CHXIN}	XIN Clock High Half-period	(see **Note 1**)	25	–	–	ns
t_{CLXIN}	XIN Clock Low Half-period	(see **Note 1**)	25	–	–	ns
V_{XIN_IL}	V_{XIN} Input Low-level Voltage	(see **Note 1**)	Min of V_{IL} for CLOCK pad	–	Max of V_{IL} for CLOCK pad	V
V_{XIN_IH}	V_{XIN} Input High-level Voltage	(see **Note 1**)	Min of V_{IH} for CLOCK pad	–	Max of V_{IH} for CLOCK pad	V

Note:

1. These characteristics apply only when the 3–20 MHz crystal oscillator is in Bypass mode.

58.4.9 Crystal Oscillator Design Considerations

58.4.9.1 Choosing a Crystal

When choosing a crystal for the 32768 Hz Slow Clock Oscillator or for the 3–20 MHz oscillator, several parameters must be taken into account. Important parameters between crystal and product specifications are as follows: