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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv71n19b-aabt

Function	Application	Description	Event Source	Event Destination
	Motor control	Puts the PWM outputs in Safe mode (overspeed detection through timer quadrature decoder) (see **Notes 2, 6**)	TC0	PWM0
			TC1	PWM1
	General-purpose, motor control, power factor correction (PFC)	Puts the PWM outputs in Safe mode (general-purpose fault inputs) (see **Note 2**)	PIO PA9, PD8, PD9	PWM0
			PIO PA21, PA26, PA28	PWM1
Security	General-purpose	Immediate GPBR clear (asynchronous) on tamper detection through WKUP0/1 IO pins (see **Note 5**)	PIO WKUP0/1	GPBR
Measurement trigger	Power factor correction (DC-DC, lighting, etc.)	Duty cycle output waveform correction Trigger source selection in PWM (see **Notes 7, 8**)	ACC	PWM0
			PIO PA10, PA22	PWM0
			ACC	PWM1
			PIO PA30, PA18	PWM1
	General-purpose	Trigger source selection in AFEC (see **Note 9**)	PIO AFE0_ADTRG	AFEC0
			TC0 TIOA0	AFEC0
			TC0 TIOA1	AFEC0
			TC0 TIOA2	AFEC0
			ACC	AFEC0
	Motor control	ADC-PWM synchronization (see **Notes 12, 14**) Trigger source selection in AFEC (see **Note 9**)	PWM0 Event Line 0 and 1	AFEC0
	General-purpose	Trigger source selection in AFEC (see **Note 9**)	PIO AFE1_ADTRG	AFEC1
			TC1 TIOA3	AFEC1
			TC1 TIOA4	AFEC1
			TC1 TIOA5	AFEC1
			ACC	AFEC1
	Motor control	ADC-PWM synchronization (see **Notes 12, 14**) Trigger source selection in AFEC (see **Note 9**)	PWM1 Event Line 0 and 1	AFEC1

19.4.3 Bus Matrix Priority Registers A For Slaves

Name: MATRIX_PRASx
Offset: 0x80 + x*0x08 [x=0..8]
Reset: 0x00000222
Property: Read/Write

This register can only be written if the WPE bit is cleared in the Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
			M7PR[1:0]				M6PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	23	22	21	20	19	18	17	16
			M5PR[1:0]				M4PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	15	14	13	12	11	10	9	8
			M3PR[1:0]				M2PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			0	0			1	0

Bit	7	6	5	4	3	2	1	0
			M1PR[1:0]				M0PR[1:0]	
Access			R/W	R/W			R/W	R/W
Reset			1	0			1	0

Bits 0:1, 4:5, 8:9, 12:13, 16:17, 20:21, 24:25, 28:29 – MxPR Master x Priority
Fixed priority of Master x for accessing the selected slave. The higher the number, the higher the priority.

All the masters programmed with the same MxPR value for the slave make up a priority pool.

Round-robin arbitration is used in the lowest (MxPR = 0) and highest (MxPR = 3) priority pools.

Fixed priority is used in intermediate priority pools (MxPR = 1) and (MxPR = 2).

See “Arbitration Priority Scheme” for details.

21.3.2 Chip ID Extension Register

Name: CHIPID_EXID
Offset: 0x4
Reset: -
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	EXID[31:24]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	23	22	21	20	19	18	17	16
	EXID[23:16]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	15	14	13	12	11	10	9	8
	EXID[15:8]							
Access	R	R	R	R	R	R	R	R
Reset								

Bit	7	6	5	4	3	2	1	0
	EXID[7:0]							
Access	R	R	R	R	R	R	R	R
Reset								

Bits 31:0 – EXID[31:0] Chip ID Extension
This field is cleared if CHIPID_CIDR.EXT = 0.

Value	Name	Description
0xX	Reserved	Reserved

Bit 16 – UECCELSB Unique ECC Error on LSB Part of the Memory Flash Data Bus (cleared on read)

Value	Description
0	No unique error detected on 64 LSB data bus of the Flash memory since the last read of EEFC_FSR.
1	One unique error detected but corrected on 64 LSB data bus of the Flash memory since the last read of EEFC_FSR.

Bit 3 – FLERR Flash Error Status (cleared when a programming operation starts)

Value	Description
0	No Flash memory error occurred at the end of programming (EraseVerify or WriteVerify test has passed).
1	A Flash memory error occurred at the end of programming (EraseVerify or WriteVerify test has failed).

Bit 2 – FLOCKE Flash Lock Error Status (cleared on read)
This flag is automatically cleared when EEFC_FSR is read or EEFC_FCR is written.

Value	Description
0	No programming/erase of at least one locked region has happened since the last read of EEFC_FSR.
1	Programming/erase of at least one locked region has happened since the last read of EEFC_FSR.

Bit 1 – FCMDE Flash Command Error Status (cleared on read or by writing EEFC_FCR)

Value	Description
0	No invalid commands and no bad keywords were written in EEFC_FMR.
1	An invalid command and/or a bad keyword was/were written in EEFC_FMR.

Bit 0 – FRDY Flash Ready Status (cleared when Flash is busy)
When set, this flag triggers an interrupt if the FRDY flag is set in EEFC_FMR.

This flag is automatically cleared when the EEFC is busy.

Value	Description
0	The EEFC is busy.
1	The EEFC is ready to start a new command.

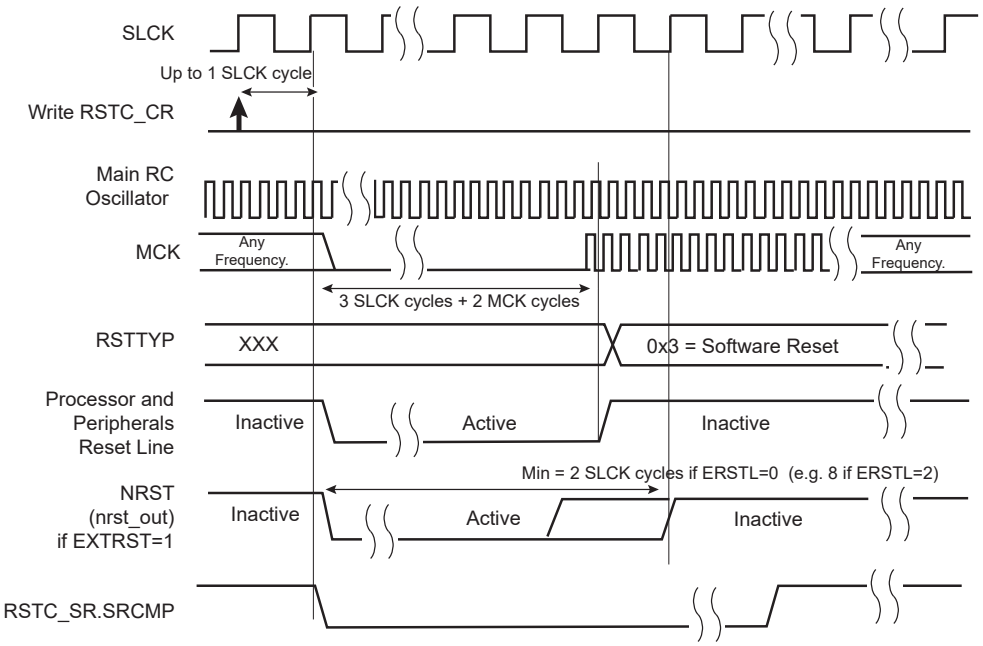
The internal reset signals are asserted as soon as the register write is performed. This is detected on the Master Clock (MCK). They are released when the software reset has ended, i.e., synchronously to SLCK.

If EXTRST is written to ‘1’, the nrst_out signal is asserted depending on the configuration of RSTC_MR.ERSTL. However, the resulting falling edge on NRST does not lead to a user reset.

If and only if the RSTC_CR.PROCRST is written to ‘1’, the RSTC reports the software status in field RSTC_SR.RSTTYP. Other software resets are not reported in RSTTYP.

As soon as a software operation is detected, RSTC_SR.SRCMP is written to ‘1’. SRCMP is cleared at the end of the software reset. No other software reset can be performed while SRCMP is written to ‘1’, and writing any value in the RSTC_CR has no effect.

Figure 26-5. Software Reset Timing Diagram



26.4.3.5 User Reset

A user reset is generated when a low level is detected on the NRST pin and RSTC_MR.URSTEN is at ‘1’. The NRST input signal is resynchronized with SLCK to ensure proper behavior of the system. Thus, the NRST pin must be asserted for at least 1 SLCK clock cycle to ensure execution of a user reset.

The user reset is triggered 2 SLCK cycles after a low level is detected on NRST. The processor reset and the peripheral reset are asserted.

The user reset ends when NRST rises, after a two-cycle resynchronization time and a three-cycle processor startup. The processor clock is reenabled as soon as NRST is confirmed high.

When the processor reset signal is released, RSTC_SR.RSTTYP is loaded with the value ‘4’, indicating a user reset.

The NRST manager guarantees that the NRST line is asserted for External Reset Length SLCK cycles, as configured in RSTC_MR.ERSTL. However, if NRST does not rise after External Reset Length because it is driven low externally, the internal reset lines remain asserted until NRST actually rises.

31.20.31 PMC SleepWalking Disable Register 1

Name: PMC_SLPWK_DR1
Offset: 0x0138
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
		PID62		PID60	PID59	PID58	PID57	PID56
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
			PID53	PID52	PID51	PID50	PID49	PID48
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	PID47	PID46	PID45	PID44	PID43	PID42	PID41	PID40
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	PID39		PID37		PID35	PID34	PID33	PID32
Access								
Reset								

Bits 0:3,5,7:28,30 – PID Peripheral Clock x Disable

Value	Description
0	No effect.
1	Disables the corresponding peripheral clock.

34.7.5 SDRAMC Interrupt Enable Register

Name: SDRAMC_IER
Offset: 0x14
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
Access								W
Reset								RES

Bit 0 – RES Refresh Error Interrupt Enable

Value	Description
0	No effect.
1	Enables the refresh error interrupt.

35.16.1.4 SMC Mode Register

Name: SMC_MODE[0..3]
Offset: 0x00
Reset: 0
Property: R/W

This register can only be written if the WPEN bit is cleared in the "SMC Write Protection Mode Register" .

The user must confirm the SMC configuration by writing any one of the SMC_MODE registers.

Bit	31	30	29	28	27	26	25	24
			PS[1:0]					PMEN
Access								
Reset			0	0				0

Bit	23	22	21	20	19	18	17	16
				TDF_MODE	TDF_CYCLES[3:0]			
Access								
Reset				0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
				DBW				BAT
Access								
Reset				0				0

Bit	7	6	5	4	3	2	1	0
			EXNW_MODE[1:0]				WRITE_MODE	READ_MODE
Access								
Reset			0	0			0	0

Bits 29:28 – PS[1:0] Page Size
If page mode is enabled, this field indicates the size of the page in bytes.

Value	Name	Description
0	4_BYTE	4-byte page
1	8_BYTE	8-byte page
2	16_BYTE	16-byte page
3	32_BYTE	32-byte page

Bit 24 – PMEN Page Mode Enabled

Value	Description
0	Standard read is applied.
1	Asynchronous burst read in page mode is applied on the corresponding chip select.

Bit 20 – TDF_MODE TDF Optimization

Value	Description
0	Codec channel fetch operation is disabled.
1	Codec channel fetch operation is enabled.

Value	Description
0	Wake on LAN magic packet Event disabled
1	Wake on LAN magic packet Event enabled

Bits 15:0 – IP[15:0] ARP Request IP Address
Wake on LAN ARP request IP address. Written to define the 16 least significant bits of the target IP address that is matched to generate a Wake on LAN event.

Value	Description
0x0000	No Event generated, even if matched by the received frame.
0x0001-0xFFFF	Wake on LAN Event generated for matching LSB of the target IP address.

38.8.107 GMAC Credit-Based Shaping IdleSlope Register for Queue B

Name: GMAC_CBSISQB
Offset: 0x4C4
Reset: 0x00000000
Property: Read/Write

Credit-based shaping must be disabled in the GMAC_CBSCR before updating this register.

Bit	31	30	29	28	27	26	25	24
	IS[31:24]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	IS[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	IS[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IS[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – IS[31:0] IdleSlope
IdleSlope value for queue B in bytes/second.

The IdleSlope value is defined as the rate of change of credit when a packet is waiting to be sent. This must not exceed the port transmit rate which is dependent on the speed of operation, e.g., 100 Mb/second = 32'h017D7840.

If 50% of bandwidth was to be allocated to a particular queue in 100 Mb/sec mode, then the IdleSlope value for that queue would be calculated as 32'h017D7840 / 2

Offset	Name	Bit Pos.								
		15:8		FIFOCONC		NBUSYBKEC		ERRORTRANSEC	DATAXEC	MDATEC
		23:16								EPDISHDMAC
		31:24								
0x0230	USBHS_DEVEPTIDR4	7:0	SHORTPACKETEC	STALLEDEC	OVERFEC	NAKINEC	NAKOUTEC	RXSTPEC	RXOUTEC	TXINEC
		15:8		FIFOCONC		NBUSYBKEC				
		23:16					STALLRQC		NYETDISC	EPDISHDMAC
		31:24								
0x0230	USBHS_DEVEPTIDR4 (ISOENPT)	7:0	SHORTPACKETEC	CRCERREC	OVERFEC	HBISOFLUSHEC	HBISOINERREC	UNDERFEC	RXOUTEC	TXINEC
		15:8		FIFOCONC		NBUSYBKEC		ERRORTRANSEC	DATAXEC	MDATEC
		23:16								EPDISHDMAC
		31:24								
0x0234	USBHS_DEVEPTIDR5	7:0	SHORTPACKETEC	STALLEDEC	OVERFEC	NAKINEC	NAKOUTEC	RXSTPEC	RXOUTEC	TXINEC
		15:8		FIFOCONC		NBUSYBKEC				
		23:16					STALLRQC		NYETDISC	EPDISHDMAC
		31:24								
0x0234	USBHS_DEVEPTIDR5 (ISOENPT)	7:0	SHORTPACKETEC	CRCERREC	OVERFEC	HBISOFLUSHEC	HBISOINERREC	UNDERFEC	RXOUTEC	TXINEC
		15:8		FIFOCONC		NBUSYBKEC		ERRORTRANSEC	DATAXEC	MDATEC
		23:16								EPDISHDMAC
		31:24								
0x0238	USBHS_DEVEPTIDR6	7:0	SHORTPACKETEC	STALLEDEC	OVERFEC	NAKINEC	NAKOUTEC	RXSTPEC	RXOUTEC	TXINEC
		15:8		FIFOCONC		NBUSYBKEC				
		23:16					STALLRQC		NYETDISC	EPDISHDMAC
		31:24								
0x0238	USBHS_DEVEPTIDR6 (ISOENPT)	7:0	SHORTPACKETEC	CRCERREC	OVERFEC	HBISOFLUSHEC	HBISOINERREC	UNDERFEC	RXOUTEC	TXINEC
		15:8		FIFOCONC		NBUSYBKEC		ERRORTRANSEC	DATAXEC	MDATEC
		23:16								EPDISHDMAC
		31:24								
0x023C	USBHS_DEVEPTIDR7	7:0	SHORTPACKETEC	STALLEDEC	OVERFEC	NAKINEC	NAKOUTEC	RXSTPEC	RXOUTEC	TXINEC
		15:8		FIFOCONC		NBUSYBKEC				

40.14.16 HSMCI DMA Configuration Register

Name: HSMCI_DMA
Offset: 0x50
Reset: 0x0
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the HSMCI Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								DMAEN
Reset								0

Bit	7	6	5	4	3	2	1	0
Access		CHKSIZE[2:0]						
Reset		0	0	0				

Bit 8 – DMAEN DMA Hardware Handshaking Enable

Value	Description
0	DMA interface is disabled.
1	DMA Interface is enabled. Note: To avoid unpredictable behavior, DMA hardware handshaking must be disabled when CPU transfers are performed.

Bits 324:4 – CHKSIZE[320:0] DMA Channel Read and Write Chunk Size
The CHKSIZE field indicates the number of data available when the DMA chunk transfer request is asserted.

Value	Name	Description
0	1	1 data available
1	2	2 data available
2	4	4 data available
3	8	8 data available
4	16	16 data available

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
96	RSTS[4]	WSTS[4]	rsvd		BD[11:0]											
112	Reserved		BA[13:0]													

Table 48-19. Asynchronous/Control CDT Entry Field Definitions

Field	Description	Details	Accessibility
BA	Buffer Base Address	- BA can start at any byte in the 16k DBR	r,w
BD	Buffer Depth	- BD = size of buffer in bytes - 1 - Buffer end address = BA + BD - BD ≥ max packet length - 1	r,w
RPC	Read Packet Count	- Software initializes to zero, hardware updates - Used in conjunction with WPC, RPTR and WPTR to determine if the buffer is empty or full	r,w,u (1)
WPC	Write Packet Count	- Software initializes to zero, hardware updates - Used in conjunction with RPC, RPTR and WPTR to determine if the buffer is empty or full	r,w,u (1)
RPTR	Read Pointer	- Software initializes to zero, hardware updates - Counts the read address offset within a buffer - DMA read address = BA + RPTR	r,w,u (1)
WPTR	Write Pointer	- Software initializes to zero, hardware updates - Counts the write address offset within a buffer - DMA read address = BA + WPTR	r,w,u (1)
RSTS	Read Status	- Software initializes to zero, hardware updates - Status states:(2) x0x00 = idle xx1xx = ReceiverProtocolError response received from Rx Device 1xxxx = ReceiverBreak command received from Rx Device	r,w,u (1)
WSTS	Write Status	- Software initializes to zero, hardware updates - Status states:(2) x0x00 = idle xx1xx = command protocol error detected	r,w,u (1)

4.2.2. For isochronous channels: (BD2 + 1) mod (BS + 1) = 0
4.2.3. For asynchronous channels: 5 ≤ (BD2 + 1) ≤ 4096 (max packet length)
4.2.4. For control channels: 5 ≤ (BD2 + 1) ≤ 4096 (max packet length)
4.3. For asynchronous and control Tx channels set the packet start bit (PS2) if the page contains the start of the packet
4.4. Clear the page done bit (DNE2)
4.5. Clear the error bit (ERR2)
4.6. Set the page ready bit (RDY2)
5. Select Big Endian (LE = 0) or Little Endian (LE = 1)
6. Select the active page: PG = 0 (ping), PG = 1 (pong)
7. Set the channel enable (CE) bit for all active logical channels
8. Repeat steps 2–7 for all active logical channels

Note: All asynchronous and control packets must start with a PMP header. The first two bytes of the PMP header contains the Port Message Length (PML), which defines the length of the message that follows in bytes (not including PML itself). Hardware uses the PML to determine when a packet is complete. Asynchronous and control packets can also be segmented into two or more pages as well as contain multiple packets per page within system memory.

Synchronize and Unmute Synchronous Channel

The MLB_MLBC0 and MLB_MLBC1 registers are accessible directly via APB reads and writes.

1. Check that MediaLB clock is running (MLB_MLBC1.CLKM = 0)
2. If MLB_MLBC1.CLKM = 1, clear the register bit, wait one APB or I/O clock cycle and repeat step 1.
3. Poll for MediaLB lock (MLB_MLBC0.MLBLK = 1)
4. Wait four frames
5. Unmute synchronous channel(s)

48.6.4.2 Channel Servicing

After initialization, each channel will require periodic servicing.

The following software flows can be performed concurrently and in any order:

- Servicing the AHB Block (DMA) Interrupts
- Servicing the MediaLB Interrupts
- Polling for MediaLB System Commands

Servicing the AHB Block (DMA) Interrupts

The MLB_ACMR0, MLB_ACMR1, MLB_ACTL, MLB_ACSR0, and MLB_ACSR1 registers are accessible directly via APB reads and writes.

1. Program the MLB_ACMRn registers to enable interrupts from all active DMA channels.
2. Select the status clear method: MLB_ACTL.SCE = 0 (hardware clears on read), MLB_ACTL.SCE = 1 (software writes a ‘1’ to clear).
3. Select 1 or 2 interrupt signals: MLB_ACTL.SMX = 0 (one interrupt for channels 0–31 on MediaLB IRQ0 and another interrupt for channels 32–63 on MediaLB IRQ1), MLB_ACTL.SMX = 1 (single interrupt for all channels on MediaLB IRQ0).
4. Wait for an interrupt from MediaLB IRQ[1:0].
5. Read the MLB_ACSRn registers to determine which channel or channels are causing the interrupt.

48.7.22 MIF Data Write Enable 3 Register

Name: MLB_MDWE3
Offset: 0x0DC
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	MASK: Bitwise Write Enable for CTR Data - Bits[127:96]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	MASK: Bitwise Write Enable for CTR Data - Bits[127:96]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	MASK: Bitwise Write Enable for CTR Data - Bits[127:96]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MASK: Bitwise Write Enable for CTR Data - Bits[127:96]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – MASK: Bitwise Write Enable for CTR Data - Bits[127:96]
MASK[n] = 1 indicates that CTR data [n] is enabled.

50.7.20 TC QDEC Interrupt Status Register

Name: TC_QISR
Offset: 0xD4
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
								DIR
Access								R
Reset								0

Bit	7	6	5	4	3	2	1	0
					MPE	QERR	DIRCHG	IDX
Access					R	R	R	R
Reset					0	0	0	0

Bit 8 – DIR Direction
Returns an image of the current rotation direction.

Bit 3 – MPE Consecutive Missing Pulse Error

Value	Description
0	The number of consecutive missing pulses has not reached the maximum value specified in MAXCMP since the last read of TC_QISR.
1	An occurrence of MAXCMP consecutive missing pulses has been detected since the last read of TC_QISR.

Bit 2 – QERR Quadrature Error

Value	Description
0	No quadrature error since the last read of TC_QISR.
1	A quadrature error occurred since the last read of TC_QISR.

Bit 1 – DIRCHG Direction Change

Value	Description
0	No change on rotation direction since the last read of TC_QISR.
1	The rotation direction changed since the last read of TC_QISR.

52.7.10 AFEC Interrupt Enable 1 Register

Name: AFEC_IER
Offset: 0x24
Reset: –
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
		TEMPCHG				COMPE	GOVRE	DRDY
Access		W				W	W	W
Reset		–				–	–	–

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
					EOC11	EOC10	EOC9	EOC8
Access					W	W	W	W
Reset					–	–	–	–

Bit	7	6	5	4	3	2	1	0
	EOC7	EOC6	EOC5	EOC4	EOC3	EOC2	EOC1	EOC0
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bit 30 – TEMPCHG Temperature Change Interrupt Enable

Bit 26 – COMPE Comparison Event Interrupt Enable

Bit 25 – GOVRE General Overrun Error Interrupt Enable

Bit 24 – DRDY Data Ready Interrupt Enable

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 – EOCx End of Conversion Interrupt Enable x

57.5.6 AES Interrupt Status Register

Name: AES_ISR
Offset: 0x1C
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								R
Reset								0

Bit	15	14	13	12	11	10	9	8
Access	R	R	R	R				R
Reset	0	0	0	0				0

Bit	7	6	5	4	3	2	1	0
Access								R
Reset								0

Bit 16 – TAGRDY GCM Tag Ready

Value	Description
0	GCM Tag is not valid.
1	GCM Tag generation is complete (cleared by reading GCM Tag, starting another processing or when writing a new key).

Bits 15:12 – URAT[3:0] Unspecified Register Access (cleared by writing SWRST in AES_CR)
Only the last Unspecified Register Access Type is available through the URAT field.

Value	Name	Description
0	IDR_WR_PROCESSING	Input Data register written during the data processing when SMOD = 2 mode.
1	ODR_RD_PROCESSING	Output Data register read during the data processing.
2	MR_WR_PROCESSING	Mode register written during the data processing.
3	ODR_RD_SUBKGEN	Output Data register read during the sub-keys generation.
4	MR_WR_SUBKGEN	Mode register written during the sub-keys generation.
5	WOR_RD_ACCESS	Write-only register read access.

Bit 8 – URAD Unspecified Register Access Detection Status (cleared by writing SWRST in AES_CR)

Table 58-65. SMC Write NCS Controlled (WRITE_MODE = 0)

Symbol		VDDIO Supply		Unit
	Parameter	Min	Max	
SMC_{22}	Data Out Valid before NCS High	NCS_WR_PULSE × t_{CPMCK} - 3.9	–	ns
SMC_{23}	NCS Pulse Width	NCS_WR_PULSE × t_{CPMCK} - 0.2	–	ns
SMC_{24}	A0–A22 valid before NCS low	NCS_WR_SETUP × t_{CPMCK} - 4.6	–	ns
SMC_{25}	NWE low before NCS high	(NCS_WR_SETUP - NWE_SETUP + NCS pulse) × t_{CPMCK} - 4.6	–	ns
SMC_{26}	NCS High to Data Out, A0–A25, change	NCS_WR_HOLD × t_{CPMCK} - 3.4	–	ns
SMC_{27}	NCS High to NWE Inactive	(NCS_WR_HOLD - NWE_HOLD) × t_{CPMCK} - 2.4	–	ns

Figure 58-24. SMC Timings - NCS Controlled Read and Write