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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv71n19b-cbt

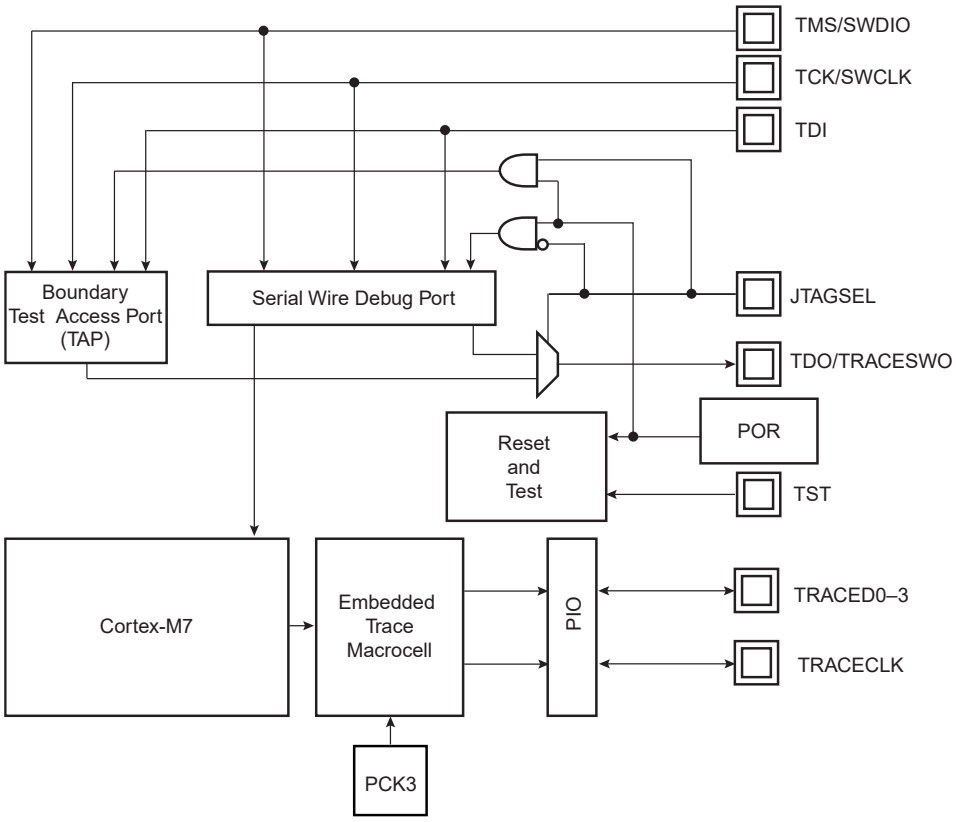
LQFP Pin	VFBGA Ball	TFBGA Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		PIO Peripheral D		Reset State
					Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
73	A10	A10	VDDIO	TEST	JTAGSEL	I	–	–	–	–	–	–	–	–	–	–	I, PD
18, 22, 39, 76	C6, D6, G6	C6, D6, G6	VDDCORE	Power	VDDCORE	I	–	–	–	–	–	–	–	–	–	–	–
86	D7	D7	VDDPLL	Power	VDDPLL	I	–	–	–	–	–	–	–	–	–	–	–
93	E5	E5	VDDUTMII	Power	VDDUTMII	I	–	–	–	–	–	–	–	–	–	–	–
94	A4	A4	VDDUTMII	USBHS	HSDM	I/O	–	–	–	–	–	–	–	–	–	–	–
95	B4	B4	VDDUTMII	USBHS	HSDP	I/O	–	–	–	–	–	–	–	–	–	–	–
3, 7, 8, 10, 29, 67	E7, F4, F5, F6	E7, F4, F5, F6	GND	Ground	GND	I	–	–	–	–	–	–	–	–	–	–	–
	D4	D4	GNDANA	Ground	GNDANA	I	–	–	–	–	–	–	–	–	–	–	–
	A6	A8	GNDUTMI	Ground	GNDUTMI	I	–	–	–	–	–	–	–	–	–	–	–
	C4	C4	GNDPLLUSB	Ground	GNDPLLUSB	I	–	–	–	–	–	–	–	–	–	–	–
	E6	E4	GNDPLL	Ground	GNDPLL	I	–	–	–	–	–	–	–	–	–	–	–
96	B3	B3	VDDUTMIC	Power	VDDUTMIC	I	–	–	–	–	–	–	–	–	–	–	–
97	A3	A3	–	VBG	VBG	I	–	–	–	–	–	–	–	–	–	–	–
90	E4	E6	VDDPLLUSB	Power	VDDPLLUSB	I	–	–	–	–	–	–	–	–	–	–	–

Note:

1. WKUPx can be used if the PIO Controller defines the I/O line as “input”.
2. To select this extra function, refer to the 32.5.14 Parallel Capture Modesection in the Parallel Input/ Output Controller (PIO) chapter.
3. PIODCEN1/PIODCx has priority over WKUPx. Refer to the 32.5.14 Parallel Capture Mode section in the PIO chapter.
4. Refer to the 23.4.2 Slow Clock Generator section in the Supply Controller (SUPC) chapter.
5. To select this extra function, refer to the 33.5.2.1 I/O Lines section in the External Bus Interface (EBI) chapter. This selection is independent of the PIO line configuration. PIO lines must be configured according to required settings (PU or PD).
6. Analog input has priority over WKUPx pin. To select the analog input, refer to the 33.5.2.1 I/O Lines section in the EBI chapter. WKUPx can be used if the PIO controller defines the I/O line as “input”.
7. Analog input has priority over RTCOUTx pin. To select the analog input, refer to the 33.5.2.1 I/O Lines section in the EBI chapter. Refer to the 27.5.8 Waveform Generation section in the Real-Time Clock (RTC) chapter to select RTCOUTx.
8. Analog input has priority over WKUPx pin. To select the analog input, refer to the 33.5.2.1 I/O Lines section in the EBI chapter. To select PIODCEN2, refer to the 32.5.14 Parallel Capture Mode in the PIO chapter.
9. Refer to the System I/O Configuration Register (19.4.7 CCFG_SYSIO) in the Bus Matrix (MATRIX) chapter.
10. Refer to the 30.5.3 Main Crystal Oscillator section in the Clock Generator chapter. This selection is independent of the PIO line configuration. PIO lines must be configured according to XINxx (I) and XOUTxx (O).

16.4 Debug and Test Block Diagram

Figure 16-1. Debug and Test Block Diagram



16.5 Debug and Test Pin Description

Table 16-1. Debug and Test Signal List

Signal Name	Function	Type	Active Level
Reset/Test			
NRST	Microcontroller Reset	Input/Output	Low
TST	Test Select	Input	–
Serial Wire Debug Port/JTAG Boundary Scan			
TCK/SWCLK	Test Clock/Serial Wire Clock	Input	–
TDI	Test Data In	Input	–
TDO/TRACESWO	Test Data Out/Trace Asynchronous Data Out	Output	–
TMS/SWDIO	Test Mode Select/Serial Wire Input/Output	Input	–
JTAGSEL	JTAG Selection	Input	High
Trace Debug Port			

27.6.11 RTC Interrupt Mask Register

Name: RTC_IMR
Offset: 0x28
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			TDERR	CAL	TIM	SEC	ALR	ACK
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit 5 – TDERR Time and/or Date Error Mask

Value	Description
0	The time and/or date error event is disabled.
1	The time and/or date error event is enabled.

Bit 4 – CAL Calendar Event Interrupt Mask

Value	Description
0	The selected calendar event interrupt is disabled.
1	The selected calendar event interrupt is enabled.

Bit 3 – TIM Time Event Interrupt Mask

Value	Description
0	The selected time event interrupt is disabled.
1	The selected time event interrupt is enabled.

Bit 2 – SEC Second Event Interrupt Mask

Value	Description
0	The second periodic interrupt is disabled.
1	The second periodic interrupt is enabled.

Bit 1 – ALR Alarm Interrupt Mask

Value	Description
0	The alarm interrupt is disabled.
1	The alarm interrupt is enabled.

Bit 0 – ACK Acknowledge Update Interrupt Mask

Value	Description
0	The acknowledge for update interrupt is disabled.
1	The acknowledge for update interrupt is enabled.

31.20.31 PMC SleepWalking Disable Register 1

Name: PMC_SLPWK_DR1
Offset: 0x0138
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
		PID62		PID60	PID59	PID58	PID57	PID56
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
			PID53	PID52	PID51	PID50	PID49	PID48
Access								
Reset								
Bit	15	14	13	12	11	10	9	8
	PID47	PID46	PID45	PID44	PID43	PID42	PID41	PID40
Access								
Reset								
Bit	7	6	5	4	3	2	1	0
	PID39		PID37		PID35	PID34	PID33	PID32
Access								
Reset								

Bits 0:3,5,7:28,30 – PID Peripheral Clock x Disable

Value	Description
0	No effect.
1	Disables the corresponding peripheral clock.

32.6.1.21 PIO Pull-Up Disable Register

Name: PIO_PUDR
Offset: 0x0060
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	P31	P30	P29	P28	P27	P26	P25	P24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	P23	P22	P21	P20	P19	P18	P17	P16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	P15	P14	P13	P12	P11	P10	P9	P8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	P7	P6	P5	P4	P3	P2	P1	P0
Access								
Reset								

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – P PIO Pull-Up Disable

Value	Description
0	No effect.
1	Disables the pullup resistor on the I/O line.

Table 34-3. SDRAM Configuration Mapping: 4K Rows, 256/512/1024/2048 Columns

CPU Address Line																										
27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					Bk[1:0]		Row[11:0]												Column[7:0]								M0
				Bk[1:0]			Row[11:0]												Column[8:0]								M0
			Bk[1:0]				Row[11:0]												Column[9:0]								M0
		Bk[1:0]					Row[11:0]												Column[10:0]								M0

Note: M0 is the byte address inside a 16-bit half-word and Bk[1] = BA1, Bk[0] = BA0.

Table 34-4. SDRAM Configuration Mapping: 8K Rows, 256/512/1024/2048 Columns

CPU Address Line																										
27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				Bk[1:0]		Row[12:0]													Column[7:0]								M0
			Bk[1:0]			Row[12:0]													Column[8:0]								M0
		Bk[1:0]				Row[12:0]													Column[9:0]								M0
	Bk[1:0]					Row[12:0]													Column[10:0]								M0

Note: M0 is the byte address inside a 16-bit half-word and Bk[1] = BA1, Bk[0] = BA0.

34.5 Product Dependencies

34.5.1 SDRAM Device Initialization

The initialization sequence is generated by software. The sequence to initialize SDRAM devices is the following:

1. Set the SDRAM features in the SDRAMC_CR: asynchronous timings (TRC, TRAS, etc.), number of columns, number of rows, CAS latency and data bus width. Set UNAL bit in SDRAMC_CFR1.
2. For mobile SDRAM, configure temperature-compensated self-refresh (TCSR), drive strength (DS) and partial array self-refresh (PASR) in the Low Power register (SDRAMC_LPR).
3. Select the SDRAM memory device type in the Memory Device register (SDRAMC_MDR).
4. A pause of at least 200 µs must be observed before a signal toggle.
5. A NOP command is issued to the SDRAM devices. The application must write a 1 to the MODE field in the Mode register (SDRAMC_MR) (see **Note**). Read the SDRAMC_MR and add a memory barrier assembler instruction just after the read. Perform a write access to any SDRAM address.
6. An All Banks Precharge command is issued to the SDRAM. The application must write a 2 to the MODE field in the SDRAMC_MR. Read the SDRAMC_MR and add a memory barrier assembler instruction just after the read. Perform a write access to any SDRAM address.
7. Eight autorefresh (CBR) cycles are provided. The application must set the MODE field to 4 in the SDRAMC_MR. Read the SDRAMC_MR and add a memory barrier assembler instruction just after the read. Perform a write access to any SDRAM location eight times.

Offset	Name	Bit Pos.								
		31:24								
0x0604	XDMAC_CDUS22	7:0	DUBS[7:0]							
		15:8	DUBS[15:8]							
		23:16	DUBS[23:16]							
		31:24								
0x0608 ... 0x060F	Reserved									
0x0610	XDMAC_CIE23	7:0		ROIE	WBIE	RBIE	FIE	DIE	LIE	BIE
		15:8								
		23:16								
		31:24								
0x0614	XDMAC_CID23	7:0		ROID	WBEID	RBEID	FID	DID	LID	BID
		15:8								
		23:16								
		31:24								
0x0618	XDMAC_CIM23	7:0		ROIM	WBEIM	RBEIM	FIM	DIM	LIM	BIM
		15:8								
		23:16								
		31:24								
0x061C	XDMAC_CIS23	7:0		ROIS	WBEIS	RBEIS	FIS	DIS	LIS	BIS
		15:8								
		23:16								
		31:24								
0x0620	XDMAC_CSA23	7:0	SA[7:0]							
		15:8	SA[15:8]							
		23:16	SA[23:16]							
		31:24	SA[31:24]							
0x0624	XDMAC_CDA23	7:0	DA[7:0]							
		15:8	DA[15:8]							
		23:16	DA[23:16]							
		31:24	DA[31:24]							
0x0628	XDMAC_CNDA23	7:0	NDA[5:0]							NDAIF
		15:8	NDA[13:6]							
		23:16	NDA[21:14]							
		31:24	NDA[29:22]							
0x062C	XDMAC_CNDC23	7:0				NDVIEW[1:0]		NDDUP	NDSUP	NDE
		15:8								
		23:16								
		31:24								
0x0630	XDMAC_CUBC23	7:0	UBLEN[7:0]							
		15:8	UBLEN[15:8]							
		23:16	UBLEN[23:16]							
		31:24								
0x0634	XDMAC_CBC23	7:0	BLEN[7:0]							
		15:8					BLEN[11:8]			

Value	Description
0	End of flush condition has not occurred.
1	End of flush condition has occurred since the last read of the Status register.

Bit 2 – DIS End of Disable Interrupt Status Bit

Value	Description
0	End of disable condition has not occurred.
1	End of disable condition has occurred since the last read of the Status register.

Bit 1 – LIS End of Linked List Interrupt Status Bit

Value	Description
0	End of linked list condition has not occurred.
1	End of linked list condition has occurred since the last read of the Status register.

Bit 0 – BIS End of Block Interrupt Status Bit

Value	Description
0	End of block interrupt has not occurred.
1	End of block interrupt has occurred since the last read of the Status register.

This bit is cleared by writing a '1' to it.

Bit	31	30	29	28	27	26	25	24
	WZO	CLTTO	OP[1:0]		PHYA[4:1]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PHYA[0:0]	REGA[4:0]					WTN[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – WZO Write ZERO
Must be written to '0'.

Value	Description
0	Mandatory
1	Reserved

Bit 30 – CLTTO Clause 22 Operation

Value	Description
0	Clause 45 operation
1	Clause 22 operation

Bits 29:28 – OP[1:0] Operation

Value	Description
01	Write
10	Read
Other	Reseved

Bits 27:23 – PHYA[4:0] PHY Address

Bits 22:18 – REGA[4:0] Register Address
Specifies the register in the PHY to access.

Bits 17:16 – WTN[1:0] Write Ten
Must be written to '10'.

Value	Description
10	Mandatory
Other	Reserved

38.8.88 GMAC IEEE 1588 Timer Increment Register

Name: GMAC_TI
Offset: 0x1DC
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	NIT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ACNS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CNS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:16 – NIT[7:0] Number of Increments
The number of increments after which the alternative increment is used.

Bits 15:8 – ACNS[7:0] Alternative Count Nanoseconds
Alternative count of nanoseconds by which the 1588 Timer Nanoseconds Register will be incremented each clock cycle.

Bits 7:0 – CNS[7:0] Count Nanoseconds
A count of nanoseconds by which the IEEE 1588 Timer Nanoseconds Register will be incremented each clock cycle.

39.5.3.4 USB Reset

The USBHS sends a USB bus reset when the user writes a one to the Send USB Reset bit in the Host General Control register (USBHS_HSTCTRL.RESET). The USB Reset Sent Interrupt bit in the Host Global Interrupt Status register (USBHS_HSTISR.RSTI) is set when the USB reset has been sent. In this case, all pipes are disabled and de-allocated.

If the bus was previously in a “Suspend” state (the Start of Frame Generation Enable (USBHS_HSTCTRL.SOFE) bit is zero), the USBHS automatically switches to the “Resume” state, the Host Wakeup Interrupt (USBHS_HSTISR.HWUPI) bit is set and the USBHS_HSTCTRL.SOFE bit is set in order to generate SOFs or micro SOFs immediately after the USB reset.

At the end of the reset, the user should check the USBHS_SR.SPEED field to know the speed running according to the peripheral capability (LS.FS/HS).

39.5.3.5 Pipe Reset

A pipe can be reset at any time by writing a one to the Pipe x Reset (USBHS_HSTPIP.PRSTx) bit. This is recommended before using a pipe upon hardware reset or when a USB bus reset has been sent. This resets:

- the internal state machine of the pipe,
- the receive and transmit bank FIFO counters,
- all the registers of the pipe (USBHS_HSTPIPCFGx, USBHS_HSTPIPISRx, USBHS_HSTPIPIMRx), except its configuration (USBHS_HSTPIPCFGx.ALLOC, USBHS_HSTPIPCFGx.PBK, USBHS_HSTPIPCFGx.PSIZE, USBHS_HSTPIPCFGx.PTOKEN, USBHS_HSTPIPCFGx.PTYPE, USBHS_HSTPIPCFGx.PEPNUM, USBHS_HSTPIPCFGx.INTFRQ) and its Data Toggle Sequence field (USBHS_HSTPIPISRx.DTSEQ).

The pipe configuration remains active and the pipe is still enabled.

The pipe reset may be associated with a clear of the data toggle sequence. This can be achieved by setting the Reset Data Toggle bit in the Pipe x Control register (USBHS_HSTPIPIMRx.RSTDT) (by writing a one to the Reset Data Toggle Set bit in the Pipe x Control Set register (USBHS_HSTPIPIERx.RSTDTS)).

In the end, the user has to write a zero to the USBHS_HSTPIP.PRSTx bit to complete the reset operation and to start using the FIFO.

39.5.3.6 Pipe Activation

The pipe is maintained inactive and reset (see "Pipe Reset" for more details) as long as it is disabled (USBHS_HSTPIP.PENx = 0). The Data Toggle Sequence field (USBHS_HSTPIPISRx.DTSEQ) is also reset.

The algorithm represented in the following figure must be followed to activate a pipe.

39.6.23 Device Endpoint Interrupt Disable Register (Control, Bulk, Interrupt Endpoints)

Name: USBHS_DEVEPTIDRx
Offset: 0x0220 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

This register view is relevant only if EPTYPE = 0x0, 0x2, or 0x3 in "Device Endpoint x Configuration Register".

For additional information, see "Device Endpoint x Mask Register (Control, Bulk, Interrupt Endpoints)".

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Clears the corresponding bit in USBHS_DEVEPTIMRx.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					STALLRQC		NYETDISC	EPDISHDMAC
Access								
Reset					0		0	0

Bit	15	14	13	12	11	10	9	8
		FIFOCONC		NBUSYBKEC				
Access								
Reset		0		0				

Bit	7	6	5	4	3	2	1	0
	SHORTPACKETEC	STALLEDEC	OVERFEC	NAKINEC	NAKOUTEC	RXSTPEC	RXOUTEC	TXINEC
Access								
Reset	0	0	0	0	0	0	0	0

Bit 19 – STALLRQC STALL Request Clear

Bit 17 – NYETDISC NYET Token Disable Clear

Bit 16 – EPDISHDMAC Endpoint Interrupts Disable HDMA Request Clear

Bit 14 – FIFOCONC FIFO Control Clear

Bit 12 – NBUSYBKEC Number of Busy Banks Interrupt Clear

Bit 7 – SHORTPACKETEC Shortpacket Interrupt Clear

Value	Description
0	No boot operation error since the last read of HSMCI_SR
1	Corrupted Boot Acknowledge signal received since the last read of HSMCI_SR.

Bit 28 – ACKRCV Boot Operation Acknowledge Received (cleared on read)

Value	Description
0	No Boot acknowledge received since the last read of the HSMCI_SR.
1	A Boot acknowledge signal has been received since the last read of HSMCI_SR.

Bit 27 – XFRDONE Transfer Done flag

Value	Description
0	A transfer is in progress.
1	Command Register is ready to operate and the data bus is in the idle state.

Bit 26 – FIFOEMPTY FIFO empty flag

Value	Description
0	FIFO contains at least one byte.
1	FIFO is empty.

Bit 24 – BLKOVRE DMA Block Overrun Error (cleared on read)

Value	Description
0	No error.
1	A new block of data is received and the DMA controller has not started to move the current pending block, a block overrun is raised.

Bit 23 – CSTOE Completion Signal Time-out Error (cleared on read)

Value	Description
0	No error.
1	The completion signal time-out set by CSTOCYC and CSTOMUL in HSMCI_CSTOR has been exceeded.

Bit 22 – DTOE Data Time-out Error (cleared on read)

Value	Description
0	No error.
1	The data time-out set by DTOCYC and DTOMUL in HSMCI_DTOR has been exceeded.

Bit 21 – DCRCE Data CRC Error (cleared on read)

Value	Description
0	No error.
1	A CRC16 error has been detected in the last data block.

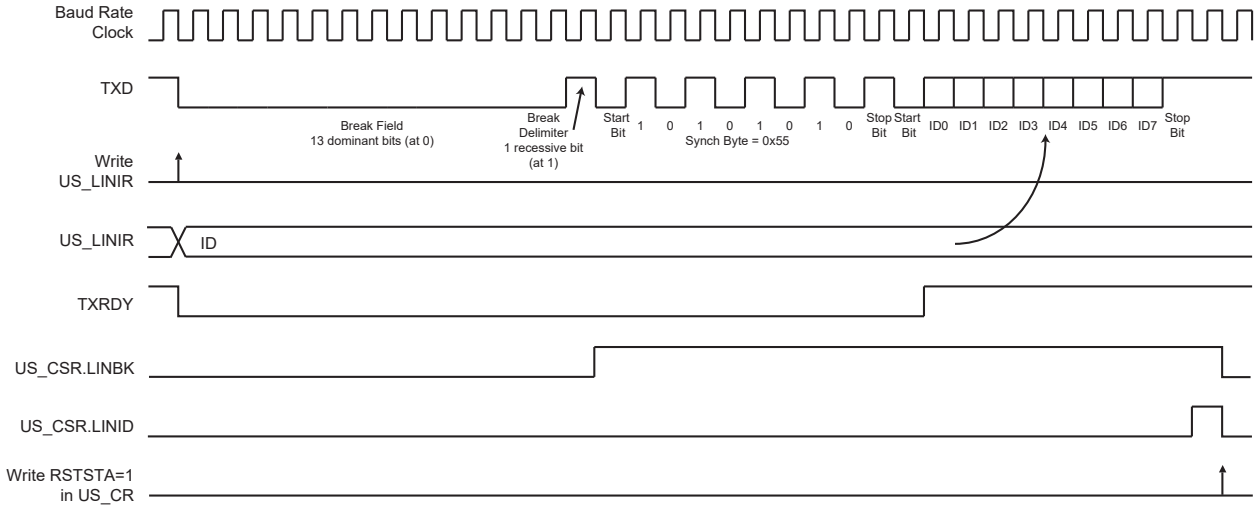
Bit 20 – RTOE Response Time-out Error (cleared by writing in HSMCI_CMDR)

The Break Field consists of 13 dominant bits and 1 recessive bit, the Synch Field is the character 0x55 and the Identifier corresponds to the character written in the LIN Identifier register (US_LINIR). The Identifier parity bits can be automatically computed and sent (see "Identifier Parity").

The flag TXRDY rises when the identifier character is transferred into the Shift register of the transmitter.

As soon as the Synch Break Field is transmitted, US_CSR.LINBK is set to '1'. Likewise, as soon as the Identifier Field is sent, US_CSR.LINID is set to '1'. These flags are reset by writing a '1' to US_CR.RSTSTA.

Figure 46-39. Header Transmission



46.6.9.7 Header Reception (Slave Node Configuration)

All the LIN frames start with a header which is sent by the master node and consists of a Synch Break Field, Synch Field and Identifier Field.

In slave node configuration, the frame handling starts with the reception of the header.

The USART uses a break detection threshold of 11 nominal bit times at the actual baud rate. At any time, if 11 consecutive recessive bits are detected on the bus, the USART detects a Break Field. As long as a Break Field has not been detected, the USART stays idle and the received data are not taken in account.

When a Break Field has been detected, US_CSR.LINBK is set to '1' and the USART expects the Synch Field character to be 0x55. This field is used to update the actual baud rate in order to stay synchronized (see "Slave Node Synchronization"). If the received Synch character is not 0x55, an Inconsistent Synch Field error is generated (see "LIN Errors").

After receiving the Synch Field, the USART expects to receive the Identifier Field.

When the Identifier Field has been received, US_CSR.LINID is set to '1'. At this moment, US_LINIR.IDCHR is updated with the received character. The Identifier parity bits can be automatically computed and checked (see "Identifier Parity").

If the Header is not entirely received within the time given by the maximum length of the header $t_{Header\_Maximum}$, the error flag US_CSR.LINHTE is set to '1'.

The flag bits LINID, LINBK and LINHTE are reset by writing a '1' to US_CR.RSTSTA.

2. Only valid for DMA pointers associated with the MediaLB block (Not valid for HBI block related pointers).

Isochronous Channel Descriptors

The format and field definitions for an isochronous CDT entry are shown in Table 48-16 and Table 48-17, respectively.

Table 48-16. Isochronous CDT Entry Format

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Reserved															
16	Reserved															
32	Reserved							BS[8:0]								
48	Reserved															
64	WSTS[2:0]			WPTR[12:0]												
80	RSTS[2:0]			RPTR[12:0]												
96	Reserved			BD[12:0]												
112	BF	rsvd	BA[13:0]													

Table 48-17. Isochronous CDT Entry Field Definitions

Field	Description	Details	Accessibility
BA	Buffer Base Address	- BA can start at any byte in the 16k DBR	r,w
BD	Buffer Depth	- BD = size of buffer in bytes - 1 - Buffer end address = BA + BD - Isochronous buffers must be large enough to hold at least 3 blocks (packets) of data - Buffer depth must be a integer multiple of blocks	r,w
BF	Buffer Full	- Software initializes to zero, hardware updates - DMA write hardware sets BF when the buffer is full - DMA read hardware clears BF when the buffer is empty - BF is valid only when the buffer is full or empty, otherwise ignore	r,w,u (1)
BS	Block Size	- BS defines when to begin the DMA to the data buffer - BS = buffer block size in bytes - 1 - For Rx channels, the DMA writes start when the number of empty bytes (SPACE) in the data buffer ≥ the block size - For Tx channels, the DMA reads start when the number of valid bytes (VALID) in the data buffer ≥ the block size	r,w,u (1)
RPTR	Read Pointer	- Software initializes to zero, hardware updates	r,w,u (1)

50.7.11 TC Interrupt Enable Register

Name: TC_IERx
Offset: 0x24 + x*0x40 [x=0..2]
Reset: –
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
Access	W	W	W	W	W	W	W	W
Reset	–	–	–	–	–	–	–	–

Bit 7 – ETRGS External Trigger

Bit 6 – LDRBS RB Loading

Bit 5 – LDRAS RA Loading

Bit 4 – CPCS RC Compare

Bit 3 – CPBS RB Compare

Bit 2 – CPAS RA Compare

Bit 1 – LOVRS Load Overrun

Bit 0 – COVFS Counter Overflow

Figure 58-27. USART SPI Slave Mode (Mode 1 or 2)

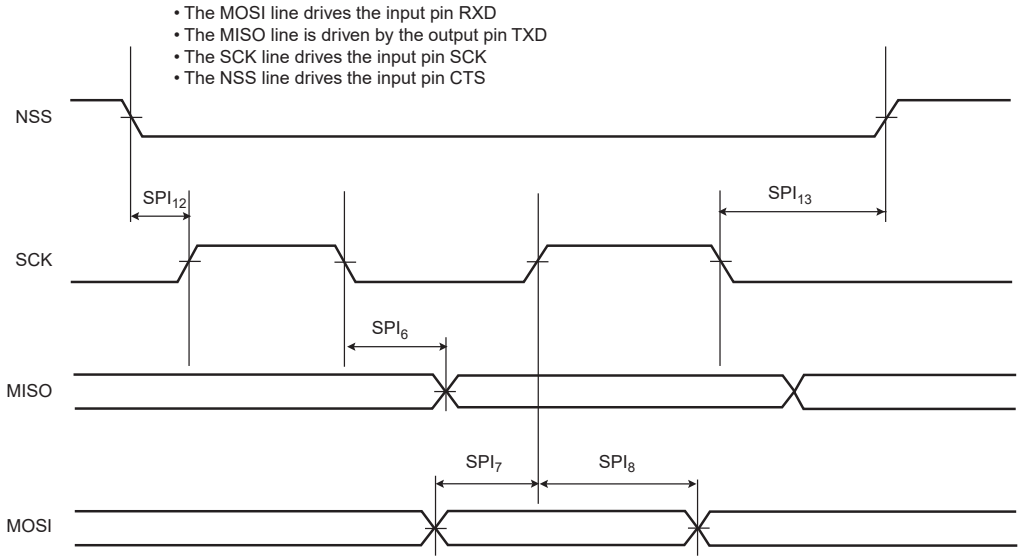
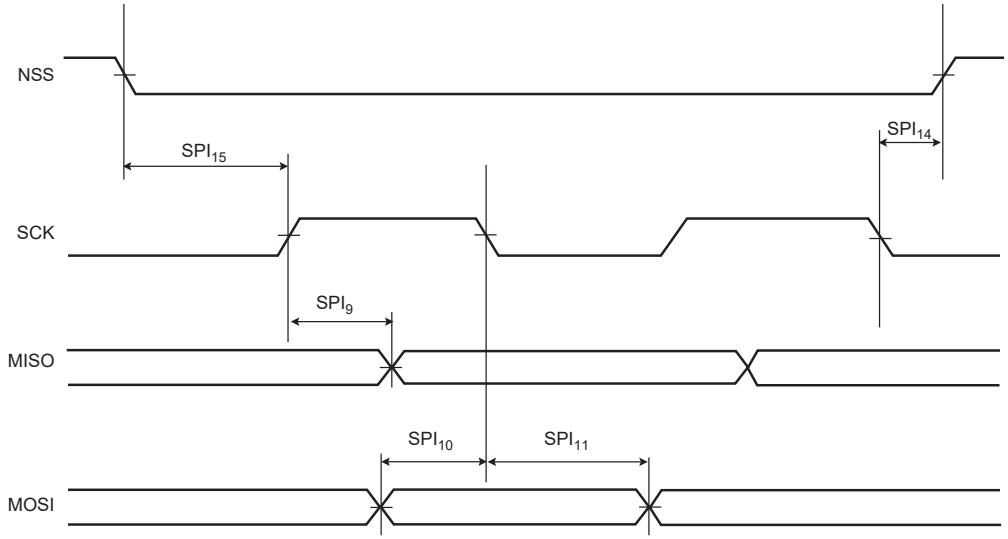


Figure 58-28. USART SPI Slave Mode (Mode 0 or 3)



58.13.1.11.1 USART SPI TImings

Timings are given in the following domains:

- 1.8V domain: VDDIO from 1.7V to 1.95V, maximum external capacitor = 20 pF
- 3.3V domain: VDDIO from 2.85V to 3.6V, maximum external capacitor = 40 pF

Table 58-66. USART SPI Timings

Symbol	Parameter	Conditions	Min	Max	Unit
Master Mode					
SPI_0	SCK Period	1.8V domain 3.3V domain	MCK/6	–	ns
SPI_1	Input Data Setup Time	1.8V domain 3.3V domain	2.8 2.5	–	ns