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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv71n20b-cb

LQFP Pin	LFBGA/ TFBGA Ball	UFBGA Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		PIO Peripheral D		Reset State
					Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
17	F4	G2	VDDIO	GPIO_AD	PC12	I/O	AFE1_AD3[5]	I	NCS3	O	TIOB8	I/O	CANRX1	I	–	–	PIO, I, PU, ST
19	G2	H3	VDDIO	GPIO_AD	PC13	I/O	AFE1_AD1[5]	I	NWAIT	I	PWMC0_PWMH3	O	SDA10	O	–	–	PIO, I, PU, ST
97	E10	F12	VDDIO	GPIO_AD	PC14	I/O	–	–	NCS0	O	TCLK8	I	CANTX1	O	–	–	PIO, I, PU, ST
18	G1	H4	VDDIO	GPIO_AD	PC15	I/O	AFE1_AD2[5]	I	NCS1/SDCS	O	PWMC0_PWML3	O	–	–	–	–	PIO, I, PU, ST
100	D11	E12	VDDIO	GPIO_AD	PC16	I/O	–	–	A21/NANDALE	O	–	–	–	–	–	–	PIO, I, PU, ST
103	B12	E10	VDDIO	GPIO_AD	PC17	I/O	–	–	A22/NANDCLE	O	–	–	–	–	–	–	PIO, I, PU, ST
111	B10	B12	VDDIO	GPIO_AD	PC18	I/O	–	–	A0/NBS0	O	PWMC0_PWML1	O	–	–	–	–	PIO, I, PU, ST
117	D8	B10	VDDIO	GPIO_AD	PC19	I/O	–	–	A1	O	PWMC0_PWMH2	O	–	–	–	–	PIO, I, PU, ST
120	A9	C9	VDDIO	GPIO_AD	PC20	I/O	–	–	A2	O	PWMC0_PWML2	O	–	–	–	–	PIO, I, PU, ST
122	A7	A9	VDDIO	GPIO_AD	PC21	I/O	–	–	A3	O	PWMC0_PWMH3	O	–	–	–	–	PIO, I, PU, ST
124	C7	A8	VDDIO	GPIO_AD	PC22	I/O	–	–	A4	O	PWMC0_PWML3	O	–	–	–	–	PIO, I, PU, ST
127	C6	C7	VDDIO	GPIO_AD	PC23	I/O	–	–	A5	O	TIOA3	I/O	–	–	–	–	PIO, I, PU, ST
130	B6	D7	VDDIO	GPIO_AD	PC24	I/O	–	–	A6	O	TIOB3	I/O	SPI1_SPCK	O	–	–	PIO, I, PU, ST
133	C5	C6	VDDIO	GPIO_AD	PC25	I/O	–	–	A7	O	TCLK3	I	SPI1_NPCS0	I/O	–	–	PIO, I, PU, ST
13	F2	F4	VDDIO	GPIO_AD	PC26	I/O	AFE1_AD7[5]	I	A8	O	TIOA4	I/O	SPI1_MISO	I	–	–	PIO, I, PU, ST
12	E2	F3	VDDIO	GPIO_AD	PC27	I/O	AFE1_AD8[5]	I	A9	O	TIOB4	I/O	SPI1_MOSI	O	–	–	PIO, I, PU, ST
76	L12	L13	VDDIO	GPIO_AD	PC28	I/O	–	–	A10	O	TCLK4	I	SPI1_NPCS1	I/O	–	–	PIO, I, PU, ST
16	F3	G1	VDDIO	GPIO_AD	PC29	I/O	AFE1_AD4[5]	I	A11	O	TIOA5	I/O	SPI1_NPCS2	O	–	–	PIO, I, PU, ST
15	F1	G3	VDDIO	GPIO_AD	PC30	I/O	AFE1_AD5[5]	I	A12	O	TIOB5	I/O	SPI1_NPCS3	O	–	–	PIO, I, PU, ST
14	E1	G4	VDDIO	GPIO_AD	PC31	I/O	AFE1_AD6[5]	I	A13	O	TCLK5	I	–	–	–	–	PIO, I, PU, ST
1	D4	B1	VDDIO	GPIO_AD	PD0	I/O	DAC1[11]	I	GTXCK	I	PWMC1_PWML0	O	SPI1_NPCS1	I/O	DCD0	I	PIO, I, PU, ST
132	B5	B6	VDDIO	GPIO	PD1	I/O	–	–	GTXEN	O	PWMC1_PWMH0	O	SPI1_NPCS2	I/O	DTR0	O	PIO, I, PU, ST
131	A5	A6	VDDIO	GPIO	PD2	I/O	–	–	GTX0	O	PWMC1_PWML1	O	SPI1_NPCS3	I/O	DSR0	I	PIO, I, PU, ST
128	B7	B7	VDDIO	GPIO	PD3	I/O	–	–	GTX1	O	PWMC1_PWMH1	O	UTXD4	O	RI0	I	PIO, I, PU, ST
126	D6	C8	VDDIO	GPIO_CLK	PD4	I/O	–	–	GRXDV	I	PWMC1_PWML2	O	TRACED0	O	DCD2	I	PIO, I, PU, ST
125	D7	B8	VDDIO	GPIO_CLK	PD5	I/O	–	–	GRX0	I	PWMC1_PWMH2	O	TRACED1	O	DTR2	O	PIO, I, PU, ST
121	A8	B9	VDDIO	GPIO_CLK	PD6	I/O	–	–	GRX1	I	PWMC1_PWML3	O	TRACED2	O	DSR2	I	PIO, I, PU, ST
119	B8	A10	VDDIO	GPIO_CLK	PD7	I/O	–	–	GRXER	I	PWMC1_PWMH3	O	TRACED3	O	RI2	I	PIO, I, PU, ST
113	E9	A12	VDDIO	GPIO_CLK	PD8	I/O	–	–	GMDC	O	PWMC0_PWMFI1	I	–	–	TRACECLK	O	PIO, I, PU, ST
110	D9	A13	VDDIO	GPIO_CLK	PD9	I/O	–	–	GMDIO	I/O	PWMC0_PWMFI2	I	AFE1_AD TRG	I	–	–	PIO, I, PU, ST

25.5.3 Reinforced Safety Watchdog Timer Status Register

Name: RSWDT_SR
Offset: 0x08
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								WDUNF
Access								
Reset								0

Bit 0 – WDUNF Watchdog Underflow

Value	Description
0	No watchdog underflow occurred since the last read of RSWDT_SR.
1	At least one watchdog underflow occurred since the last read of RSWDT_SR.

invalidated as soon as the transfer address fails to lie in the selected NCSx address space. For details on these waveforms, refer to 35. Static Memory Controller (SMC).

NAND Flash Signals

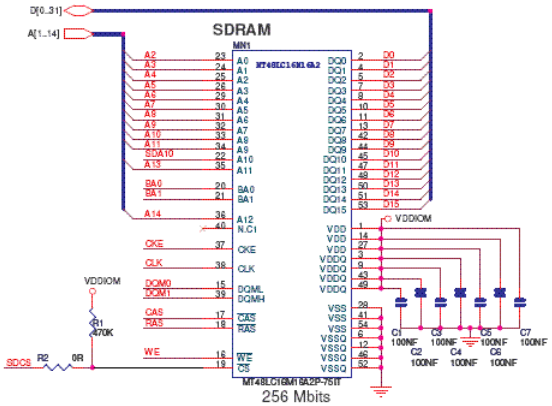
The address latch enable and command latch enable signals on the NAND Flash device are driven by address bits A22 and A21 of the EBI address bus. The command, address or data words on the data bus of the NAND Flash device are distinguished by using their address within the NCSx address space. The chip enable (CE) signal of the device and the ready/busy (R/B) signals are connected to PIO lines. The CE signal then remains asserted even when NCSx is not selected, preventing the device from returning to standby mode.

33.5.4 Implementation Examples

The following hardware configurations are given for illustration only. The user should refer to the memory manufacturer web site to check current device availability.

33.5.4.1 16-bit SDRAM on NCS1

Figure 33-2. Hardware Configuration



Software Configuration

The following configuration has to be performed:

- Enable the SDRAM support by setting the bit SDRAMEN field in the CCFG_SMCNFCS Register in the Bus Matrix.
- Initialize the SDRAM Controller depending on the SDRAM device and system bus frequency.

The Data Bus Width is to be programmed to 16 bits.

The SDRAM initialization sequence is described in 34.5.1 SDRAM Device Initialization.

37.6.2 ISI Configuration 2 Register

Name: ISI_CFG2
Offset: 0x04
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	RGB_CFG[1:0]		YCC_SWAP[1:0]			IM_HSIZE[10:8]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	23	22	21	20	19	18	17	16
	IM_HSIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	COL_SPACE	RGB_SWAP	GRAYSCALE	RGB_MODE	GS_MODE	IM_VSIZE[10:8]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IM_VSIZE[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:30 – RGB_CFG[1:0] RGB Pixel Mapping Configuration
Defines RGB pattern when RGB_MODE is set to 1.

If RGB_MODE is set to RGB 8:8:8, then RGB_CFG = 0 implies RGB color sequence, else it implies BGR color sequence.

Value	Name	Description
0	DEFAULT	Byte 0 R/G(MSB) Byte 1 G(LSB)/B Byte 2 R/G(MSB) Byte 3 G(LSB)/B
1	MODE1	Byte 0 B/G(MSB) Byte 1 G(LSB)/R Byte 2 B/G(MSB) Byte 3 G(LSB)/R
2	MODE2	Byte 0 G(LSB)/R Byte 1 B/G(MSB) Byte 2 G(LSB)/R

37.6.6 ISI Color Space Conversion YCrCb to RGB Set 1 Register

Name: ISI_Y2R_SET1
Offset: 0x14
Reset: 0x00007102
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
		Cboff	Croff	Yoff				C4[8:8]
Access		R/W	R/W	R/W				R/W
Reset		1	1	1				1

Bit	7	6	5	4	3	2	1	0
	C4[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	0

Bit 14 – Cboff Color Space Conversion Blue Chrominance Default Offset

Value	Description
0	No offset.
1	Offset = 16.

Bit 13 – Croff Color Space Conversion Red Chrominance Default Offset

Value	Description
0	No offset.
1	Offset = 16.

Bit 12 – Yoff Color Space Conversion Luminance Default Offset

Value	Description
0	No offset.
1	Offset = 128.

Bits 8:0 – C4[8:0] Color Space Conversion Matrix Coefficient C4
C4 element default step is 1/128, ranges from 0 to 3.9921875.

Bit	31	30	29	28	27	26	25	24
	WZO	CLTTO	OP[1:0]		PHYA[4:1]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PHYA[0:0]	REGA[4:0]					WTN[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	DATA[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	DATA[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 31 – WZO Write ZERO
Must be written to '0'.

Value	Description
0	Mandatory
1	Reserved

Bit 30 – CLTTO Clause 22 Operation

Value	Description
0	Clause 45 operation
1	Clause 22 operation

Bits 29:28 – OP[1:0] Operation

Value	Description
01	Write
10	Read
Other	Reseved

Bits 27:23 – PHYA[4:0] PHY Address

Bits 22:18 – REGA[4:0] Register Address
Specifies the register in the PHY to access.

Bits 17:16 – WTN[1:0] Write Ten
Must be written to '10'.

Value	Description
10	Mandatory
Other	Reserved

39.6.51 Host Pipe x Set Register (Control, Bulk Pipes)

Name: USBHS_HSTPIPIFRx
Offset: 0x0590
Reset: 0
Property: Read/Write

This register view is relevant only if PTYPE = 0x0 or 0x2 in "Host Pipe x Configuration Register".

For additional information, see "Host Pipe x Status Register (Control, Bulk Pipes)".

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Sets the corresponding bit in USBHS_HSTPIPISRx, which may be useful for test or debug purposes.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
				NBUSYBKS				
Access								
Reset				0				

Bit	7	6	5	4	3	2	1	0
	SHORTPACKETIS	RXSTALLDIS	OVERFIS	NAKEDIS	PERRIS	TXSTPIS	TXOUTIS	RXINIS
Access								
Reset	0	0	0	0	0	0	0	0

Bit 12 – NBUSYBKS Number of Busy Banks Set

Bit 7 – SHORTPACKETIS Short Packet Interrupt Set

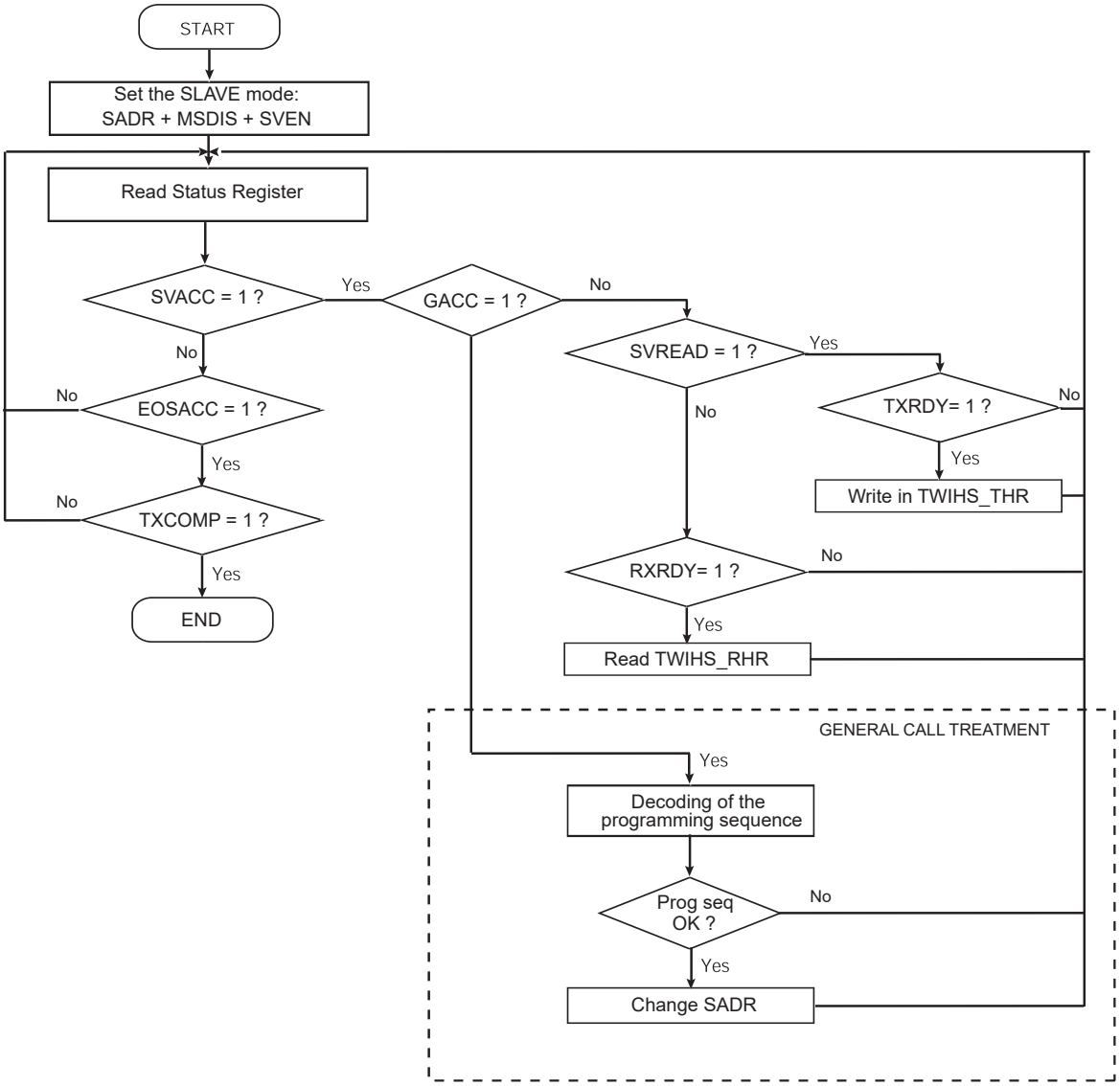
Bit 6 – RXSTALLDIS Received STALLed Interrupt Set

Bit 5 – OVERFIS Overflow Interrupt Set

Bit 4 – NAKEDIS NAKed Interrupt Set

Bit 3 – PERRIS Pipe Error Interrupt Set

Figure 43-43. Read Write Flowchart in Slave Mode



43.7.10 TWIHS Interrupt Disable Register

Name: TWIHS_IDR
Offset: 0x28
Reset: –
Property: Write-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			SMBHHM	SMBDAM	PECERR	TOUT		MCACK
Access			W	W	W	W		W
Reset			–	–	–	–		–

Bit	15	14	13	12	11	10	9	8
					EOSACC	SCL_WS	ARBLST	NACK
Access					W	W	W	W
Reset					–	–	–	–

Bit	7	6	5	4	3	2	1	0
	UNRE	OVRE	GACC	SVACC		TXRDY	RXRDY	TXCOMP
Access	W	W	W	W		W	W	W
Reset	–	–	–	–		–	–	–

Bit 21 – SMBHHM SMBus Host Header Address Match Interrupt Disable

Bit 20 – SMBDAM SMBus Default Address Match Interrupt Disable

Bit 19 – PECERR PEC Error Interrupt Disable

Bit 18 – TOUT Timeout Error Interrupt Disable

Bit 16 – MCACK Master Code Acknowledge Interrupt Disable

Bit 11 – EOSACC End Of Slave Access Interrupt Disable

Bit 10 – SCL_WS Clock Wait State Interrupt Disable

Bit 9 – ARBLST Arbitration Lost Interrupt Disable

Bit 8 – NACK Not Acknowledge Interrupt Disable

Bit 5 – OVRUN Receive Overrun Interrupt Enable

Value	Description
0	No effect.
1	Enables the Receive Overrun Interrupt.

Bit 4 – RXRDY Receive Ready Interrupt Enable

Value	Description
0	No effect.
1	Enables the Receive Ready Interrupt.

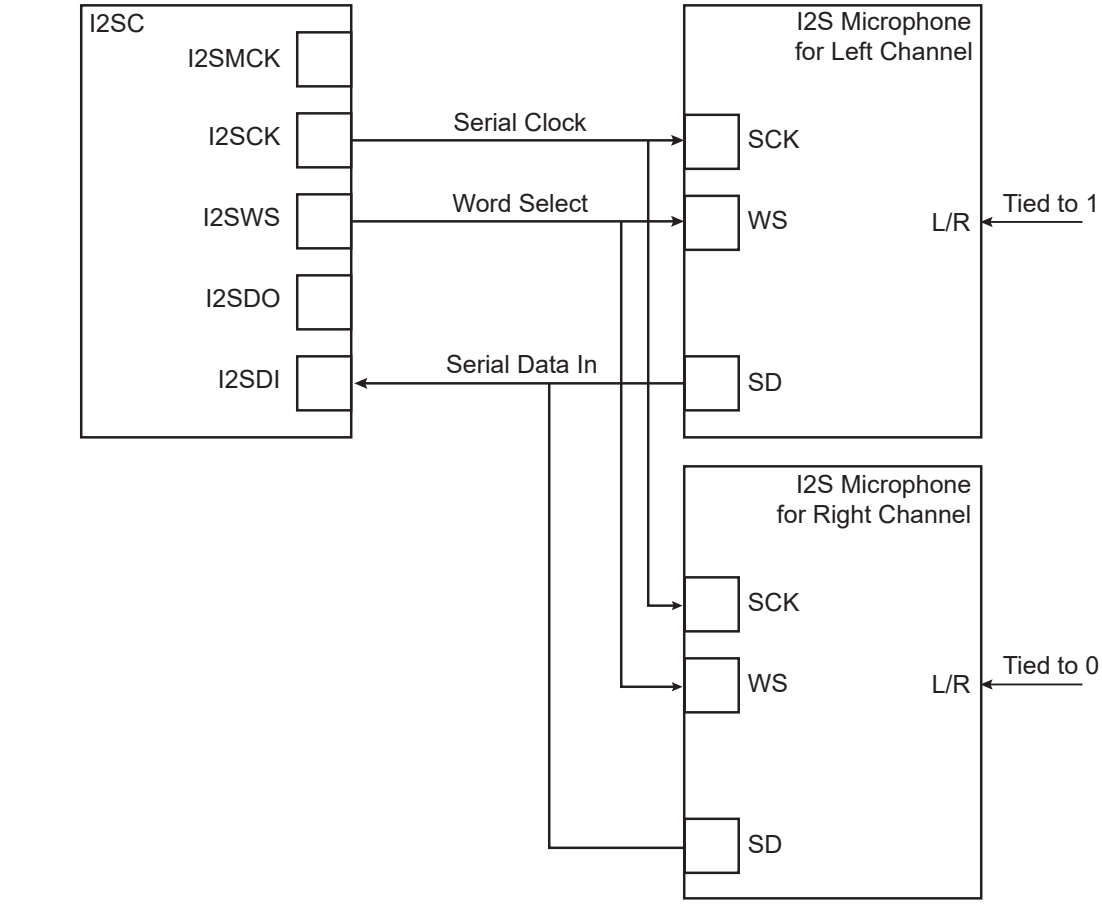
Bit 1 – TXEMPTY Transmit Empty Interrupt Enable

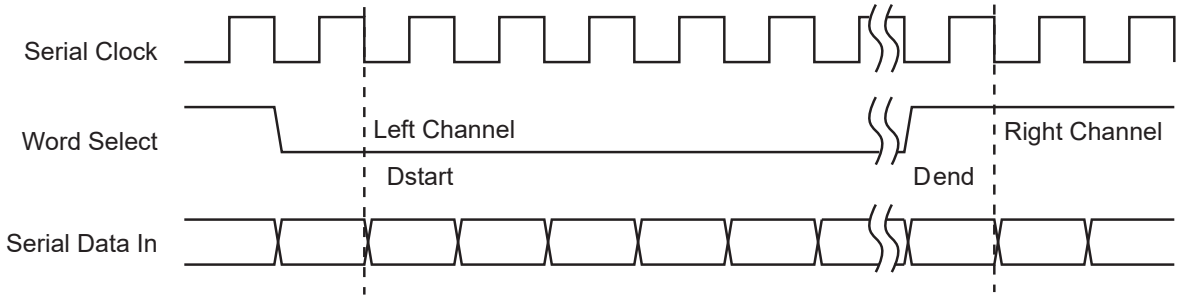
Value	Description
0	No effect.
1	Enables the Transmit Empty Interrupt.

Bit 0 – TXRDY Transmit Ready Interrupt Enable

Value	Description
0	No effect.
1	Enables the Transmit Ready Interrupt.

Figure 45-6. Dual Microphone Application Block Diagram





46.7.46 USART Write Protection Mode Register

Name: US_WPMR
Offset: 0x00E4
Reset: 0x0
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	WPKEY[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	WPKEY[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	WPKEY[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
								WPEN
Access								
Reset								0

Bits 31:8 – WPKEY[23:0] Write Protection Key

Value	Name	Description
0x555341	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

Bit 0 – WPEN Write Protection Enable
See Section 7.12 “Register Write Protection” for the list of registers that can be write-protected.

Value	Description
0	Disables the write protection if WPKEY corresponds to 0x555341 (“USA” in ASCII).
1	Enables the write protection if WPKEY corresponds to 0x555341 (“USA” in ASCII).

(e.g. MediaLB or HBI channel). All entries are indexed according to a fixed physical address assigned to every Rx/Tx channel (as shown in the following table). The value stored in a CAT entry includes a 6-bit Connection Label, which provides a pointer to the CDT. To complete a logical channel and form a routing connection, system software must assign the same Connection Label to both the Rx and Tx channels.

Table 48-11. CAT Entry Map

Peripheral	Tx Channels	Rx Channels	CAT Start Index	CAT End Index	Entries
MediaLB	0 to 64	64 - Tx Channels	0	63	64
HBI	0 to 64	64 - Tx Channels	64	127	64

The format of a full CAT entry is shown in Table 48-12, with field descriptions described in Table 48-13. All reserved bits of a CAT entry field should be written as zero.

Table 48-12. CAT Entry Formats

Channel Type	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Isochronous	rsvd	FCE	rsvd	RNW	CE	CT[2:0] = 3			rsvd		CL[5:0]					
Asynchronous	rsvd		MT	RNW	CE	CT[2:0] = 2			rsvd		CL[5:0]					
Control	rsvd		MT	RNW	CE	CT[2:0] = 1			rsvd		CL[5:0]					
Synchronous	rsvd	MFE	MT	RNW	CE	CT[2:0] = 0			rsvd		CL[5:0]					

Table 48-13. CAT Field Definitions

Field	Description
CL[5:0]	Connection Label (offset into CDT)
CT[2:0]	Channel Type (Others): 111 = Reserved 110 = Reserved 101 = Reserved 100 = Reserved 011 = Isochronous 010 = Asynchronous 001 = Control 000 = Synchronous
CE	Channel Enable: 1 = Enabled 0 = Disabled
RNW	Read Not Write: 1 = Read 0 = Write
MT	Mute Enable (1): 1 = Enabled 0 = Disabled

49.6.41 MCAN Transmit Buffer Transmission Occurred

Name: MCAN_TXBTO
Offset: 0xD8
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	TO31	TO30	TO29	TO28	TO27	TO26	TO25	TO24
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	TO23	TO22	TO21	TO20	TO19	TO18	TO17	TO16
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TO15	TO14	TO13	TO12	TO11	TO10	TO9	TO8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	TO7	TO6	TO5	TO4	TO3	TO2	TO1	TO0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – TOx Transmission Occurred for Buffer x
Each Transmit Buffer has its own Transmission Occurred bit. The bits are set when the corresponding MCAN_TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a ‘1’ to the corresponding bit of register MCAN_TXBAR.

Value	Description
0	No transmission occurred.
1	Transmission occurred.

49.6.45 MCAN Transmit Event FIFO Configuration

Name: MCAN_TXEFC
Offset: 0xF0
Reset: 0x00000000
Property: Read/Write

This register can only be written if the bits CCE and INIT are set in MCAN CC Control Register.

Bit	31	30	29	28	27	26	25	24
			EFWM[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
			EFS[5:0]					
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	EFSA[13:6]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	EFSA[5:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bits 29:24 – EFWM[5:0] Event FIFO Watermark

Value	Description
0	Watermark interrupt disabled.
1-32	Level for Tx Event FIFO watermark interrupt (MCAN_IR.TEFW).
>32	Watermark interrupt disabled.

Bits 21:16 – EFS[5:0] Event FIFO Size
The Tx Event FIFO elements are indexed from 0 to EFS - 1.

Value	Description
0	Tx Event FIFO disabled.
1-32	Number of Tx Event FIFO elements.
>32	Values greater than 32 are interpreted as 32.

Bits 15:2 – EFSA[13:0] Event FIFO Start Address
Start address of Tx Event FIFO in Message RAM (32-bit word address, see Message RAM Configuration).

Write EFSA with the bits [15:2] of the 32-bit address.

Offset	Name	Bit Pos.								
0x0248	PWM_CDTYUPD2	7:0	CDTYUPD[7:0]							
		15:8	CDTYUPD[15:8]							
		23:16	CDTYUPD[23:16]							
		31:24								
0x024C	PWM_CPRD2	7:0	CPRD[7:0]							
		15:8	CPRD[15:8]							
		23:16	CPRD[23:16]							
		31:24								
0x0250	PWM_CPRDUPD2	7:0	CPRDUPD[7:0]							
		15:8	CPRDUPD[15:8]							
		23:16	CPRDUPD[23:16]							
		31:24								
0x0254	PWM_CCNT2	7:0	CNT[7:0]							
		15:8	CNT[15:8]							
		23:16	CNT[23:16]							
		31:24								
0x0258	PWM_DT2	7:0	DTH[7:0]							
		15:8	DTH[15:8]							
		23:16	DTL[7:0]							
		31:24	DTL[15:8]							
0x025C	PWM_DTUPD2	7:0	DTHUPD[7:0]							
		15:8	DTHUPD[15:8]							
		23:16	DTLUPD[7:0]							
		31:24	DTLUPD[15:8]							
0x0260	PWM_CMR3	7:0					CPRE[3:0]			
		15:8			TCTS	DPOLI	UPDS	CES	CPOL	CALG
		23:16					PPM	DTLI	DTHI	DTE
		31:24								
0x0264	PWM_CDTY3	7:0	CDTY[7:0]							
		15:8	CDTY[15:8]							
		23:16	CDTY[23:16]							
		31:24								
0x0268	PWM_CDTYUPD3	7:0	CDTYUPD[7:0]							
		15:8	CDTYUPD[15:8]							
		23:16	CDTYUPD[23:16]							
		31:24								
0x026C	PWM_CPRD3	7:0	CPRD[7:0]							
		15:8	CPRD[15:8]							
		23:16	CPRD[23:16]							
		31:24								
0x0270	PWM_CPRDUPD3	7:0	CPRDUPD[7:0]							
		15:8	CPRDUPD[15:8]							
		23:16	CPRDUPD[23:16]							
		31:24								
0x0274	PWM_CCNT3	7:0	CNT[7:0]							
		15:8	CNT[15:8]							

53.6.4.4 Bypass Mode

Bypass mode disables the DAC output buffer and thus minimizes power consumption. This mode can be used to generate slow varying signals. Refer to the DAC Characteristics in the section “Electrical Characteristics” of this datasheet.

To enter this mode, Free-running mode must be selected and the DACC_ACR.IBCTLCHx field configured in Bypass mode.

Related Links

58. Electrical Characteristics for SAM V70/V71

53.6.4.5 Interpolation Mode

The DACC integrates interpolation filters that allow OSR of 2×, 4×, 8×, 16× or 32×. This mode can be used only if Trigger mode is enabled and value in the field OSRx is not ‘0’. The OSR of the interpolator is configured in the OSRx field in the DACC Trigger Register (DACC_TRIGR).

The data is sampled once every OSR trigger event and then recomputed at the trigger sample rate using a third-order SINC filter. This reduces the number of accesses to the DACC and increases the signal-to-noise ratio (SNR) of the converted output signal.

The figures below show the spectral mask of the SINC filter depending on the selected OSR. f_s is the sampling frequency of the input signal which corresponds to the trigger frequency divided by OSR.

Figure 53-5. Interpolator Spectral Mask for OSR = 2

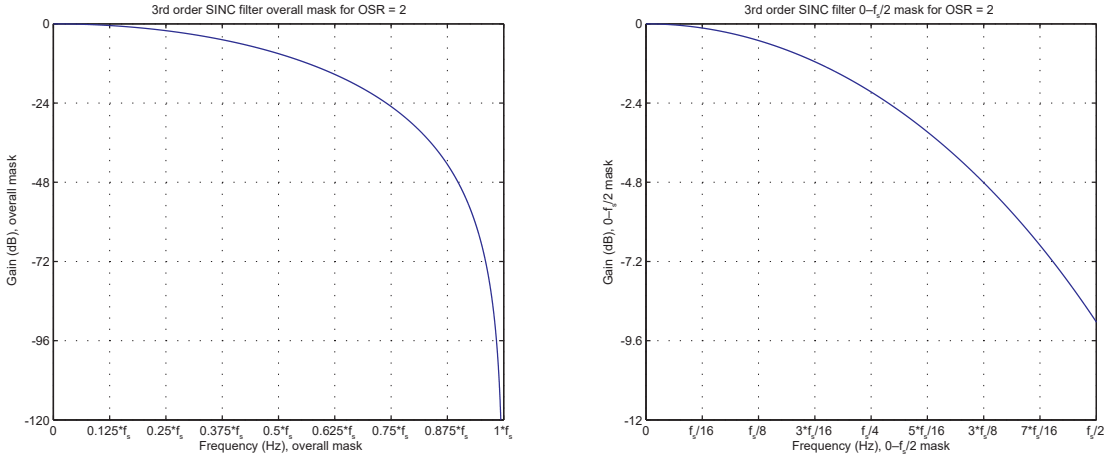
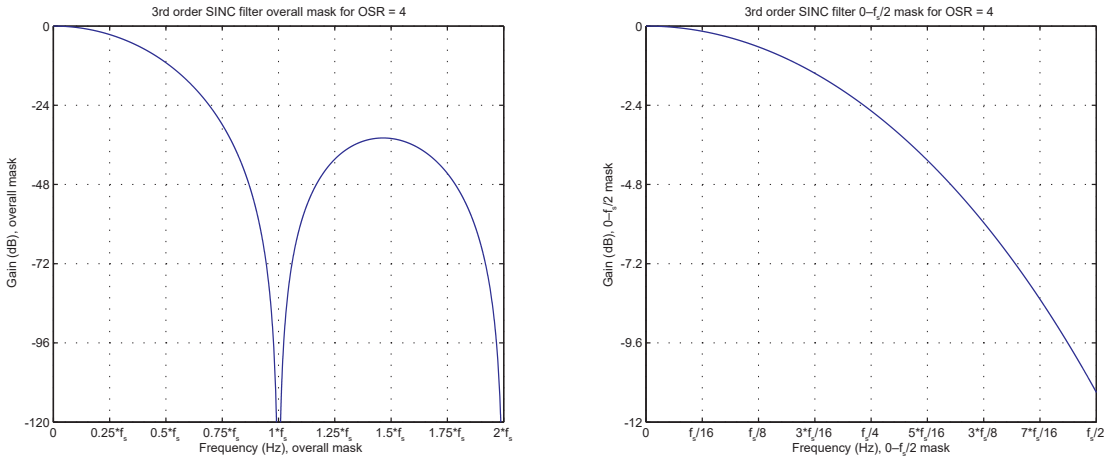


Figure 53-6. Interpolator Spectral Mask for OSR = 4



58.4.5 XIN32 Clock Characteristics in Bypass Mode

Table 58-22. XIN32 Clock Characteristics in Bypass Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$1/(t_{CPXIN})$	XIN32 Clock Frequency	(see **Note**)	–	–	32	kHz
t_{CHXIN}	XIN32 Clock High Half-period	(see **Note**)	15	–	–	ns
t_{CLXIN}	XIN32 Clock Low Half-period	(see **Note**)	15	–	–	ns
V_{XIN_IL}	V_{XIN} Input Low-level Voltage	(see **Note**)	Min of V_{IL} for CLOCK pad	–	Max of V_{IL} for CLOCK pad	V
V_{XIN_IH}	V_{XIN} Input High-level Voltage	(see **Note**)	Min of V_{IH} for CLOCK pad	–	Max of V_{IH} for CLOCK pad	V

Note:

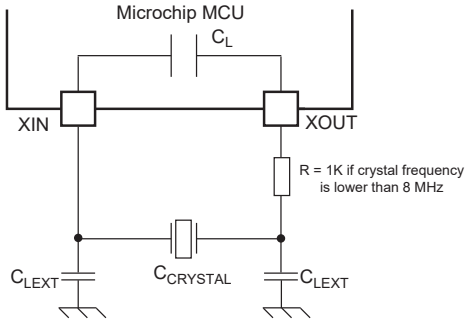
1. These characteristics apply only when the 32.768 kHz crystal oscillator is in Bypass mode.

58.4.6 3 to 20 MHz Crystal Oscillator Characteristics

Table 58-23. 3 to 20 MHz Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Operating Frequency	Normal mode with crystal	3	–	20	MHz
t_{START}	Startup Time	3 MHz, C_{SHUNT} = 3 pF	–	–	40	ms
		12 MHz, C_{SHUNT} = 7 pF with C_M = 1.6 fF	–	–	6	ms
		20 MHz, C_{SHUNT} = 7 pF with C_M = 1.6 fF	–	–	5.7	ms
I_{DDON}	Current Consumption (on VDDIO)	3 MHz	–	230	–	µA
		12 MHz	–	390	–	µA
		20 MHz	–	450	–	µA
C_L	Internal Equivalent Load Capacitance	Integrated Load Capacitance	7.5	9	10.5	pF
		(X_{IN} and X_{OUT} in series)				

Figure 58-10. 3 to 20 MHz Crystal Oscillator Schematics



$C_{LEXT} = 2 \times (C_{CRYSTAL} - C_L - C_{PCB})$

Figure 58-38. SSC Receiver, RK in Input and RF in Output

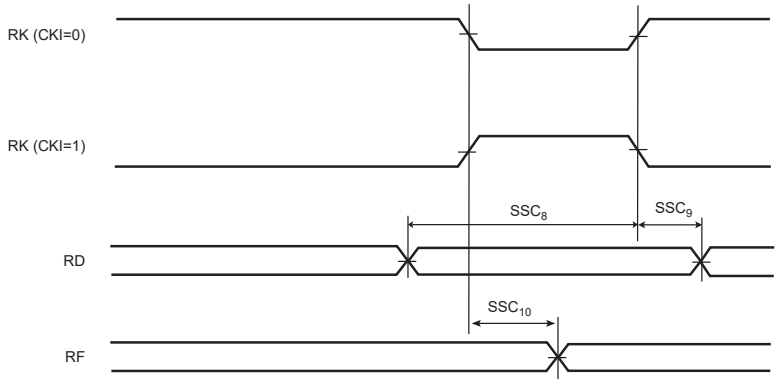


Figure 58-39. SSC Receiver, RK and RF in Output

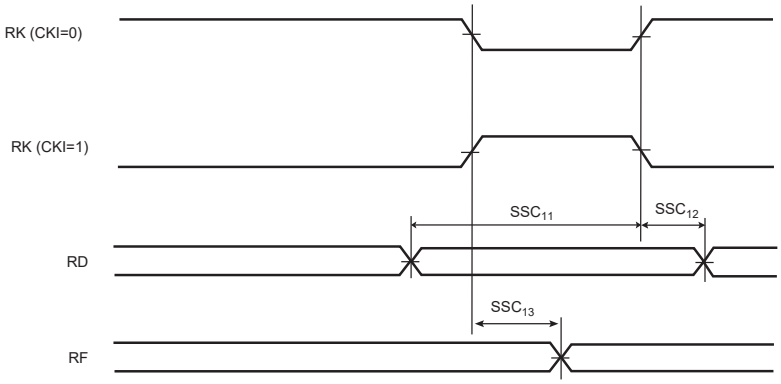


Figure 58-40. SSC Receiver, RK in Output and RF in Input

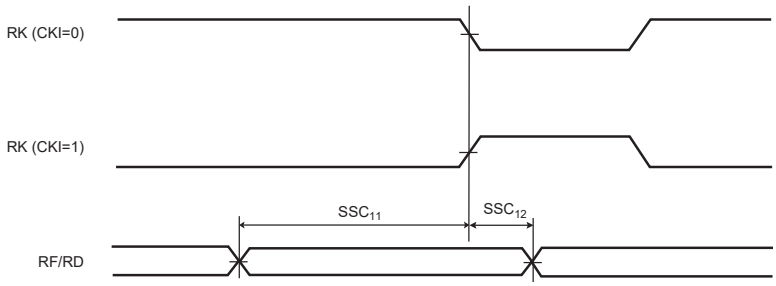


Table 58-74. SSC Timings with 3.3V Peripheral Supply

Symbol	Parameter	Condition	Min	Max	Unit
Transmitter					
SSC_0	TK edge to TF/TD (TK output, TF output)	–	-3.9(1)	4.0 (1)	ns
SSC_1	TK edge to TF/TD (TK input, TF output)	–	3.1(1)	12.7(1)	ns
SSC_2	TF setup time before TK edge (TK output)	–	13.6	–	ns
SSC_3	TF hold time after TK edge (TK output)	–	0	–	ns

Note:

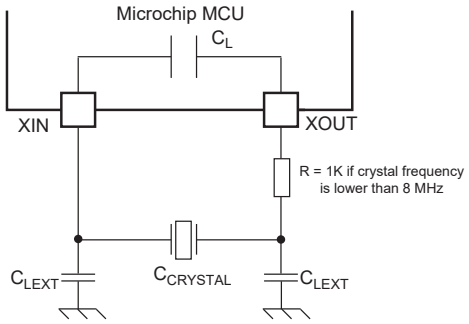
1. These characteristics apply only when the 32.768 kHz crystal oscillator is in Bypass mode.

59.4.6 3 to 20 MHz Crystal Oscillator Characteristics

Table 59-23. 3 to 20 MHz Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Operating Frequency	Normal mode with crystal	3	–	20	MHz
t_{START}	Startup Time	3 MHz, C_{SHUNT} = 3 pF	–	–	40	ms
		12 MHz, C_{SHUNT} = 7 pF with C_M = 1.6 fF	–	–	6	ms
		20 MHz, C_{SHUNT} = 7 pF with C_M = 1.6 fF	–	–	5.7	ms
I_{DDON}	Current Consumption (on VDDIO)	3 MHz	–	230	–	µA
		12 MHz	–	390	–	µA
		20 MHz	–	450	–	µA
C_L	Internal Equivalent Load Capacitance	Integrated Load Capacitance (X_{IN} and X_{OUT} in series)	7.5	9	10.5	pF

Figure 59-10. 3 to 20 MHz Crystal Oscillator Schematics



$C_{LEXT} = 2 \times (C_{CRYSTAL} - C_L - C_{PCB})$

where, C_{PCB} is the capacitance of the printed circuit board (PCB) track layout from the crystal to the pin.

59.4.7 3 to 20 MHz Crystal Characteristics

Table 59-24. 3 to 20 MHz Crystal Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistor	Fundamental at 3 MHz	–	–	150	Ohm
		Fundamental at 8 MHz			140	
		Fundamental at 12 MHz			120	
		Fundamental at 16 MHz			80	
		Fundamental at 20 MHz			50	
C_M	Motional capacitance	Fundamental at 3 MHz	3	–	8	fF
		Fundamental at 8–20 MHz	1.6	–	8	