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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	75
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv71n20b-cbt

Bits 7:0 – DIVA[7:0] PLLA Front End Divider

Value	Name	Description
0	0	PLLA is disabled.
1	BYPASS	Divider is bypassed (divide by 1) and PLLA is enabled.
2–255	Divider output is the selected clock divided by DIVA.	

31.20.34 PMC SleepWalking Activity Status Register 0

Name: PMC_SLPWK_ASR0
Offset: 0x0120
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	PID31	PID30	PID29	PID28	PID27	PID26	PID25	PID24
Access								
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	PID23	PID22	PID21	PID20	PID19	PID18	PID17	PID16
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PID7							
Access								
Reset	0							

Bits 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – PIDx
Peripheral x Activity Status
Only the following PIDs can be configured with asynchronous partial wake-up: UARTx and TWIHSx.
All other PIDs are always read at ‘0’.

Value	Description
0	The peripheral x is not currently active. The asynchronous partial wake-up (SleepWalking) function can be activated.
1	The peripheral x is currently active. The asynchronous partial wake-up (SleepWalking) function must not be activated. **Note:** “PIDx” refers to identifiers as defined in the section “Peripheral Identifiers”.

Signals: EBI_	Power supply	Pins of the Interfaced Device	
		SDR/LPSDR	NAND Flash
Controller		SDRAMC	NFC
A2–A10	VDDIO	A[0:8]	–
A11	VDDIO	A9	–
SDA10	VDDIO	A10	–
A12	VDDIO	–	–
A13–A14	VDDIO	A[11:12]	–
A15	VDDIO	A13	–
A16/BA0	VDDIO	BA0	–
A17/BA1	VDDIO	BA1	–
A18	VDDIO	–	–
A19	VDDIO	–	–
A20	VDDIO	–	–
A21/NANDALE	VDDIO	–	ALE
A22/NANDCLE	VDDIO	–	CLE
A23	VDDIO	–	–
NCS0	VDDIO	–	–
NCS1/SDCS	VDDIO	SDCS	–
NCS2	VDDIO	–	–
NCS3/NANDCS	VDDIO	–	CE
NANDOE	VDDIO	–	OE
NANDWE	VDDIO	–	WE
NRD	VDDIO	–	–
NWR0/NWE	VDDIO	–	–
NWR1/NBS1	VDDIO	DQM1	–
SDCK	VDDIO	CK	–
SDCKE	VDDIO	CKE	–
RAS	VDDIO	RAS	–
CAS	VDDIO	CAS	–
SDWE	VDDIO	WE	–
Pxx	VDDIO	–	CE
Pxx	VDDIO	–	RDY

Bit 22 – PDRQFR PDelay Request Frame Received

Bit 21 – SFT PTP Sync Frame Transmitted

Bit 20 – DRQFT PTP Delay Request Frame Transmitted

Bit 19 – SFR PTP Sync Frame Received

Bit 18 – DRQFR PTP Delay Request Frame Received

Bit 15 – EXINT External Interrupt

Bit 14 – PFTR Pause Frame Transmitted

Bit 13 – PTZ Pause Time Zero

Bit 12 – PFNZ Pause Frame with Non-zero Pause Quantum Received

Bit 11 – HRESP HRESP Not OK

Bit 10 – ROVR Receive Overrun

Bit 7 – TCOMP Transmit Complete

Bit 6 – TFC Transmit Frame Corruption Due to AHB Error

Bit 5 – RLEX Retry Limit Exceeded or Late Collision

Bit 4 – TUR Transmit Underrun

Bit 3 – TXUBR TX Used Bit Read

Bit 2 – RXUBR RX Used Bit Read

Bit 1 – RCOMP Receive Complete

Bit 0 – MFS Management Frame Sent

38.8.48 GMAC 512 to 1023 Byte Frames Transmitted Register

Name: GMAC_TBFT1023
Offset: 0x128
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
	NFTX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFTX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFTX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFTX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFTX[31:0] 512 to 1023 Byte Frames Transmitted without Error
This register counts the number of 512 to 1023 byte frames successfully transmitted without error, i.e., no underrun and not too many retries.

38.8.64 GMAC 64 Byte Frames Received Register

Name: GMAC_BFR64
Offset: 0x168
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
	NFRX[31:24]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	NFRX[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NFRX[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NFRX[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – NFRX[31:0] 64 Byte Frames Received without Error
This bit field counts the number of 64 byte frames successfully received without error. Excludes pause frames, and is only incremented if the frame is successfully filtered and copied to memory.

38.8.90 GMAC PTP Event Frame Transmitted Nanoseconds Register

Name: GMAC_EFTN
Offset: 0x1E4
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
			RUD[29:24]					
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	RUD[23:16]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	RUD[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RUD[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 29:0 – RUD[29:0] Register Update
The register is updated with the value that the IEEE 1588 Timer Nanoseconds Register holds when the SFD of a PTP transmit primary event crosses the MII interface. An interrupt is issued when the bit field is updated.

1: Set when the current bank is ready to accept a new IN packet. This triggers a PEP_x interrupt if TXINE = 1.

For IN endpoints:

0: Cleared when TXINIC = 1. This acknowledges the interrupt, which has no effect on the endpoint FIFO. USBHS_DEVEPTISRx.TXINI shall always be cleared before clearing USBHS_DEVEPTIMRx.FIFOCON.

1: Set at the same time as USBHS_DEVEPTIMRx.FIFOCON when the current bank is free. This triggers a PEP_x interrupt if TXINE = 1.

The user writes into the FIFO and clears the USBHS_DEVEPTIMRx.FIFOCON bit to allow the USBHS to send the data. If the IN endpoint is composed of multiple banks, this also switches to the next bank. The USBHS_DEVEPTISRx.TXINI and USBHS_DEVEPTIMRx.FIFOCON bits are set/cleared in accordance with the status of the next bank.

This bit is inactive (cleared) for OUT endpoints.

Value	Description
0	Disables the ping protocol.
1	Enables the ping mechanism according to the USB 2.0 Standard.

Bits 19:16 – PEPNUM[3:0] Pipe Endpoint Number
This field contains the number of the endpoint targeted by the pipe. This value is from 0 to 10.

This field is cleared upon sending a USB reset.

Bits 13:12 – PTYPE[1:0] Pipe Type
This field contains the pipe type.

This field is cleared upon sending a USB reset.

Value	Name	Description
0	CTRL	Control
1	Reserved	
2	BLK	Bulk
3	Reserved	

Bit 10 – AUTOSW Automatic Switch
This bit is cleared upon sending a USB reset.

Value	Description
0	The automatic bank switching is disabled.
1	The automatic bank switching is enabled.

Bits 9:8 – PTOKEN[1:0] Pipe Token
This field contains the pipe token.

Value	Name	Description
0	SETUP	SETUP
1	IN	IN
2	OUT	OUT
3	Reserved	

Bits 6:4 – PSIZE[2:0] Pipe Size
This field contains the size of each pipe bank.

This field is cleared upon sending a USB reset.

Value	Name	Description
0	8_BYTE	8 bytes
1	16_BYTE	16 bytes
2	32_BYTE	32 bytes
3	64_BYTE	64 bytes
4	128_BYTE	128 bytes
5	256_BYTE	256 bytes
6	512_BYTE	512 bytes
7	1024_BYTE	1024 bytes

Value	Description
0	No channel register is loaded after the end of the channel transfer.
1	The channel controller loads the next descriptor after the end of the current transfer, i.e., when the USBHS_HSTDMASTATUS.CHANN_ENB bit is reset.

Bit 0 – CHANN_ENB Channel Enable Command
If the LDNXT_DSC bit has been cleared by descriptor loading, the firmware has to set the corresponding CHANN_ENB bit to start the described transfer, if needed.

If the LDNXT_DSC bit is cleared, the channel is frozen and the channel registers may then be read and/or written reliably as soon as both the USBHS_HSTDMASTATUS.CHANN_ENB and the CHANN_ACT flags read as 0.

If a channel request is currently serviced when this bit is cleared, the DMA FIFO buffer is drained until it is empty, then the USBHS_HSTDMASTATUS.CHANN_ENB bit is cleared.

If the LDNXT_DSC bit is set or after it has been cleared, the currently loaded descriptor is skipped (no data transfer occurs) and the next descriptor is immediately loaded.

Value	Description
0	The DMA channel is disabled and no transfer occurs upon request. This bit is also cleared by hardware when the channel source bus is disabled at the end of the buffer.
1	The USBHS_HSTDMASTATUS.CHANN_ENB bit is set, enabling DMA channel data transfer. Then, any pending request starts the transfer. This may be used to start or resume any requested transfer.

- To read in the serial memory, but not a memory data, for example a JEDEC-ID or the QSPI_SR, QSPI_IFR.TFRTYP must be written to ‘0’.
- To read in the serial memory, and particularly a memory data, TFRTYP must be written to ‘1’.
- To write in the serial memory, but not a memory data, for example writing the configuration or the QSPI_SR, TFRTYP must be written to ‘2’.
- If the user wants to write in the serial memory in particular to program a memory data, TFRTYP must be written to ‘3’ .

If QSPI_IFR.TFRTYP has a value other than ‘1’, the address sent in the instruction frame is the address of the first system bus accesses. The addresses of the next accesses are not used by the QSPI. At each system bus access, an SPI transfer is performed with the same size. For example, a halfword system bus access leads to a 16-bit SPI transfer, and a byte system bus access leads to an 8-bit SPI transfer.

If TFRTYP = 1, the address of the first instruction frame is the one of the first read access in the QSPI memory space. Each time the read accesses become nonsequential (addresses are not consecutive), a new instruction frame is sent with the last system bus access address. In this way, the system can read data at a random location in the serial memory. The size of the SPI transfers may differ from the size of the system bus read accesses.

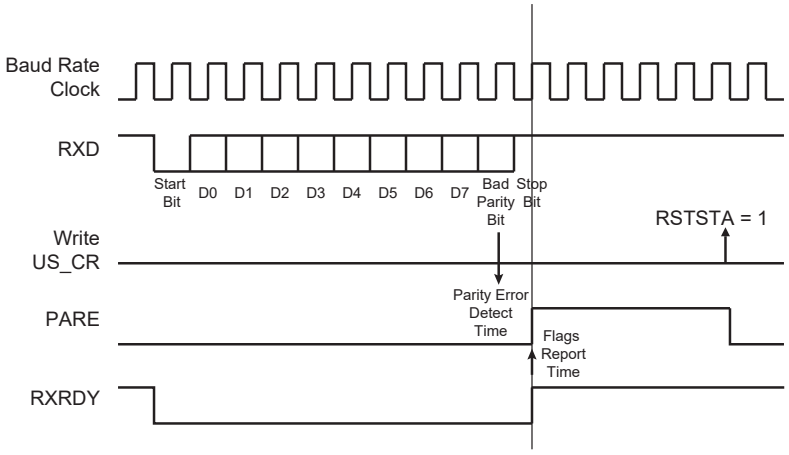
When data transfer is not enabled, the end of the instruction frame is indicated when QSPI_SR.INSTRE rises. (The QSPI_SR.CSR flag indicates when chip select rises. A delay between these flags may exist in case of high clock division or a high DLYBCT value).

When data transfer is enabled, the user must indicate when the data transfer is completed in the QSPI memory space by setting QSPI_CR.LASTXFR. The end of the instruction frame is indicated when QSPI_SR.INSTRE rises.

The following figure illustrates instruction transmission management.

When the receiver detects a parity error, it sets US_CSR.PARE (Parity Error). PARE can be cleared by writing a ‘1’ to the RSTSTA bit the US_CR. The following figure illustrates the parity bit status setting and clearing.

Figure 46-21. Parity Error



46.6.3.9 Multidrop Mode

If the value 0x6 or 0x07 is written to US_MR.PAR, the USART runs in Multidrop mode. This mode differentiates the data characters and the address characters. Data is transmitted with the parity bit at 0 and addresses are transmitted with the parity bit at 1.

If the USART is configured in Multidrop mode, the receiver sets PARE when the parity bit is high and the transmitter is able to send a character with the parity bit high when a ‘1’ is written to US_CR.SENTA.

To handle parity error, PARE is cleared when a ‘1’ is written to US_CR.RSTSTA.

The transmitter sends an address byte (parity bit set) when US_CR.SENDA = 1. In this case, the next byte written to US_THR is transmitted as an address. Any character written in the US_THR without having written SENDA is transmitted normally with the parity at 0.

46.6.3.10 Transmitter Timeguard

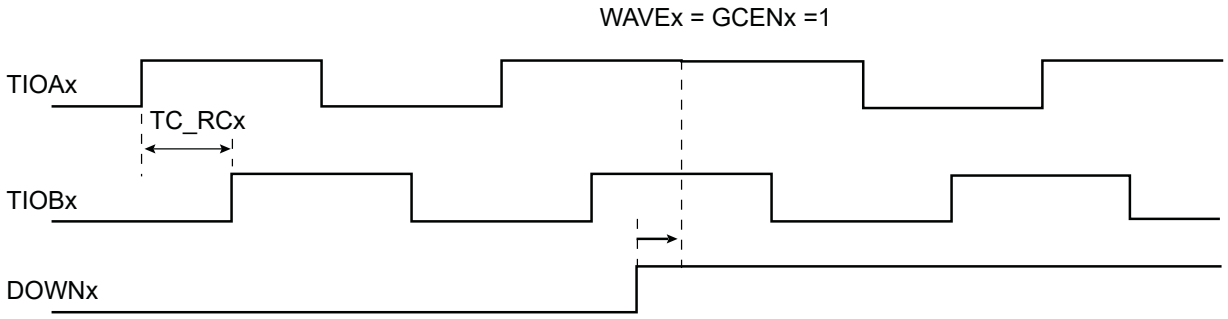
The timeguard feature enables the USART interface with slow remote devices.

The timeguard function enables the transmitter to insert an idle state on the TXD line between two characters. This idle state acts as a long stop bit.

The duration of the idle state is programmed in the TG field of the Transmitter Timeguard register (US_TTGR). When this field is written to ‘0’, no timeguard is generated. Otherwise, the transmitter holds a high level on TXD after each transmitted byte during the number of bit periods programmed in TG in addition to the number of stop bits.

As illustrated in the following figure, the behavior of TXRDY and TXEMPTY status bits is modified by the programming of a timeguard. TXRDY rises only when the start bit of the next character is sent, and thus remains at 0 during the timeguard transmission if a character has been written in US_THR. TXEMPTY remains low until the timeguard transmission is completed as the timeguard is part of the current character being transmitted.

Figure 50-23. 2-bit Gray Up/Down Counter



50.6.18 Fault Mode

At any time, the TC_RCx registers can be used to perform a comparison on the respective current channel counter value (TC_CVx) with the value of TC_RCx register.

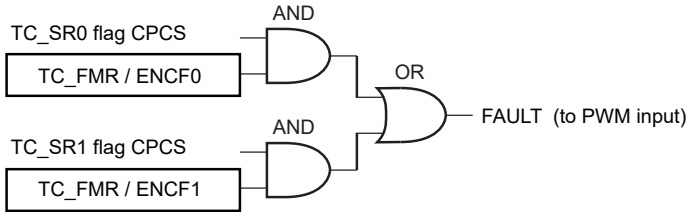
The CPCSx flags can be set accordingly and an interrupt can be generated.

This interrupt is processed but requires an unpredictable amount of time to be achieve the required action.

It is possible to trigger the FAULT output of the TIMER1 with CPCS from TC_SR0 and/or CPCS from TC_SR1. Each source can be independently enabled/disabled in the TC_FMR.

This can be useful to detect an overflow on speed and/or position when QDEC is processed and to act immediately by using the FAULT output.

Figure 50-24. Fault Output Generation



50.6.19 Register Write Protection

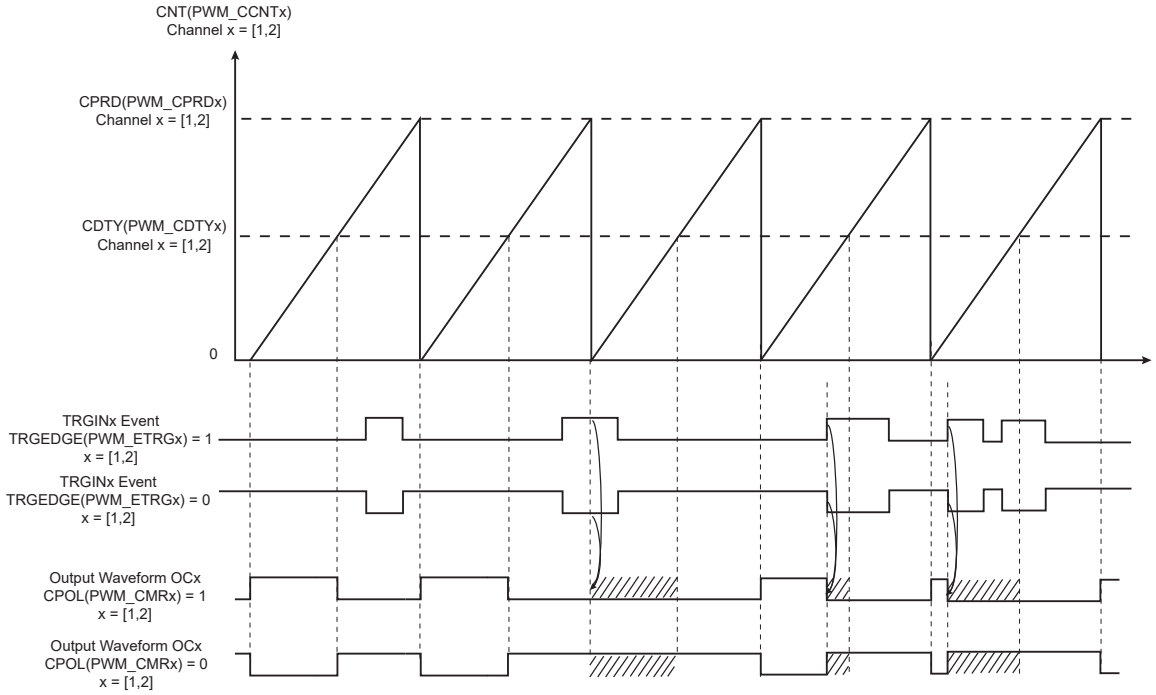
To prevent any single software error from corrupting TC behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the TC Write Protection Mode Register (TC_WPMR).

The Timer Counter clock of the first channel must be enabled to access TC_WPMR.

The following registers can be write-protected when WPEN is set:

- TC Block Mode Register
- TC Channel Mode Register Capture Mode
- TC Channel Mode Register Waveform Mode
- TC Fault Mode Register
- TC Stepper Motor Mode Register
- TC Register A
- TC Register B
- TC Register C
- TC Extended Mode Register

Figure 51-31. Cycle-By-Cycle Duty Mode



51.6.5.3.2 Application Example

The figure below illustrates an application example of the Cycle-by-cycle Duty mode.

In an LED string control circuit, Cycle-by-cycle Duty mode can be used to automatically limit the current in the LED string.

53.7.10 DACC Interrupt Mask Register

Name: DACC_IMR
Offset: 0x2C
Reset: 0x00000000
Property: Read-only

The following configuration values are valid for all listed bit names of this register:

0: The corresponding interrupt is disabled.

1: The corresponding interrupt is enabled.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			EOC1	EOC0			TXRDY1	TXRDY0
Access			R	R			R	R
Reset			0	0			0	0

Bits 4, 5 – EOCx End of Conversion Interrupt Mask of channel x

Bits 0, 1 – TXRDYx Transmit Ready Interrupt Mask of channel x

54.7.5 ACC Interrupt Mask Register

Name: ACC_IMR
Offset: 0x2C
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
								CE
Access								R
Reset								0

Bit 0 – CE Comparison Edge

Value	Description
0	The interrupt is disabled.
1	The interrupt is enabled.

55.6.3 ICM Status Register

Name: ICM_SR
Offset: 0x08
Reset: –
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RMDIS[3:0]				RAWRMDIS[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	–	0	0	0	–

Bit	7	6	5	4	3	2	1	0
								ENABLE
Access								R
Reset								–

Bits 15:12 – RMDIS[3:0] Region Monitoring Disabled Status

Value	Description
0	Region i is being monitored (occurs after integrity check value has been calculated and written to Hash area).
1	Region i monitoring is not being monitored.

Bits 11:8 – RAWRMDIS[3:0] Region Monitoring Disabled Raw Status

Value	Description
0	Region i monitoring has been activated by writing a 1 in RMEN[i] of ICM_CTRL.
1	Region i monitoring has been deactivated by writing a 1 in RMDIS[i] of ICM_CTRL.

Bit 0 – ENABLE ICM Enable Register

Value	Description
0	ICM is disabled.
1	ICM is activated.

Bits 11:8 – RBE[3:0] Region Bus Error Interrupt Enable

Value	Description
0	No effect.
1	When RBE[i] is set to one, the Region i Bus Error interrupt is enabled.

Bits 7:4 – RDM[3:0] Region Digest Mismatch Interrupt Enable

Value	Description
0	No effect.
1	When RDM[i] is set to one, the Region i Digest Mismatch interrupt is enabled.

Bits 3:0 – RHC[3:0] Region Hash Completed Interrupt Enable

Value	Description
0	No effect.
1	When RHC[i] is set to one, the Region i Hash Completed interrupt is enabled.

Symbol		VDDIO Supply		Unit
	Parameter	Min	Max	
SMC_5	A0–A22 Valid before NRD High	(NRD_SETUP + NRD_PULSE) × t_{CPMCK} - 4.3	–	ns
SMC_6	NCS low before NRD High	(NRD_SETUP + NRD_PULSE - NCS_RD_SETUP) × t_{CPMCK} - 2.4	–	ns
SMC_7	NRD Pulse Width	NRD_PULSE × t_{CPMCK} - 0.3	–	ns

Table 58-61. SMC Read Signals - NCS Controlled (READ_MODE = 0)

Symbol		VDDIO Supply		Unit
	Parameter	Min	Max	
NO HOLD Settings (NCS_RD_HOLD = 0)				
SMC_8	Data Setup before NCS High	21.4	–	ns
SMC_9	Data Hold after NCS High	0	–	ns
HOLD Settings (NCS_RD_HOLD ≠ 0)				
SMC_{10}	Data Setup before NCS High	11.7	–	ns
SMC_{11}	Data Hold after NCS High	0	–	ns
HOLD or NO HOLD Settings (NCS_RD_HOLD ≠ 0, NCS_RD_HOLD = 0)				
SMC_{12}	A0–A22 valid before NCS High	(NCS_RD_SETUP + NCS_RD_PULSE) × t_{CPMCK} - 3.9	–	ns
SMC_{13}	NRD low before NCS High	(NCS_RD_SETUP + NCS_RD_PULSE - NRD_SETUP) × t_{CPMCK} - 4.2	–	ns
SMC_{14}	NCS Pulse Width	NCS_RD_PULSE length × t_{CPMCK} - 0.2	–	ns

58.13.1.9.3 Write Timings

Table 58-62. SMC Write Signals - NWE Controlled (WRITE_MODE = 1)

Symbol	VDDIO Supply	1.8V Domain	3.3V Domain	1.8V Domain	3.3V Domain	Unit
	Parameter	Min		Max		
HOLD or NO HOLD Settings (NWE_HOLD ≠ 0, NWE_HOLD = 0)						
SMC_{15}	Data Out Valid before NWE High	NWE_PULSE × t_{CPMCK} - 5.4	NWE_PULSE × t_{CPMCK} - 4.6	–	–	ns
SMC_{16}	NWE Pulse Width	NWE_PULSE × t_{CPMCK} - 0.7	NWE_PULSE × t_{CPMCK} - 0.3	–	–	ns
SMC_{17}	A0–A22 valid before NWE low	NWE_SETUP × t_{CPMCK} - 4.9	NWE_SETUP × t_{CPMCK} - 4.2	–	–	ns

Core Clock/MCK (MHz)	VDDCORE Consumption (AMP1)	Total Consumption (AMP2)	Unit	Wakeup Time	Unit
96/96	12.5	15		1.4	
96/48	7.5	10		2.5	
48/48	7	9.5		2.8	
24/24	3.5	5		5.6	
24/12	2	3		10	
12/12	2	3		11.2	
8/8	1.5	2		16.8	
4/4	1.0	1.5		32.9	
4/2	0.9	1		60	
4/1	0.8	1		112.6	

Table 59-14. Typical Sleep Mode Current Consumption vs. Master Clock (MCK) Variation with Fast RC

Core Clock/MCK (MHz)	VDDCORE Consumption (AMP1)	Total Consumption (AMP2)	Unit	Wakeup Time	Unit
12	2.0	2.0		12	
8	1.5	1.5		18	
4	1.0	1.1		31	
2	0.8	0.8	mA	62	µs
1	0.6	0.7		123	
0.5	0.6	0.6		247	
0.25	0.5	0.5		494	

59.3.3 Wait Mode Current Consumption and Wakeup Time

The Wait mode configuration and measurements are defined as follows:

- Core clock and Master clock stopped
- Current measurement as shown below
- All peripheral clocks deactivated
- BOD disabled
- RTT enabled