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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv71q19b-aabt

19.4.11 Write Protection Mode Register

Name: MATRIX_WPMR
Offset: 0x01E4
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	WPKEY[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	WPKEY[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	WPKEY[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
								WPEN
Access								
Reset								0

Bits 31:8 – WPKEY[23:0] Write Protection Key

Value	Name	Description
0x4D4154	PASSWD	Writing any other value in this field aborts the write operation of the WPEN bit. Always reads as 0.

Bit 0 – WPEN Write Protection Enable
Refer to the "Register Write Protection" section for the list of registers that can be write-protected.

Value	Description
0	Disables the write protection if WPKEY corresponds to 0x4D4154 (“MAT” in ASCII).
1	Enables the write protection if WPKEY corresponds to 0x4D4154 (“MAT” in ASCII).

23.5.4 Supply Controller Wakeup Mode Register

Name: SUPC_WUMR
Offset: 0x0C
Reset: 0x00000000
Property: Read/Write

This register is located in the VDDIO domain.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
						LPDBC[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bit	15	14	13	12	11	10	9	8
		WKUPDBC[2:0]						
Access		R/W	R/W	R/W				
Reset		0	0	0				

Bit	7	6	5	4	3	2	1	0
	LPDBCCLR	LPDBCEN1	LPDBCEN0		RTCEN	RTTEN	SMEN	
Access	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0		0	0	0	

Bits 18:16 – LPDBC[2:0] Low-power Debouncer Period

Value	Name	Description
0	DISABLE	Disables the low-power debouncers.
1	2_RTCOUT	WKUP0/1 in active state for at least 2 RTCOUTx clock periods
2	3_RTCOUT	WKUP0/1 in active state for at least 3 RTCOUTx clock periods
3	4_RTCOUT	WKUP0/1 in active state for at least 4 RTCOUTx clock periods
4	5_RTCOUT	WKUP0/1 in active state for at least 5 RTCOUTx clock periods
5	6_RTCOUT	WKUP0/1 in active state for at least 6 RTCOUTx clock periods
6	7_RTCOUT	WKUP0/1 in active state for at least 7 RTCOUTx clock periods
7	8_RTCOUT	WKUP0/1 in active state for at least 8 RTCOUTx clock periods

Bits 14:12 – WKUPDBC[2:0] Wakeup Inputs Debouncer Period

Value	Name	Description
0	IMMEDIATE	Immediate, no debouncing, detected active at least on one Slow Clock edge.
1	3_SLCK	WKUPx shall be in its active state for at least 3 SLCK periods
2	32_SLCK	WKUPx shall be in its active state for at least 32 SLCK periods
3	512_SLCK	WKUPx shall be in its active state for at least 512 SLCK periods

The user can adjust the value of the Main RC oscillator frequency by modifying the trimming values done in production on 8 MHz and 12 MHz. This may be used to compensate frequency drifts due to temperature or voltage. The values stored in the Flash cannot be erased by a Flash erase command or by the ERASE signal. Values written by the user application in the Oscillator Calibration Register (PMC_OCR) are reset after each power-up or peripheral reset.

By default, SEL4/SEL8/SEL12 are cleared, so the Main RC oscillator is driven with the factory-programmed Flash calibration bits which are programmed during chip production.

In order to calibrate the oscillator lower frequency, SEL4 must be set to ‘1’ and a valid frequency value must be configured in CAL4. Likewise, SEL8/12 must be set to ‘1’ and a trim value must be configured in CAL8/12 in order to adjust the other frequencies of the oscillator.

It is possible to adjust the oscillator frequency while operating from this oscillator. For example, when running on lowest frequency, it is possible to change the CAL4 value if SEL4 is set in PMC_OCR.

At any time, the user can measure the main RC oscillator output frequency by means of the Main Frequency Counter (refer to "Main Frequency Counter"). Once the frequency measurement is done, the main RC oscillator calibration fields (CALMIN, CALx) can be adjusted accordingly to correct this oscillator output frequency.

Related Links

58. Electrical Characteristics for SAM V70/V71
59. Electrical Characteristics for SAM E70/S70

30.5.3 Main Crystal Oscillator

After reset, the Main crystal oscillator is disabled and is not selected as the source of MAINCK.

As the source of MAINCK, the Main crystal oscillator provides a very precise frequency. The software enables or disables this oscillator in order to reduce power consumption via CKGR_MOR.MOSCXTEN.

When disabling this oscillator by clearing the CKGR_MOR.MOSCXTEN, PMC_SR.MOSCXTS is automatically cleared, indicating the oscillator is off.

When enabling this oscillator, the user must initiate the startup time counter. The startup time depends on the characteristics of the external device connected to this oscillator.

When CKGR_MOR.MOSCXTEN and CKGR_MOR.MOSCXTST are written to enable this oscillator, the PIO lines multiplexed with XIN and XOUT are driven by the Main crystal oscillator. PMC_SR.MOSCXTS is cleared and the counter starts counting down on SLCK divided by 8 from the CKGR_MOR.MOSCXTST value. Since the CKGR_MOR.MOSCXTST value is coded with 8 bits, the startup time can be programmed up to 65536 SLCKperiods, corresponding to about 62 ms when running at 32.768 kHz.

When the startup time counter reaches ‘0’, PMC_SR.MOSCXTS is set, indicating that the oscillator is stabilized. Setting the MOSCXTS bit in the Interrupt Mask Register (PMC_IMR) can trigger an interrupt to the processor.

30.5.4 Main Clock Source Selection

The source of MAINCK can be selected from the following:

- The Main RC oscillator
- The Main crystal oscillator
- An external clock signal provided on the XIN input (Bypass mode of the Main crystal oscillator)

The advantage of the Main RC oscillator is its fast startup time. By default, this oscillator is selected to start the system and it must be selected prior to entering Wait mode.

invalidated as soon as the transfer address fails to lie in the selected NCSx address space. For details on these waveforms, refer to 35. Static Memory Controller (SMC).

NAND Flash Signals

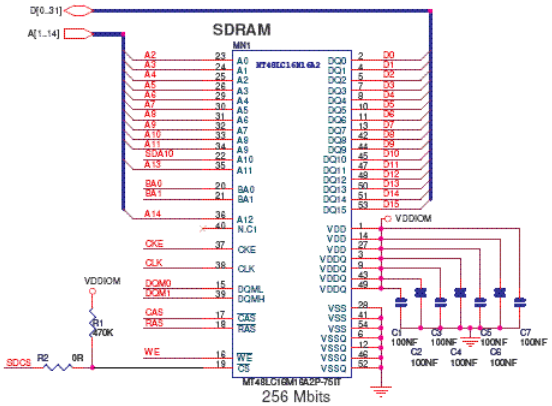
The address latch enable and command latch enable signals on the NAND Flash device are driven by address bits A22 and A21 of the EBI address bus. The command, address or data words on the data bus of the NAND Flash device are distinguished by using their address within the NCSx address space. The chip enable (CE) signal of the device and the ready/busy (R/B) signals are connected to PIO lines. The CE signal then remains asserted even when NCSx is not selected, preventing the device from returning to standby mode.

33.5.4 Implementation Examples

The following hardware configurations are given for illustration only. The user should refer to the memory manufacturer web site to check current device availability.

33.5.4.1 16-bit SDRAM on NCS1

Figure 33-2. Hardware Configuration



Software Configuration

The following configuration has to be performed:

- Enable the SDRAM support by setting the bit SDRAMEN field in the CCFG_SMCNFCS Register in the Bus Matrix.
- Initialize the SDRAM Controller depending on the SDRAM device and system bus frequency.

The Data Bus Width is to be programmed to 16 bits.

The SDRAM initialization sequence is described in 34.5.1 SDRAM Device Initialization.

Figure 35-33. Clock Rate Transition Occurs while the SMC is Performing a Write Operation

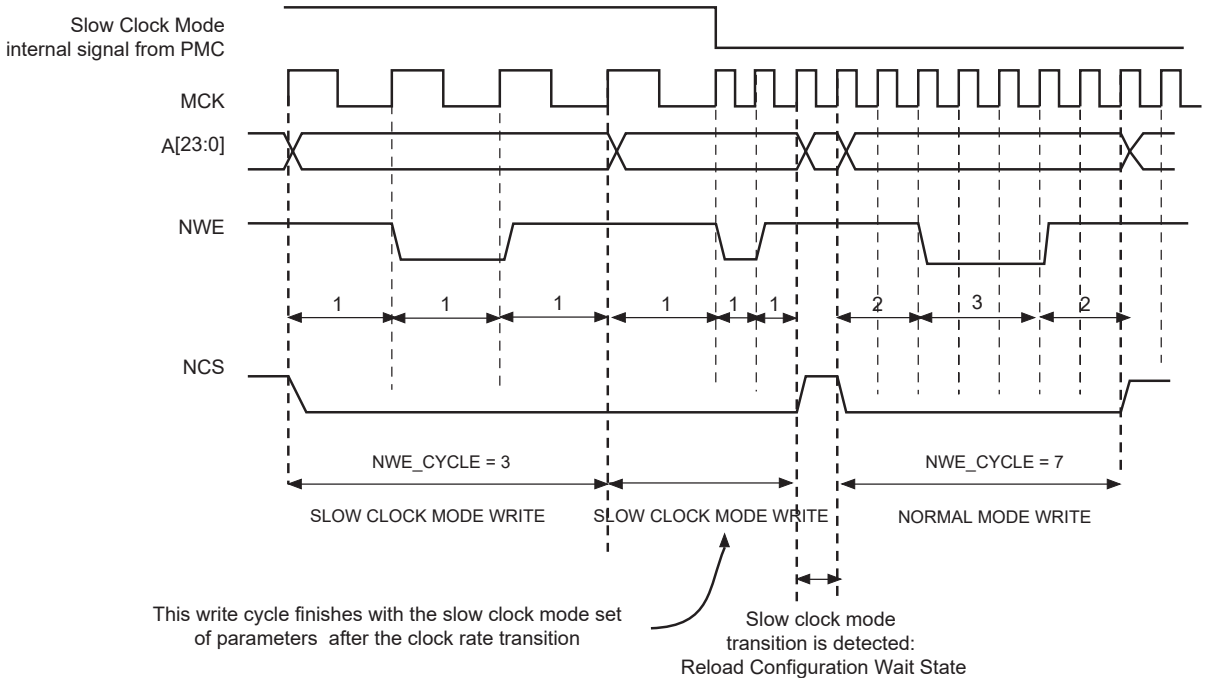
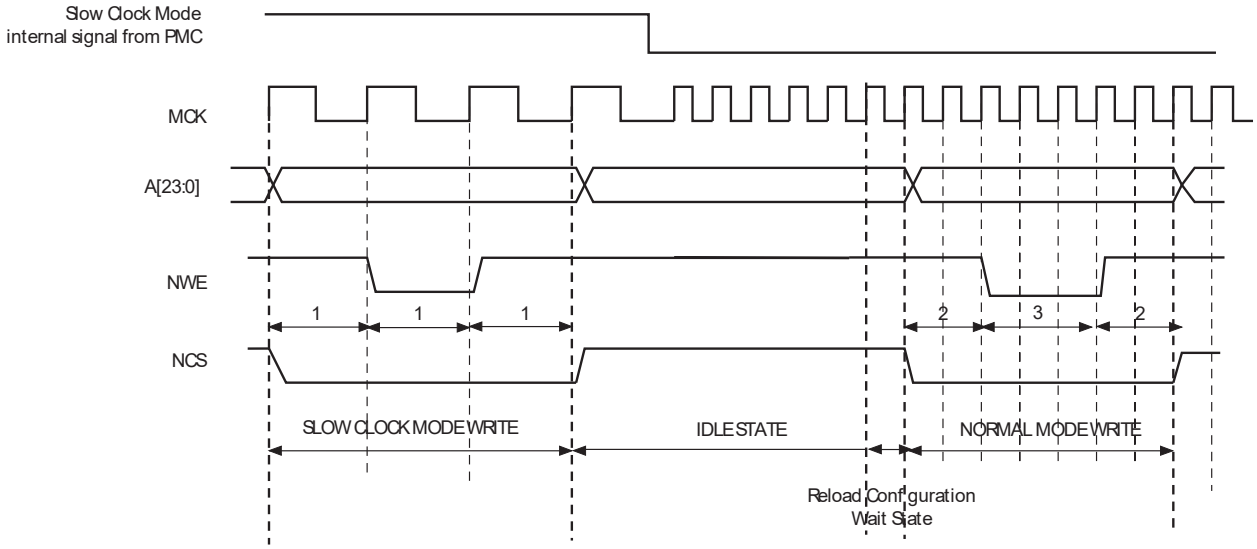


Figure 35-34. Recommended Procedure to Switch from Slow Clock Mode to Normal Mode or from Normal Mode to Slow Clock Mode



35.15 Asynchronous Page Mode

The SMC supports asynchronous burst reads in Page mode, provided that the Page mode is enabled (SMC_MODE.PMEN =1). The page size must be configured in the SMC_MODE register (PS field) to 4, 8, 16 or 32 bytes.

The page defines a set of consecutive bytes into memory. A 4-byte page (resp. 8-, 16-, 32-byte page) is always aligned to 4-byte boundaries (resp. 8-, 16-, 32-byte boundaries) of memory. The MSB of data address defines the address of the page in memory, the LSB of address define the address of the data in the page as detailed in the following table.

Offset	Name	Bit Pos.								
0x04BC	GMAC_CBSCR	7:0							QAE	QBE
		15:8								
		23:16								
		31:24								
0x04C0	GMAC_CBSISQA	7:0	IS[7:0]							
		15:8	IS[15:8]							
		23:16	IS[23:16]							
		31:24	IS[31:24]							
0x04C4	GMAC_CBSISQB	7:0	IS[7:0]							
		15:8	IS[15:8]							
		23:16	IS[23:16]							
		31:24	IS[31:24]							
0x04C8 ... 0x04FF	Reserved									
0x0500	GMAC_ST1RPQ0	7:0	DSTCM[3:0]					QNB[2:0]		
		15:8	UDPM[3:0]				DSTCM[7:4]			
		23:16	UDPM[11:4]							
		31:24			UDPE	DSTCE	UDPM[15:12]			
0x0504	GMAC_ST1RPQ1	7:0	DSTCM[3:0]					QNB[2:0]		
		15:8	UDPM[3:0]				DSTCM[7:4]			
		23:16	UDPM[11:4]							
		31:24			UDPE	DSTCE	UDPM[15:12]			
0x0508	GMAC_ST1RPQ2	7:0	DSTCM[3:0]					QNB[2:0]		
		15:8	UDPM[3:0]				DSTCM[7:4]			
		23:16	UDPM[11:4]							
		31:24			UDPE	DSTCE	UDPM[15:12]			
0x050C	GMAC_ST1RPQ3	7:0	DSTCM[3:0]					QNB[2:0]		
		15:8	UDPM[3:0]				DSTCM[7:4]			
		23:16	UDPM[11:4]							
		31:24			UDPE	DSTCE	UDPM[15:12]			
0x0510 ... 0x053F	Reserved									
0x0540	GMAC_ST2RPQ0	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x0544	GMAC_ST2RPQ1	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x0548	GMAC_ST2RPQ2	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE

Offset	Name	Bit Pos.								
0x054C	GMAC_ST2RPQ3	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x0550	GMAC_ST2RPQ4	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x0554	GMAC_ST2RPQ5	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x0558	GMAC_ST2RPQ6	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x055C	GMAC_ST2RPQ7	7:0		VLANP[2:0]				QNB[2:0]		
		15:8	COMPA[2:0]			ETHE	I2ETH[2:0]			VLANE
		23:16	COMPB[4:0]					COMPAE	COMPA[4:3]	
		31:24		COMPCE	COMPC[4:0]					COMPBE
0x0560 ... 0x05FF	Reserved									
0x0600	GMAC_IERPQ1	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x0604	GMAC_IERPQ2	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x0608	GMAC_IERPQ3	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x060C	GMAC_IERPQ4	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x0610	GMAC_IERPQ5	7:0	TCOMP	TFC	RLEX			RXUBR	RCOMP	
		15:8					HRESP	ROVR		
		23:16								
		31:24								
0x0614 ... 0x061F	Reserved									

Bits 23:19 – COMPB[4:0] Index of Screening Type 2 Compare Word 0/Word 1 register x
COMPB is a pointer to the compare registers GMAC_ST2CW0x and GMAC_ST2CW1x. When COMPBE=1, the compare is true if the data at the frame offset ANDed with the value MASKVAL is equal to the value of COMPVAL ANDed with the value of MASKVAL.

Bit 18 – COMPAE Compare A Enable

Value	Description
0	Compare A is disabled.
1	Comparison via the register designated by index COMPA is enabled.

Bits 17:13 – COMPA[4:0] Index of Screening Type 2 Compare Word 0/Word 1 register x
COMPA is a pointer to the compare registers GMAC_ST2CW0x and GMAC_ST2CW1x. When COMPAE=1, the compare is true if the data at the frame offset ANDed with the value MASKVAL is equal to the value of COMPVAL ANDed with the value of MASKVAL.

Bit 12 – ETHE EtherType Enable

Value	Description
0	EtherType match is disabled
1	EtherType match with bits [15:0] of the register designated by the value in I2ETH is enabled

Bits 11:9 – I2ETH[2:0] Index of Screening Type 2 EtherType register x
When EtherType is enabled (ETHE=1), the EtherType field (last EtherType in the header if the frame is VLAN-tagged) is compared with bits [15:0] in the register designated by the value of this bit field.

Bit 8 – VLANE VLAN Enable

Value	Description
0	VLAN match disabled
1	VLAN match is enabled

Bits 6:4 – VLANP[2:0] VLAN Priority
When VLAN match is enabled (VLANE=1), the VLAN Priority field of the received frame is matched against the value of this bit field.

Bits 2:0 – QNB[2:0] Queue Number
If a match is successful, then the queue value programmed in QNB is allocated to the frame.

Offset	Name	Bit Pos.								
		23:16					STALLRQ	RSTDT	NYETDIS	EPDISHDMA
		31:24								
0x01C4	USBHS_DEVEPTIMR1 (ISOENPT)	7:0	SHORTPACKETE	CRCERRE	OVERFE	HBISOFLUSHE	HBISOINERRE	UNDERFE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE		ERRORTRANSE	DATAXE	MDATAE
		23:16						RSTDT		EPDISHDMA
		31:24								
0x01C8	USBHS_DEVEPTIMR2	7:0	SHORTPACKETE	STALLEDE	OVERFE	NAKINE	NAKOUTE	RXSTPE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE				
		23:16					STALLRQ	RSTDT	NYETDIS	EPDISHDMA
		31:24								
0x01C8	USBHS_DEVEPTIMR2 (ISOENPT)	7:0	SHORTPACKETE	CRCERRE	OVERFE	HBISOFLUSHE	HBISOINERRE	UNDERFE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE		ERRORTRANSE	DATAXE	MDATAE
		23:16						RSTDT		EPDISHDMA
		31:24								
0x01CC	USBHS_DEVEPTIMR3	7:0	SHORTPACKETE	STALLEDE	OVERFE	NAKINE	NAKOUTE	RXSTPE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE				
		23:16					STALLRQ	RSTDT	NYETDIS	EPDISHDMA
		31:24								
0x01CC	USBHS_DEVEPTIMR3 (ISOENPT)	7:0	SHORTPACKETE	CRCERRE	OVERFE	HBISOFLUSHE	HBISOINERRE	UNDERFE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE		ERRORTRANSE	DATAXE	MDATAE
		23:16						RSTDT		EPDISHDMA
		31:24								
0x01D0	USBHS_DEVEPTIMR4	7:0	SHORTPACKETE	STALLEDE	OVERFE	NAKINE	NAKOUTE	RXSTPE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE				
		23:16					STALLRQ	RSTDT	NYETDIS	EPDISHDMA
		31:24								
0x01D0	USBHS_DEVEPTIMR4 (ISOENPT)	7:0	SHORTPACKETE	CRCERRE	OVERFE	HBISOFLUSHE	HBISOINERRE	UNDERFE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE		ERRORTRANSE	DATAXE	MDATAE
		23:16						RSTDT		EPDISHDMA
		31:24								
0x01D4	USBHS_DEVEPTIMR5	7:0	SHORTPACKETE	STALLEDE	OVERFE	NAKINE	NAKOUTE	RXSTPE	RXOUTE	TXINE
		15:8		FIFOCON	KILLBK	NBUSYBKE				
		23:16					STALLRQ	RSTDT	NYETDIS	EPDISHDMA
		31:24								

Offset	Name	Bit Pos.								
		31:24								
0x0590	USBHS_HSTPIPIFR0 (INTPIPES)	7:0	SHORTPACKETIS	RXSTALLDIS	OVERFIS	NAKEDIS	PERRIS	UNDERFIS	TXOUTIS	RXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x0590	USBHS_HSTPIPIFR0 (ISOPIPES)	7:0	SHORTPACKETIS	CRCERRIS	OVERFIS	NAKEDIS	PERRIS	UNDERFIS	TXOUTIS	RXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x0594	USBHS_HSTPIPIFR1 (INTPIPES)	7:0	SHORTPACKETIS	RXSTALLDIS	OVERFIS	NAKEDIS	PERRIS	UNDERFIS	TXOUTIS	RXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x0594	USBHS_HSTPIPIFR1 (ISOPIPES)	7:0	SHORTPACKETIS	CRCERRIS	OVERFIS	NAKEDIS	PERRIS	UNDERFIS	TXOUTIS	RXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x0598	USBHS_HSTPIPIFR2 (INTPIPES)	7:0	SHORTPACKETIS	RXSTALLDIS	OVERFIS	NAKEDIS	PERRIS	UNDERFIS	TXOUTIS	RXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x0598	USBHS_HSTPIPIFR2 (ISOPIPES)	7:0	SHORTPACKETIS	CRCERRIS	OVERFIS	NAKEDIS	PERRIS	UNDERFIS	TXOUTIS	RXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x059C	USBHS_HSTPIPIFR3 (INTPIPES)	7:0	SHORTPACKETIS	RXSTALLDIS	OVERFIS	NAKEDIS	PERRIS	UNDERFIS	TXOUTIS	RXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x059C	USBHS_HSTPIPIFR3 (ISOPIPES)	7:0	SHORTPACKETIS	CRCERRIS	OVERFIS	NAKEDIS	PERRIS	UNDERFIS	TXOUTIS	RXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								
0x05A0	USBHS_HSTPIPIFR4 (INTPIPES)	7:0	SHORTPACKETIS	RXSTALLDIS	OVERFIS	NAKEDIS	PERRIS	UNDERFIS	TXOUTIS	RXINIS
		15:8				NBUSYBKS				
		23:16								
		31:24								

Value	Description
0	Cleared when USBHS_HSTPIPICR.TXOUTIC = 1.
1	Set when the current OUT bank is free and can be filled. This triggers an interrupt if USBHS_HSTPIPIMR.TXOUTE = 1.

Bit 0 – RXINI Received IN Data Interrupt

Value	Description
0	Cleared when USBHS_HSTPIPICR.RXINIC = 1.
1	Set when a new USB message is stored in the current bank of the pipe. This triggers an interrupt if USBHS_HSTPIPIMR.RXINE = 1.

Bit 21 – DCRCE Data CRC Error Interrupt Mask

Bit 20 – RTOE Response Time-out Error Interrupt Mask

Bit 19 – RENDE Response End Bit Error Interrupt Mask

Bit 18 – RCRCE Response CRC Error Interrupt Mask

Bit 17 – RDIRE Response Direction Error Interrupt Mask

Bit 16 – RINDE Response Index Error Interrupt Mask

Bit 13 – CSRCV Completion Signal Received Interrupt Mask

Bit 12 – SDIOWAIT SDIO Read Wait Operation Status Interrupt Mask

Bit 8 – SDIOIRQA SDIO Interrupt for Slot A Interrupt Mask

Bit 5 – NOTBUSY Data Not Busy Interrupt Mask

Bit 4 – DTIP Data Transfer in Progress Interrupt Mask

Bit 3 – BLKE Data Block Ended Interrupt Mask

Bit 2 – TXRDY Transmit Ready Interrupt Mask

Bit 1 – RXRDY Receiver Ready Interrupt Mask

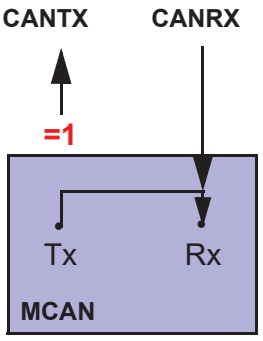
Bit 0 – CMDRDY Command Ready Interrupt Mask

Bit 1 – LKSYSCMD Network Lock System Command Detected in the System Quadlet (cleared by writing a 0)
Set by hardware, cleared by software.

Bit 0 – RSTSYSCMD Reset System Command Detected in the System Quadlet (cleared by writing a 0)
Set by hardware, cleared by software.

The Bus Monitoring mode can be used to analyze the traffic on a CAN bus without affecting it by the transmission of dominant bits. The figure below shows the connection of signals CANTX and CANRX to the MCAN in Bus Monitoring mode.

Figure 49-3. Pin Control in Bus Monitoring Mode



Bus Monitoring Mode

49.5.1.7 Disabled Automatic Retransmission

According to the CAN Specification (see ISO11898-1, 6.3.3 Recovery Management), the MCAN provides means for automatic retransmission of frames that have lost arbitration or that have been disturbed by errors during transmission. By default automatic retransmission is enabled. To support time-triggered communication as described in ISO 11898-1, chapter 9.2, the automatic retransmission may be disabled via MCAN_CCCR.DAR.

49.5.1.7.1 Frame Transmission in DAR Mode

In DAR mode, all transmissions are automatically cancelled after they start on the CAN bus. A Tx Buffer's Tx Request Pending bit TXBRP.TRPx is reset after successful transmission, when a transmission has not yet been started at the point of cancellation, has been aborted due to lost arbitration, or when an error occurred during frame transmission.

- Successful transmission:
  Corresponding Tx Buffer Transmission Occurred bit MCAN_TXBTO.TOx set

  Corresponding Tx Buffer Cancellation Finished bit MCAN_TXBCF.CFx not set
- Successful transmission in spite of cancellation:
  Corresponding Tx Buffer Transmission Occurred bit MCAN_TXBTO.TOx set

  Corresponding Tx Buffer Cancellation Finished bit MCAN_TXBCF.CFx set
- Arbitration lost or frame transmission disturbed:
  Corresponding Tx Buffer Transmission Occurred bit MCAN_TXBTO.TOx not set

  Corresponding Tx Buffer Cancellation Finished bit MCAN_TXBCF.CFx set

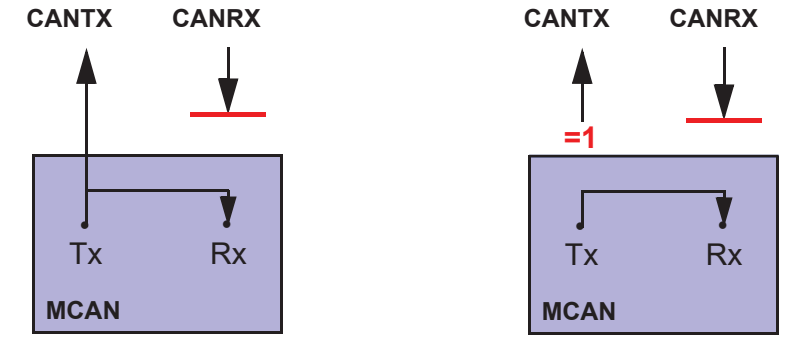
In case of a successful frame transmission, and if storage of Tx events is enabled, a Tx Event FIFO element is written with Event Type ET = “10” (transmission in spite of cancellation).

49.5.1.8 Power-down (Sleep Mode)

The MCAN can be set into Power-down mode via bit MCAN_CCCR.CSR.

When all pending transmission requests have completed, the MCAN waits until bus idle state is detected. Then the MCAN sets MCAN_CCCR.INIT to prevent any further CAN transfers. Now the MCAN acknowledges that it is ready for power down by setting to one the bit MCAN_CCCR.CSA. In this state, before the clocks are switched off, further register accesses can be made. A write access to

Figure 49-4. Pin Control in Loop Back Modes



49.5.2 Timestamp Generation

For timestamp generation the MCAN supplies a 16-bit wrap-around counter. A prescaler TSCC.TCP can be configured to clock the counter in multiples of CAN bit times (1…16). The counter is readable via MCAN_TSCV.TSC. A write access to the Timestamp Counter Value register (MCAN_TSCV) resets the counter to zero. When the timestamp counter wraps around, interrupt flag MCAN_IR.TSW is set.

On start of frame reception / transmission the counter value is captured and stored into the timestamp section of an Rx Buffer / Rx FIFO (RXTS[15:0]) or Tx Event FIFO (TXTS[15:0]) element.

By programming bit MCAN_TSCC.TSS an external 16-bit timestamp can be used. See Timestamping for more details.

49.5.3 Timeout Counter

To signal timeout conditions for Rx FIFO 0, Rx FIFO 1, and the Tx Event FIFO, the MCAN supplies a 16-bit Timeout Counter. It operates as down-counter and uses the same prescaler controlled by TSCC.TCP as the Timestamp Counter. The Timeout Counter is configured via the Timeout Counter Configuration register (MCAN_TOCC). The actual counter value can be read from MCAN_TOCV.TOC. The Timeout Counter can only be started while MCAN_CCCR.INIT = ‘0’. It is stopped when MCAN_CCCR.INIT = ‘1’, e.g. when the MCAN enters Bus_Off state.

The operating mode is selected by MCAN_TOCC.TOS. When operating in Continuous mode, the counter starts when MCAN_CCCR.INIT is reset. A write to MCAN_TOCV presets the counter to the value configured by MCAN_TOCC.TOP and continues down-counting.

When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by MCAN_TOCC.TOP. Down-counting is started when the first FIFO element is stored. Writing to MCAN_TOCV has no effect.

When the counter reaches zero, interrupt flag MCAN_IR.TOO is set. In Continuous mode, the counter is immediately restarted at MCAN_TOCC.TOP.

Note: The clock signal for the Timeout Counter is derived from the CAN Core’s sample point signal. Therefore the point in time where the Timeout Counter is decremented may vary due to the synchronization / re-synchronization mechanism of the CAN Core. If the bit rate switch feature in CAN FD is used, the timeout counter is clocked differently in arbitration and data field.

49.5.4 Rx Handling

The Rx Handler controls the acceptance filtering, the transfer of received messages to the Rx Buffers or to one of the two Rx FIFOs, as well as the Rx FIFO’s Put and Get Indices.

50.7.4 TC Stepper Motor Mode Register

Name: TC_SMMRx
Offset: 0x08 + x*0x40 [x=0..2]
Reset: 0x00000000
Property: R/W

This register can only be written if the WPEN bit is cleared in the TC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
							DOWN	GCEN
Access							R/W	R/W
Reset							0	0

Bit 1 – DOWN Down Count

Value	Description
0	Up counter.
1	Down counter.

Bit 0 – GCEN Gray Count Enable

Value	Description
0	TIOAx [x=0..2] and TIOBx [x=0..2] are driven by internal counter of channel x.
1	TIOAx [x=0..2] and TIOBx [x=0..2] are driven by a 2-bit Gray counter.

50.7.10 TC Interrupt Status Register

Name: TC_SRx
Offset: 0x20 + x*0x40 [x=0..2]
Reset: 0x00000000
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
						MTIOB	MTIOA	CLKSTA
Access						R	R	R
Reset						0	0	0

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	ETRGS	LDRBS	LDRAS	CPCS	CPBS	CPAS	LOVRS	COVFS
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit 18 – MTIOB TIOBx Mirror

Value	Description
0	TIOBx is low. If TC_CMRx.WAVE = 0, TIOBx pin is low. If TC_CMRx.WAVE = 1, TIOBx is driven low.
1	TIOBx is high. If TC_CMRx.WAVE = 0, TIOBx pin is high. If TC_CMRx.WAVE = 1, TIOBx is driven high.

Bit 17 – MTIOA TIOAx Mirror

Value	Description
0	TIOAx is low. If TC_CMRx.WAVE = 0, TIOAx pin is low. If TC_CMRx.WAVE = 1, TIOAx is driven low.
1	TIOAx is high. If TC_CMRx.WAVE = 0, TIOAx pin is high. If TC_CMRx.WAVE = 1, TIOAx is driven high.

Bit 16 – CLKSTA Clock Enabling Status

Value	Description
0	Clock is disabled.
1	Clock is enabled.

- N = 12 when KEYSIZE = 1
- N = 14 when KEYSIZE = 2

The processing time represents the number of clock cycles that the AES needs in order to perform one encryption/decryption.

Note: The best performance is achieved with PROCDLY equal to 0.

Bit 3 – DUALBUFF Dual Input Buffer

Value	Name	Description
0	INACTIVE	AES_IDATARx cannot be written during processing of previous block.
1	ACTIVE	AES_IDATARx can be written during processing of previous block when SMOD = 2. It speeds up the overall runtime of large files.

Bit 1 – GTAGEN GCM Automatic Tag Generation Enable

Value	Description
0	Automatic GCM Tag generation disabled.
1	Automatic GCM Tag generation enabled.

Bit 0 – CIPHER Processing Mode

Value	Description
0	Decrypts data.
1	Encrypts data.

Symbol	VDDIO Supply	1.8V Domain	3.3V Domain	1.8V Domain	3.3V Domain	Unit
	Parameter	Min		Max		
NO HOLD Settings (NWE_HOLD = 0)						
SMC_{21}	NWE High to Data OUT, NBS0/A0 NBS1, A1, A2–A25, NCS change(1)	2.1	1.5	–	–	ns

Note:
Hold length = total cycle duration - setup duration - pulse duration. “hold length” is for “NCS_WR_HOLD length” or “NWE_HOLD length”

Table 59-63. SMC Write NCS Controlled (WRITE_MODE = 0)

Symbol	VDDIO Supply	1.8V Domain	3.3V Domain	1.8V Domain	3.3V Domain	Unit
	Parameter	Min		Max		
SMC_{22}	Data Out Valid before NCS High	NCS_WR_PULSE × t_{CPMCK} - 2.8	NCS_WR_PULSE × t_{CPMCK} - 3.9	—	—	ns
SMC_{23}	NCS Pulse Width	NCS_WR_PULSE × t_{CPMCK} - 0.9	NCS_WR_PULSE × t_{CPMCK} - 0.2	—	—	ns
SMC_{24}	A0–A22 valid before NCS low	NCS_WR_SETUP × t_{CPMCK} - 4.0	NCS_WR_SETUP × t_{CPMCK} - 4.6	—	—	ns
SMC_{25}	NWE low before NCS high	(NCS_WR_SETUP - NWE_SETUP + NCS pulse) × t_{CPMCK} - 4.6	(NCS_WR_SETUP - NWE_SETUP + NCS pulse) × t_{CPMCK} - 4.6	—	—	ns
SMC_{26}	NCS High to Data Out, A0–A25, change	NCS_WR_HOLD × t_{CPMCK} - 4.4	NCS_WR_HOLD × t_{CPMCK} - 3.4	—	—	ns
SMC_{27}	NCS High to NWE Inactive	(NCS_WR_HOLD - NWE_HOLD) × t_{CPMCK} - 2.8	(NCS_WR_HOLD - NWE_HOLD) × t_{CPMCK} - 2.4	—	—	ns

Timings are given in the 3.3V domain, with VDDIO from 2.85V to 3.6V, maximum external capacitor = 50 pF.

Timings are given assuming a capacitance load on data, control and address pads.

In the tables that follow, t_{CPMCK} is MCK period.

59.13.1.13.3 MII Mode

Table 59-71. GMAC MII Mode Timings

Symbol	Parameter	Min	Max	Unit
$GMAC_4$	Setup for GCOL from GTXCK rising	10	–	ns
$GMAC_5$	Hold for GCOL from GTXCK rising	10	–	
$GMAC_6$	Setup for GCRS from GTXCK rising	10	–	
$GMAC_7$	Hold for GCRS from GTXCK rising	10	–	
$GMAC_8$	GTXER toggling from GTXCK rising	10	25	
$GMAC_9$	GTXEN toggling from GTXCK rising	10	25	
$GMAC_{10}$	GTX toggling from GTXCK rising	10	25	
$GMAC_{11}$	Setup for GRX from GRXCK	10	–	
$GMAC_{12}$	Hold for GRX from GRXCK	10	–	
$GMAC_{13}$	Setup for GRXER from GRXCK	10	–	
$GMAC_{14}$	Hold for GRXER from GRXCK	10	–	
$GMAC_{15}$	Setup for GRXDV from GRXCK	10	–	
$GMAC_{16}$	Hold for GRXDV from GRXCK	10	–	