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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv71q21b-aabt

Voltage

- Single supply voltage from 3.0V to 3.6V for Qualification AEC - Q100 Grade 2 Devices
- Single Supply voltage from 1.7V to 3.6V for Industrial Temperature Devices

Packages

- LQFP144, 144-lead LQFP, 20x20 mm, pitch 0.5 mm
- LFBGA144, 144-ball LFBGA, 10x10 mm, pitch 0.8 mm
- TFBGA144, 144-ball TFBGA, 10x10mm, pitch 0.8 mm
- UFBGA144, 144-ball UFBGA, 6x6 mm, pitch 0.4 mm
- LQFP100, 100-lead LQFP, 14x14 mm, pitch 0.5 mm
- TFBGA100, 100-ball TFBGA, 9x9 mm, pitch 0.8 mm
- VFBGA100, 100-ball VFBGA, 7x7 mm, pitch 0.65 mm
- LQFP64, 64-lead LQFP, 10x10 mm, pitch 0.5 mm
- QFN64, 64-pad QFN 9x9 mm, pitch 0.5 mm, with wettable flanks

19.4.1 Bus Matrix Master Configuration Registers

Name: MATRIX_MCFGx
Offset: 0x00 + x*0x04 [x=0..12]
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
						ULBT[2:0]		
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:0 – ULBT[2:0] Undefined Length Burst Type

Value	Name	Description
0	UNLTD_LENGTH	Unlimited Length Burst—No predicted end of burst is generated, therefore INCR bursts coming from this master can only be broken if the Slave Slot Cycle Limit is reached. If the Slot Cycle Limit is not reached, the burst is normally completed by the master, at the latest, on the next AHB 1-Kbyte address boundary, allowing up to 256-beat word bursts or 128-beat double-word bursts. This value should not be used in the very particular case of a master capable of performing back-to-back undefined length bursts on a single slave, since this could indefinitely freeze the slave arbitration and thus prevent another master from accessing this slave.
1	SINGLE_ACCESS	Single Access—The undefined length burst is treated as a succession of single accesses, allowing re-arbitration at each beat of the INCR burst or bursts sequence.
2	4BEAT_BURST	4-beat Burst—The undefined length burst or bursts sequence is split into 4-beat bursts or less, allowing re-arbitration every 4 beats.
3	8BEAT_BURST	8-beat Burst—The undefined length burst or bursts sequence is split into 8-beat bursts or less, allowing re-arbitration every 8 beats.

20. USB Transmitter Macrocell Interface (UTMI)

20.1 Description

The USB Transmitter Macrocell Interface (UTMI) registers manage specific aspects of the integrated USB transmitter macrocell functionality not controlled in USB sections.

20.2 Embedded Characteristics

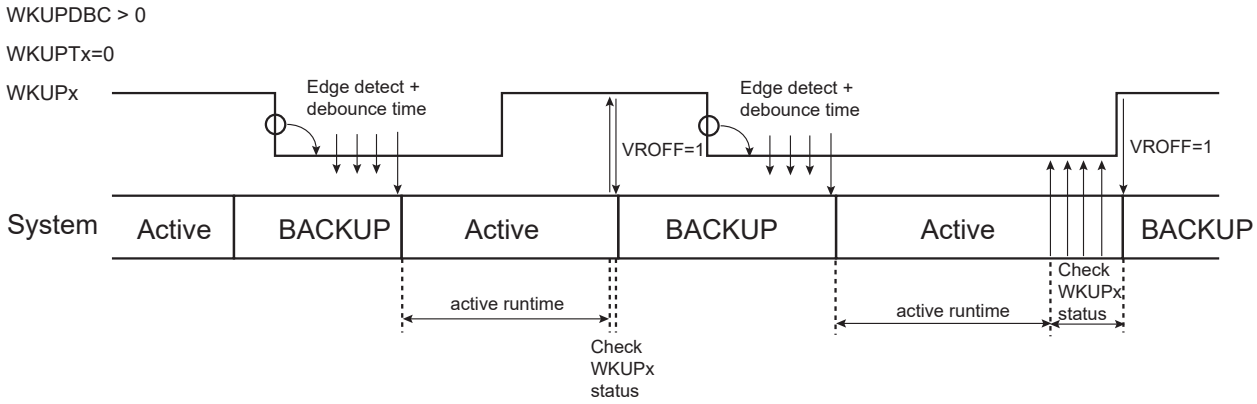
- 32-bit UTMI Registers Control Product-specific Behavior

The resulting signals are wired-ORed to trigger a debounce counter, which is programmed with SUPC_WUMR.WKUPDBC. This field selects a debouncing period of 3, 32, 512, 4,096 or 32,768 slow clock cycles. The duration of these periods corresponds, respectively, to about 100 µs, about 1 ms, about 16 ms, about 128 ms and about 1 second (for a typical slow clock frequency of 32 kHz). Programming SUPC_WUMR.WKUPDBC to 0 selects an immediate wakeup, i.e., an enabled WKUP pin must be active according to its polarity during a minimum of one slow clock period to wake up the core power supply.

If an enabled WKUP pin is asserted for a duration longer than the debouncing period, a wakeup of the core power supply is started and the signals, WKUP0 to WKUPx as shown in "Wakeup Sources", are latched in SUPC_SR. This allows the user to identify the source of the wakeup. However, if a new wakeup condition occurs, the primary information is lost. No new wakeup can be detected since the primary wakeup condition has disappeared.

Before instructing the system to enter Backup mode, if the field SUPC_WUMR.WKUPDBC > 0, it must be checked that none of the WKUPx pins that are enabled for a wakeup (exit from Backup mode) holds an active polarity. This is checked by reading the pin status in the PIO Controller. If SUPC_WUIR.WKUPENx=1 and the pin WKUPx holds an active polarity, the system must not be instructed to enter Backup mode.

Figure 23-8. Entering and Exiting Backup Mode with a WKUP Pin



23.4.9.2 Low-power Tamper Detection and Anti-Tampering

Low-power debouncer inputs (WKUP0, WKUP1) can be used for tamper detection. If the tamper sensor is biased through a resistor and constantly driven by the power supply, this leads to power consumption as long as the tamper detection switch is in its active state. To prevent power consumption when the switch is in active state, the tamper sensor circuitry must be intermittently powered, and thus a specific waveform must be applied to the sensor circuitry.

The waveform is generated using RTCOUTx in all modes including Backup mode. Refer to the section "Real-Time Clock (RTC)" for waveform generation.

Separate debouncers are embedded, one for WKUP0 input, one for WKUP1 input.

The WKUP0 and/or WKUP1 inputs perform a system wakeup upon tamper detection. This is enabled by setting SUPC_WUMR.LPDBCEN0/1.

WKUP0 and/or WKUP1 inputs can also be used when VDDCORE is powered to detect a tamper.

When SUPC_WUMR.LPDBCENx is written to '1', WKUPx pins must not be configured to act as a debouncing source for the WKUPDBC counter (WKUPENx must be cleared in SUPC_WUIR).

- RTC Mode Register
- RTC Time Alarm Register
- RTC Calendar Alarm Register
- General Purpose Backup Registers
- Supply Controller Control Register
- Supply Controller Supply Monitor Mode Register
- Supply Controller Mode Register
- Supply Controller Wakeup Mode Register
- Supply Controller Wakeup Inputs Register

23.4.11 Register Bits in Backup Domain (VDDIO)

The following configuration registers, or certain bits of the registers, are physically located in the product backup domain:

- RSTC Mode Register (all bits)
- RTT Mode Register (all bits)
- RTT Alarm Register (all bits)
- RTC Control Register (all bits)
- RTC Mode Register (all bits)
- RTC Time Alarm Register (all bits)
- RTC Calendar Alarm Register (all bits)
- General Purpose Backup Registers (all bits)
- Supply Controller Control Register (see register description for details)
- Supply Controller Supply Monitor Mode Register (all bits)
- Supply Controller Mode Register (see register description for details)
- Supply Controller Wakeup Mode Register (all bits)
- Supply Controller Wakeup Inputs Register (all bits)
- Supply Controller Status Register (all bits)

output. To accommodate the measure, several clock frequencies can be selected among 1 Hz, 32 Hz, 64 Hz, 512 Hz.

The clock calibration correction drives the internal RTC counters but can also be observed in the RTC output when one of the following three frequencies 1 Hz, 32 Hz or 64 Hz is configured. The correction is not visible in the RTC output if 512 Hz frequency is configured.

Note that this adjustment does not take into account the temperature variation.

The frequency drift (up to -200 ppm) due to temperature variation can be compensated using a reference time if the application can access such a reference. If a reference time cannot be used, a temperature sensor can be placed close to the crystal oscillator in order to get the operating temperature of the crystal oscillator. Once obtained, the temperature may be converted using a lookup table (describing the accuracy/temperature curve of the crystal oscillator used) and RTC_MR configured accordingly. The calibration can be performed on-the-fly. This adjustment method is not based on a measurement of the crystal frequency/drift and therefore can be improved by means of the networking capability of the target application.

If no crystal frequency adjustment has been done during manufacturing, it is still possible to do it. In the case where a reference time of the day can be obtained through LAN/WAN network, it is possible to calculate the drift of the application crystal oscillator by comparing the values read on RTC Time Register (RTC_TIMR) and programming the HIGHPPM and CORRECTION fields on RTC_MR according to the difference measured between the reference time and those of RTC_TIMR.

27.5.8 Waveform Generation

Waveforms can be generated in order to take advantage of the RTC inherent prescalers while the RTC is the only powered circuitry (Low-power mode of operation, Backup mode) or in any active mode. Entering Backup or Low-power operating modes does not affect the waveform generation outputs.

The outputs RTCOUT0 and RTCOUT1 can be configured to provide several types of waveforms. The figure below illustrates the different signals available to generate RTCOUT0 and RTCOUT1.

PIO lines associated to the RTC outputs automatically select these waveforms as soon as RTC_MR.OUT0/OUT1 differ from 0 .

31.20.17 PMC Interrupt Mask Register

Name: PMC_IMR
Offset: 0x006C
Reset: 0x00000000
Property: Read-only

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			XT32KERR			CFDEV	MOSCRCS	MOSCSELS
Access								
Reset			0			0	0	0

Bit	15	14	13	12	11	10	9	8
		PCKRDY6	PCKRDY5	PCKRDY4	PCKRDY3	PCKRDY2	PCKRDY1	PCKRDY0
Access								
Reset		0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		LOCKU			MCKRDY		LOCKA	MOSCXTS
Access								
Reset		0			0		0	0

Bit 21 – XT32KERR 32.768 kHz Crystal Oscillator Error Interrupt Mask

Bit 18 – CFDEV Clock Failure Detector Event Interrupt Mask

Bit 17 – MOSCRCS Main RC Status Interrupt Mask

Bit 16 – MOSCSELS Main Clock Source Oscillator Selection Status Interrupt Mask

Bits 8, 9, 10, 11, 12, 13, 14 – PCKRDY Programmable Clock Ready x Interrupt Mask

Bit 6 – LOCKU UTMI PLL Lock Interrupt Mask

Bit 3 – MCKRDY Master Clock Ready Interrupt Mask

Bit 1 – LOCKA PLLA Lock Interrupt Mask

Bit 0 – MOSCXTS Main Crystal Oscillator Status Interrupt Mask

32. Parallel Input/Output Controller (PIO)

32.1 Description

The Parallel Input/Output Controller (PIO) manages up to 32 fully programmable input/output lines. Each I/O line may be dedicated as a general-purpose I/O or be assigned to a function of an embedded peripheral. This ensures effective optimization of the pins of the product.

Each I/O line is associated with a bit number in all of the 32-bit registers of the 32-bit wide user interface.

Each I/O line of the PIO Controller features the following:

- An input change interrupt enabling level change detection on any I/O line
- Additional Interrupt modes enabling rising edge, falling edge, low-level or high-level detection on any I/O line
- A glitch filter providing rejection of glitches lower than one-half of peripheral clock cycle
- A debouncing filter providing rejection of unwanted pulses from key or push button operations
- Multi-drive capability similar to an open drain I/O line
- Control of the I/O line pullup and pulldown
- Input visibility and output control

The PIO Controller also features a synchronous output providing up to 32 bits of data output in a single write operation.

An 8-bit Parallel Capture mode is also available which can be used to interface a CMOS digital image sensor, an ADC, a DSP synchronous port in Synchronous mode, etc.

32.2 Embedded Characteristics

- Up to 32 Programmable I/O Lines
- Fully Programmable through Set/Clear Registers
- Multiplexing of Four Peripheral Functions per I/O Line
- For each I/O Line (Whether Assigned to a Peripheral or Used as General Purpose I/O)
  - Input Change Interrupt
  - Programmable Glitch Filter
  - Programmable Debouncing Filter
  - Multi-drive Option Enables Driving in Open Drain
  - Programmable Pullup on Each I/O Line
  - Pin Data Status Register, Supplies Visibility of the Level on the Pin at Any Time
  - Additional Interrupt Modes on a Programmable Event: Rising Edge, Falling Edge, Low-Level or High-Level
  - Lock of the Configuration by the Connected Peripheral
- Synchronous Output, Provides Set and Clear of Several I/O Lines in a Single Write
- Register Write Protection
- Programmable Schmitt Trigger Inputs
- Programmable I/O Drive
- Parallel Capture Mode

37.6 Register Summary

Note: Several parts of the ISI controller use the pixel clock provided by the image sensor (ISI_PCK). Thus the user must first program the image sensor to provide this clock (ISI_PCK) before programming the Image Sensor Controller.

Offset	Name	Bit Pos.									
0x00	ISI_CFG1	7:0	CRC_SYNC	EMB_SYNC	GRAYLE	PIXCLK_POL	VSYNC_POL	HSYNC_POL		
		15:8		THMASK[1:0]		FULL	DISCR	FRATE[2:0]		
		23:16	SLD[7:0]							
		31:24	SFD[7:0]							
0x04	ISI_CFG2	7:0	IM_VSIZE[7:0]							
		15:8	COL_SPACE	RGB_SWAP	GRAYSCALE	RGB_MODE	GS_MODE	IM_VSIZE[10:8]		
		23:16	IM_HSIZE[7:0]							
		31:24	RGB_CFG[1:0]		YCC_SWAP[1:0]			IM_HSIZE[10:8]		
0x08	ISI_PSIZE	7:0	PREV_VSIZE[7:0]							
		15:8							PREV_VSIZE[9:8]	
		23:16	PREV_HSIZE[7:0]							
		31:24							PREV_HSIZE[9:8]	
0x0C	ISI_PDECF	7:0	DEC_FACTOR[7:0]							
		15:8								
		23:16								
		31:24								
0x10	ISI_Y2R_SET0	7:0	C0[7:0]							
		15:8	C1[7:0]							
		23:16	C2[7:0]							
		31:24	C3[7:0]							
0x14	ISI_Y2R_SET1	7:0	C4[7:0]							
		15:8		Cboff	Croff	Yoff				C4[8:8]
		23:16								
		31:24								
0x18	ISI_R2Y_SET0	7:0		C0[6:0]						
		15:8		C1[6:0]						
		23:16		C2[6:0]						
		31:24								Roff
0x1C	ISI_R2Y_SET1	7:0		C3[6:0]						
		15:8		C4[6:0]						
		23:16		C5[6:0]						
		31:24								Goff
0x20	ISI_R2Y_SET2	7:0		C6[6:0]						
		15:8		C7[6:0]						
		23:16		C8[6:0]						
		31:24								Boff
0x24	ISI_CR	7:0						ISI_SRST	ISI_DIS	ISI_EN
		15:8								ISI_CDC
		23:16								
		31:24								

Value	Description
0	Codec channel fetch operation is disabled.
1	Codec channel fetch operation is enabled.

38.8.53 GMAC Multiple Collision Frames Register

Name: GMAC_MCF
Offset: 0x13C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							MCOL[17:16]	
Access							R	R
Reset							0	0

Bit	15	14	13	12	11	10	9	8
	MCOL[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	MCOL[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 17:0 – MCOL[17:0] Multiple Collision
This register counts the number of frames experiencing between two and fifteen collisions prior to being successfully transmitted, i.e., no underrun and not too many retries.

38.8.113 GMAC Screening Type 2 EtherType Register x

Name: GMAC_ST2ERx
Offset: 0x06E0 + x*0x04 [x=0..3]
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	COMPVAL[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COMPVAL[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – COMPVAL[15:0] EtherType Compare Value
When the bit GMAC_ST2RPQ.ETHE is written to '1', the EtherType (last EtherType in the header if the frame is VLAN tagged) is compared with bits [15:0] in the register designated by GMAC_ST2RPQ.I2ETH.

42.7.2 QSPI Mode Register

Name: QSPI_MR
Offset: 0x04
Reset: 0x00000000
Property: Read/Write

This register can only be written if bit WPEN is cleared in the QSPI Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	DLYCS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DLYBCT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
					NBBITS[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
			CSMODE[1:0]			WDRBT	LLB	SMM
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bits 31:24 – DLYCS[7:0] Minimum Inactive QCS Delay
This field defines the minimum delay between the deactivation and the activation of QCS. The DLYCS time guarantees the slave minimum deselect time.

If DLYCS written to ‘0’, one peripheral clock period is inserted by default.

Otherwise, the following equation determines the delay:

DLYCS = Minimum inactive × $f_{peripheral\ clock}$

Bits 23:16 – DLYBCT[7:0] Delay Between Consecutive Transfers
This field defines the delay between two consecutive transfers with the same peripheral without removing the chip select. The delay is always inserted after each transfer and before removing the chip select if needed.

When DLYBCT is written to ‘0’, no delay between consecutive transfers is inserted and the clock keeps its duty cycle over the character transfers. In Serial Memory mode (SMM = 1), DLYBCT must be written to ‘0’ and no delay is inserted.

Otherwise, the following equation determines the delay:

DLYBCT = (Delay Between Consecutive Transfers × $f_{peripheral\ clock}$) / 32

45.8.5 I2SC Status Set Register

Name: I2SC_SSR
Offset: 0x10
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
			TXURCH[1:0]					
Access			W	W				
Reset			–	–				

Bit	15	14	13	12	11	10	9	8
							RXORCH[1:0]	
Access							W	W
Reset							–	–

Bit	7	6	5	4	3	2	1	0
		TXUR				RXOR		
Access		W				W		
Reset		–				–		

Bits 21:20 – TXURCH[1:0] Transmit Underrun Per Channel Status Set
Writing a ’0’ has no effect.

Writing a ’1’ to any bit in this field sets the corresponding bit in I2SC_SR and the corresponding interrupt request.

Bits 9:8 – RXORCH[1:0] Receive Overrun Per Channel Status Set
Writing a ’0’ has no effect.

Writing a ’1’ to any bit in this field sets the corresponding bit in I2SC_SR and the corresponding interrupt request.

Bit 6 – TXUR Transmit Underrun Status Set
Writing a ’0’ to this bit has no effect.

Writing a ’1’ to this bit sets the status bit.

Bit 2 – RXOR Receive Overrun Status Set
Writing a ’0’ to this bit has no effect.

Writing a ’1’ to this bit sets the status bit.

Offset	Name	Bit Pos.								
		15:8	CD[15:8]							
		23:16						FP[2:0]		
		31:24								
0x24	US_RTOR	7:0	TO[7:0]							
		15:8	TO[15:8]							
		23:16								TO[16:16]
		31:24								
0x28	US_TTGR	7:0	TG[7:0]							
		15:8								
		23:16								
		31:24								
0x28	US_TTGR (LON_MODE)	7:0	PCYCLE[7:0]							
		15:8	PCYCLE[15:8]							
		23:16	PCYCLE[23:16]							
		31:24								
0x2C ... 0x3F	Reserved									
0x40	US_FIDI	7:0	FI_DI_RATIO[7:0]							
		15:8	FI_DI_RATIO[15:8]							
		23:16								
		31:24								
0x40	US_FIDI (LON_MODE)	7:0	BETA2[7:0]							
		15:8	BETA2[15:8]							
		23:16	BETA2[23:16]							
		31:24								
0x44	US_NER	7:0	NB_ERRORS[7:0]							
		15:8								
		23:16								
		31:24								
0x48 ... 0x4B	Reserved									
0x4C	US_IF	7:0	IRDA_FILTER[7:0]							
		15:8								
		23:16								
		31:24								
0x50	US_MAN	7:0					TX_PL[3:0]			
		15:8				TX_MPOL			TX_PP[1:0]	
		23:16					RX_PL[3:0]			
		31:24	RXIDLEV	DRIFT	ONE	RX_MPOL			RX_PP[1:0]	
0x54	US_LINMR	7:0	WKUPTYP	FSDIS	DLM	CHKTYP	CHKDIS	PARDIS	NACT[1:0]	
		15:8	DLC[7:0]							
		23:16							SYNCDIS	PDCM
		31:24								
0x58	US_LINIR	7:0	IDCHR[7:0]							

46.7.43 USART LON IDT Tx Register

Name: US_IDTTX
Offset: 0x0080
Reset: 0x0
Property: Read/Write

This register is relevant only if USART_MODE = 0x9 in the USART Mode Register.

This register can only be written if the WPEN bit is cleared in the USART Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	IDTTX[23:16]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	IDTTX[15:8]							
Access								
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	IDTTX[7:0]							
Access								
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – IDTTX[23:0] LON Indeterminate Time after Transmission (comm_type = 1 mode only)

Value	Description
0–16777215	LON indeterminate time after transmission in t_{bit}.

47.6.5 UART Interrupt Mask Register

Name: UART_IMR
Offset: 0x10
Reset: 0x00000000
Property: Read-only

The following configuration values are valid for all listed bit names of this register:

0: The corresponding interrupt is disabled.

1: The corresponding interrupt is enabled.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	CMP						TXEMPTY	
Access	R						R	
Reset	0						0	

Bit	7	6	5	4	3	2	1	0
	PARE	FRAME	OVRE				TXRDY	RXRDY
Access	R	R	R				R	R
Reset	0	0	0				0	0

Bit 15 – CMP Mask Comparison Interrupt

Bit 9 – TXEMPTY Mask TXEMPTY Interrupt

Bit 7 – PARE Mask Parity Error Interrupt

Bit 6 – FRAME Mask Framing Error Interrupt

Bit 5 – OVRE Mask Overrun Error Interrupt

Bit 1 – TXRDY Disable TXRDY Interrupt

Bit 0 – RXRDY Mask RXRDY Interrupt

If conversion results are signed and resolution is less than 16 bits, the sign is extended up to the bit 15 (e.g., 0xF43 for 12-bit resolution will be read as 0xFF43 and 0x467 will be read as 0x0467).

52.6.6 Conversion Triggers

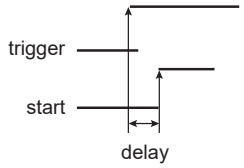
Conversions of the active analog channels are started with a software or hardware trigger. The software trigger is provided by writing a '1' to the bit START in the Control Register (AFEC_CR).

The hardware trigger can be one of the TIOA outputs of the Timer Counter channels, PWM Event line, or the external trigger input of the AFEC (ADTRG). The hardware trigger is selected with AFEC_MR.TRGSEL. The selected hardware trigger is enabled with AFEC_MR.TRGEN

The minimum time between two consecutive trigger events must be strictly greater than the duration of the longest conversion sequence according to configuration of registers AFEC_MR, AFEC_CHSR, AFEC_SEQ1R, AFEC_SEQ2R.

If a hardware trigger is selected, the start of a conversion is triggered after a delay starting at each rising edge of the selected signal. Due to asynchronous handling, the delay may vary in a range of two peripheral clock periods to one AFE clock period. This delay varies from trigger to trigger and so introduces a jitter error leading to a reduced Signal-to-Noise ratio performance.

Figure 52-6. Conversion Start with the Hardware Trigger



If one of the TIOA outputs is selected, the corresponding Timer Counter channel must be programmed in Waveform mode.

Only one start command is necessary to initiate a conversion sequence on all the channels. The AFEC hardware logic automatically performs the conversions on the active channels, then waits for a new request. The Channel Enable (AFEC_CHER) and Channel Disable (AFEC_CHDR) registers permit the analog channels to be enabled or disabled independently.

If the AFEC is used with a DMA, only the transfers of converted data from enabled channels are performed and the resulting data buffers should be interpreted accordingly.

52.6.7 Sleep Mode and Conversion Sequencer

The AFEC Sleep mode maximizes power saving by automatically deactivating the AFE when it is not being used for conversions. Sleep mode is selected by setting AFEC_MR.SLEEP.

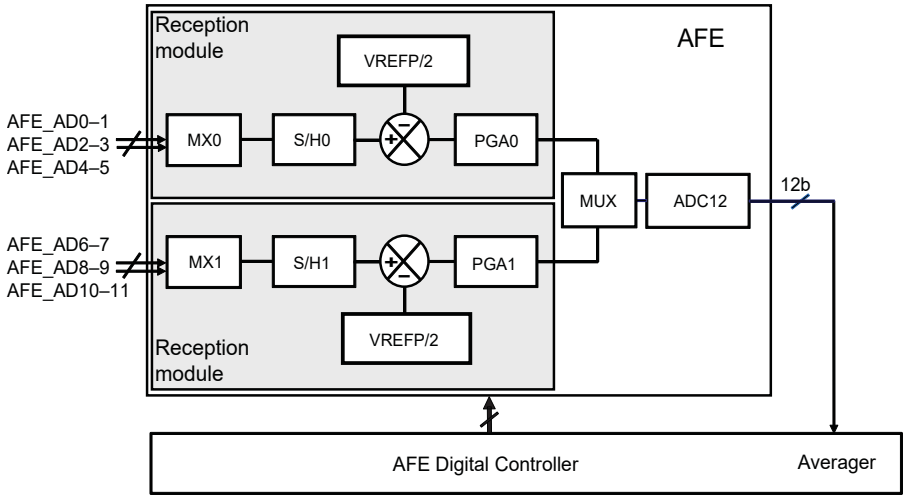
Sleep mode is managed by a conversion sequencer, which automatically processes the conversions of all channels at lowest power consumption.

This mode can be used when the minimum period of time between two successive trigger events is greater than the startup period of the AFEC. Refer to the AFE Characteristics in the section "Electrical Characteristics".

When a start conversion request occurs, the AFE is automatically activated. As the analog cell requires a startup time, the logic waits during this lapse and starts the conversion on the enabled channels. When all conversions are complete, the AFE is deactivated until the next trigger. Triggers occurring during the sequence are not taken into account.

A fast wakeup mode is available in the AFEC_MR as a compromise between power-saving strategy and responsiveness. Setting the FWUP bit enables the Fast Wakeup mode. In Fast Wakeup mode, the AFE is

Figure 59-12. Differential Mode AFE



59.8.1 AFE Power Supply

59.8.1.1 Power Supply Characteristics

Table 59-29. Power Supply Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VDDIN}	Analog Current Consumption	Sleep mode (see **Note 2**)	–	2	–	µA
		Fast wake-up mode (see **Note 3**)		0.4		mA
		Normal mode, single sampling		3.4		mA
		Normal mode, dual sampling		4.2		mA
$I_{VDDCORE}$	Digital Current Consumption	Sleep mode (see **Note 2**)	-	1	-	µA
		Normal mode		80		

Note:

1. Current consumption is measured with AFEC_ACR.IBCTL=10.
2. In Sleep mode, the AFE core, the Sample and Hold and the internal reference operational amplifer are off.
3. In Fast Wake-up mode, only the AFE core is off.

59.8.1.2 ADC Bias Current

AFEC_ACR.IBCTL controls the ADC bias current, with the nominal setting IBCTL = 10.

IBCTL = 10 is the mandatory configuration suitable for a sampling frequency of up to 1 MHz. If the sampling frequency is below 500 kHz, IBCTL = 01 can also be used to reduce the current consumption.

If the sampling frequency is more than 1 MHz, then the setting must be IBCTL=11.

Note: The default value in the register is 01 and must be modified according to the defined sampling frequency.

59.8.2 External Reference Voltage

V_{VREFP} is an external reference voltage applied on the pin VREFP. The quality of the reference voltage V_{VREFP} is critical to the performance of the AFE. A DC variation of the reference voltage V_{VREFP} is

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