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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M7
Core Size	32-Bit Single-Core
Speed	300MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, LINbus, MMC/SD/SDIO, QSPI, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	114
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsamv71q21b-cb

Offset	Name	Bit Pos.								
		23:16			FIXED_DEFMSTR[3:0]				DEFMSTR_TYPE[1:0]	
		31:24								
0x64 ... 0x7F	Reserved									
0x80	MATRIX_PRAS0	7:0			M1PR[1:0]				M0PR[1:0]	
		15:8			M3PR[1:0]				M2PR[1:0]	
		23:16			M5PR[1:0]				M4PR[1:0]	
		31:24			M7PR[1:0]				M6PR[1:0]	
0x84	MATRIX_PRBS0	7:0			M9PR[1:0]				M8PR[1:0]	
		15:8			M11PR[1:0]				M10PR[1:0]	
		23:16							M12PR[1:0]	
		31:24								
0x88	MATRIX_PRAS1	7:0			M1PR[1:0]				M0PR[1:0]	
		15:8			M3PR[1:0]				M2PR[1:0]	
		23:16			M5PR[1:0]				M4PR[1:0]	
		31:24			M7PR[1:0]				M6PR[1:0]	
0x8C	MATRIX_PRBS1	7:0			M9PR[1:0]				M8PR[1:0]	
		15:8			M11PR[1:0]				M10PR[1:0]	
		23:16							M12PR[1:0]	
		31:24								
0x90	MATRIX_PRAS2	7:0			M1PR[1:0]				M0PR[1:0]	
		15:8			M3PR[1:0]				M2PR[1:0]	
		23:16			M5PR[1:0]				M4PR[1:0]	
		31:24			M7PR[1:0]				M6PR[1:0]	
0x94	MATRIX_PRBS2	7:0			M9PR[1:0]				M8PR[1:0]	
		15:8			M11PR[1:0]				M10PR[1:0]	
		23:16							M12PR[1:0]	
		31:24								
0x98	MATRIX_PRAS3	7:0			M1PR[1:0]				M0PR[1:0]	
		15:8			M3PR[1:0]				M2PR[1:0]	
		23:16			M5PR[1:0]				M4PR[1:0]	
		31:24			M7PR[1:0]				M6PR[1:0]	
0x9C	MATRIX_PRBS3	7:0			M9PR[1:0]				M8PR[1:0]	
		15:8			M11PR[1:0]				M10PR[1:0]	
		23:16							M12PR[1:0]	
		31:24								
0xA0	MATRIX_PRAS4	7:0			M1PR[1:0]				M0PR[1:0]	
		15:8			M3PR[1:0]				M2PR[1:0]	
		23:16			M5PR[1:0]				M4PR[1:0]	
		31:24			M7PR[1:0]				M6PR[1:0]	
0xA4	MATRIX_PRBS4	7:0			M9PR[1:0]				M8PR[1:0]	
		15:8			M11PR[1:0]				M10PR[1:0]	
		23:16							M12PR[1:0]	
		31:24								
0xA8	MATRIX_PRAS5	7:0			M1PR[1:0]				M0PR[1:0]	

RSWDT_MR can be written only once. Only a processor reset resets it. Writing RSWDT_MR reloads the timer with the newly programmed mode parameters.

In normal operation, the user reloads the watchdog at regular intervals before the timer underflow occurs, by setting bit RSWDT_CR.WDRSTT. The watchdog counter is then immediately reloaded from the RSWDT_MR and restarted, and the slow clock 128 divider is reset and restarted. The RSWDT_CR is write-protected. As a result, writing RSWDT_CR without the correct hard-coded key has no effect. If an underflow does occur, the “wdt_fault” signal to the Reset Controller is asserted if RSWDT_MR.WDRSTEN is set. Moreover, WDUNF (Watchdog Underflow) is set in the Status Register (RSWDT_SR).

The status bits WDUNF and WDERR trigger an interrupt, provided the WDFIEN bit is set in the RSWDT_MR. The signal “wdt_fault” to the Reset Controller causes a Watchdog reset if the WDRSTEN bit. For details, refer to the section “Reset Controller (RSTC)”. In this case, the processor and the RSWDT are reset, and the WDUNF and WDERR flags are reset.

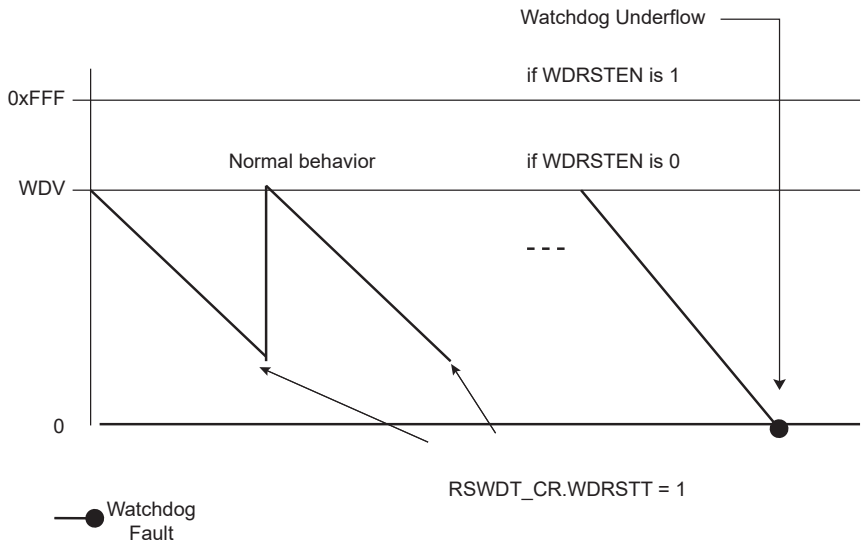
If a reset is generated, or if RSWDT_SR is read, the status bits are reset, the interrupt is cleared, and the “wdt_fault” signal to the reset controller is deasserted

Writing RSWDT_MR reloads and restarts the down counter.

The RSWDT is disabled after any power-on sequence.

While the processor is in Debug state or in Idle mode, the counter may be stopped depending on the value programmed for the WDIDLEHLT and WDDBGHLT bits in the RSWDT_MR.

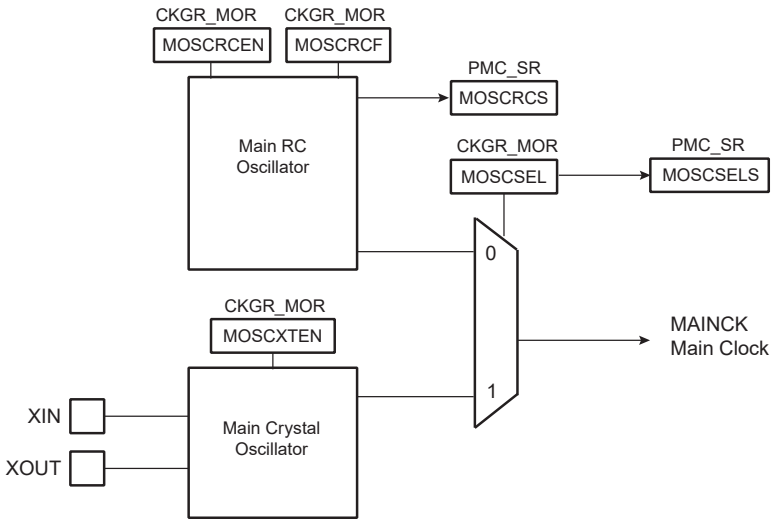
Figure 25-2. Watchdog Behavior



Related Links

26. Reset Controller (RSTC)

Figure 30-2. Main Clock (MAINCK) Block Diagram



30.5.1 Main RC Oscillator

After reset, the Main RC oscillator is enabled with the 12 MHz frequency selected. This oscillator is selected as the source of MAINCK. MAINCK is the default clock selected to start the system.

Only the 8/12 MHz RC oscillator frequencies are calibrated in production. Refer to the section “Electrical Characteristics”.

The software can disable or enable the Main RC oscillator with the MOSCRCEN bit in the Clock Generator Main Oscillator Register (CKGR_MOR).

The output frequency of the Main RC oscillator can be selected among 4, 8 or 12 MHz. Selection is done by configuring the field MOSCRCF in CKGR_MOR. When changing the frequency selection, the MOSCRCS bit in the Power Management Controller Status Register (PMC_SR) is automatically cleared and MAINCK is stopped until the oscillator is stabilized. Once the oscillator is stabilized, MAINCK restarts and PMC_SR.MOSCRCS is set. Note that enabling the Main RC oscillator (MOSCRCEN = 1) and changing its frequency (MOSCRCF) at the same time is not allowed.

This oscillator must be enabled first and its frequency changed in a second step.

When disabling the Main RC oscillator by clearing the CKGR_MOR.MOSCRCEN bit, the PMC_SR.MOSCRCS bit is automatically cleared, indicating that the oscillator is OFF.

Setting the MOSCRCS bit in the Power Management Controller Interrupt Enable Register (PMC_IER) triggers an interrupt to the processor.

Related Links

58. Electrical Characteristics for SAM V70/V71
59. Electrical Characteristics for SAM E70/S70

30.5.2 Main RC Oscillator Frequency Adjustment

The 8 MHz and 12 MHz frequencies are factory-centered to the typical values by using Flash calibration bits (refer to the “Electrical Characteristics” chapter).

The Flash calibration bits setting the Main RC oscillator frequency to 8 MHz and 12 MHz vary from device to device. To get a starting point when changing the CAL8 or CAL12 fields, it is recommended to first read their corresponding Flash calibration bits in the Flash Controller.

31.20.28 PMC SleepWalking Enable Register 0

Name: PMC_SLPWK_ER0
Offset: 0x0114
Property: Write-only

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
	PID31	PID30	PID29	PID28	PID27	PID26	PID25	PID24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	PID23	PID22	PID21	PID20	PID19	PID18	PID17	PID16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PID7							
Access								
Reset								

Bits 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – PIDx
Peripheral x SleepWalking Enable
Not all PIDs can be configured with asynchronous partial wake-up.

Only the following PID can be configured with asynchronous partial wake-up: UARTx and TWIHSx.

The clock of the peripheral must be enabled before using its asynchronous partial wake-up (SleepWalking) function (its associated PIDx field in PMC Peripheral Clock Status Register 0 or PMC Peripheral Clock Status Register 1 is set to ‘1’).

Value	Description
0	No effect.
1	The asynchronous partial wakeup (SleepWalking) function of the corresponding peripheral is enabled. **Note:** “PIDx” refers to identifiers as defined in the section “Peripheral Identifiers”

Value	Description
0	TDF optimization disabled–the number of TDF wait states is inserted before the next access begins.
1	TDF optimization enabled–the number of TDF wait states is optimized using the setup period of the next read/write access.

Bits 19:16 – TDF_CYCLES[3:0] Data Float Time
This field gives the integer number of clock cycles required by the external device to release the data after the rising edge of the read controlling signal. The SMC always provide one full cycle of bus turnaround after the TDF_CYCLES period. The external bus cannot be used by another chip select during TDF_CYCLES + 1 cycles. From 0 up to 15 TDF_CYCLES can be set.

Bit 12 – DBW Data Bus Width

Value	Name	Description
0	8_BIT	8-bit Data Bus
1	16_BIT	16-bit Data Bus

Bit 8 – BAT Byte Access Type
This field is used only if DBW defines a 16-bit data bus.

Value	Name	Description
0	BYTE_SELECT	Byte select access type: - Write operation is controlled using NCS, NWE, NBS0, NBS1. - Read operation is controlled using NCS, NRD, NBS0, NBS1.
1	BYTE_WRITE	Byte write access type: - Write operation is controlled using NCS, NWR0, NWR1. - Read operation is controlled using NCS and NRD.

Bits 5:4 – EXNW_MODE[1:0] NWAIT Mode
The NWAIT signal is used to extend the current read or write signal. It is only taken into account during the pulse phase of the read and write controlling signal. When the use of NWAIT is enabled, at least one cycle hold duration must be programmed for the read and write controlling signal.

Value	Name	Description
0	DISABLED	Disabled–The NWAIT input signal is ignored on the corresponding chip select.
1	Reserved	
2	FROZEN	Frozen Mode–If asserted, the NWAIT signal freezes the current read or write cycle. After deassertion, the read/write cycle is resumed from the point where it was stopped.
3	READY	Ready Mode–The NWAIT signal indicates the availability of the external device at the end of the pulse of the controlling read or write signal, to complete the access. If high, the access normally completes. If low, the access is extended until NWAIT returns high.

Bit 1 – WRITE_MODE Write Mode

Value	Description
0	The write operation is controlled by the NCS signal.

Offset	Name	Bit Pos.								
		23:16	COMPVAL[7:0]							
		31:24	COMPVAL[15:8]							
0x073C	GMAC_ST2CW17	7:0	OFFSSTRT[0:0]	OFFSVAL[6:0]						
		15:8								OFFSSTRT[1:1]
		23:16								
		31:24								
0x0740	GMAC_ST2CW08	7:0	MASKVAL[7:0]							
		15:8	MASKVAL[15:8]							
		23:16	COMPVAL[7:0]							
		31:24	COMPVAL[15:8]							
0x0744	GMAC_ST2CW18	7:0	OFFSSTRT[0:0]	OFFSVAL[6:0]						
		15:8								OFFSSTRT[1:1]
		23:16								
		31:24								
0x0748	GMAC_ST2CW09	7:0	MASKVAL[7:0]							
		15:8	MASKVAL[15:8]							
		23:16	COMPVAL[7:0]							
		31:24	COMPVAL[15:8]							
0x074C	GMAC_ST2CW19	7:0	OFFSSTRT[0:0]	OFFSVAL[6:0]						
		15:8								OFFSSTRT[1:1]
		23:16								
		31:24								
0x0750	GMAC_ST2CW010	7:0	MASKVAL[7:0]							
		15:8	MASKVAL[15:8]							
		23:16	COMPVAL[7:0]							
		31:24	COMPVAL[15:8]							
0x0754	GMAC_ST2CW110	7:0	OFFSSTRT[0:0]	OFFSVAL[6:0]						
		15:8								OFFSSTRT[1:1]
		23:16								
		31:24								
0x0758	GMAC_ST2CW011	7:0	MASKVAL[7:0]							
		15:8	MASKVAL[15:8]							
		23:16	COMPVAL[7:0]							
		31:24	COMPVAL[15:8]							
0x075C	GMAC_ST2CW111	7:0	OFFSSTRT[0:0]	OFFSVAL[6:0]						
		15:8								OFFSSTRT[1:1]

38.8.13 GMAC Interrupt Mask Register

Name: GMAC_IMR
Offset: 0x030
Reset: 0x07FFFFFF
Property: Read/Write

This register is a read-only register indicating which interrupts are masked. All bits are set at Reset and can be reset individually by writing to the Interrupt Enable Register (GMAC_IER), or set individually by writing to the Interrupt Disable Register (GMAC_IDR).

For test purposes there is a write-only function to this register that allows the bits in the Interrupt Status Register to be set or cleared, regardless of the state of the mask register. A write to this register directly affects the state of the corresponding bit in the Interrupt Status Register, causing an interrupt to be generated if a 1 is written.

The following values are valid for all listed bit names of this register when read:

0: The corresponding interrupt is enabled.

1: The corresponding interrupt is not enabled.

Bit	31	30	29	28	27	26	25	24
			TSUTIMCMP	WOL	RXLPISBC	SRI	PDRSFT	PDRQFT
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	1	1	1

Bit	23	22	21	20	19	18	17	16
	PDRSFR	PDRQFR	SFT	DRQFT	SFR	DRQFR		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	1	1	1	1	1	1		

Bit	15	14	13	12	11	10	9	8
	EXINT	PFTR	PTZ	PFNZ	HRESP	ROVR		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	1	1	1	1	1	1		

Bit	7	6	5	4	3	2	1	0
	TCOMP	TFC	RLEX	TUR	TXUBR	RXUBR	RCOMP	MFS
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 29 – TSUTIMCMP TSU Timer Comparison

Bit 28 – WOL Wake On LAN

Bit 27 – RXLPISBC Receive LPI indication Status Bit Change
Receive LPI indication status bit change.

Cleared on read.

Bit 26 – SRI TSU Seconds Register Increment

Offset	Name	Bit Pos.								
		23:16					PEPNUM[3:0]			
		31:24	INTFRQ[7:0]							
0x050C	USBHS_HSTPIPCFG3 (HSBOHSCP)	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16				PINGEN	PEPNUM[3:0]			
		31:24	BINTERVAL[7:0]							
0x0510	USBHS_HSTPIPCFG4	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16					PEPNUM[3:0]			
		31:24	INTFRQ[7:0]							
0x0510	USBHS_HSTPIPCFG4 (HSBOHSCP)	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16				PINGEN	PEPNUM[3:0]			
		31:24	BINTERVAL[7:0]							
0x0514	USBHS_HSTPIPCFG5	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16					PEPNUM[3:0]			
		31:24	INTFRQ[7:0]							
0x0514	USBHS_HSTPIPCFG5 (HSBOHSCP)	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16				PINGEN	PEPNUM[3:0]			
		31:24	BINTERVAL[7:0]							
0x0518	USBHS_HSTPIPCFG6	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16					PEPNUM[3:0]			
		31:24	INTFRQ[7:0]							
0x0518	USBHS_HSTPIPCFG6 (HSBOHSCP)	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16				PINGEN	PEPNUM[3:0]			
		31:24	BINTERVAL[7:0]							
0x051C	USBHS_HSTPIPCFG7	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16					PEPNUM[3:0]			
		31:24	INTFRQ[7:0]							
0x051C	USBHS_HSTPIPCFG7 (HSBOHSCP)	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16				PINGEN	PEPNUM[3:0]			
		31:24	BINTERVAL[7:0]							
0x0520	USBHS_HSTPIPCFG8	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16					PEPNUM[3:0]			
		31:24	INTFRQ[7:0]							
0x0520	USBHS_HSTPIPCFG8 (HSBOHSCP)	7:0		PSIZE[2:0]			PBK[1:0]		ALLOC	
		15:8			PTYPE[1:0]			AUTOSW	PTOKEN[1:0]	
		23:16				PINGEN	PEPNUM[3:0]			
		31:24	BINTERVAL[7:0]							

Offset	Name	Bit Pos.								
0x0538	USBHS_HSTPIPISR2 (INTPIPES)	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0538	USBHS_HSTPIPISR2 (ISOPIPES)	7:0	SHORTPACKETI	CRCERRI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x053C	USBHS_HSTPIPISR3	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	TXSTPI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x053C	USBHS_HSTPIPISR3 (INTPIPES)	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x053C	USBHS_HSTPIPISR3 (ISOPIPES)	7:0	SHORTPACKETI	CRCERRI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0540	USBHS_HSTPIPISR4	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	TXSTPI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0540	USBHS_HSTPIPISR4 (INTPIPES)	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0540	USBHS_HSTPIPISR4 (ISOPIPES)	7:0	SHORTPACKETI	CRCERRI	OVERFI	NAKEDI	PERRI	UNDERFI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						
0x0544	USBHS_HSTPIPISR5	7:0	SHORTPACKETI	RXSTALLDI	OVERFI	NAKEDI	PERRI	TXSTPI	TXOUTI	RXINI
		15:8	CURRBK[1:0]		NBUSYBK[1:0]				DTSEQ[1:0]	
		23:16	PBYCT[3:0]					CFGOK		RWALL
		31:24		PBYCT[10:4]						

Bit 5 – OVERFIEC Overflow Interrupt Disable

Bit 4 – NAKEDEC NAKed Interrupt Disable

Bit 3 – PERREC Pipe Error Interrupt Disable

Bit 2 – TXSTPEC Transmitted SETUP Interrupt Disable

Bit 1 – TXOUTEC Transmitted OUT Data Interrupt Disable

Bit 0 – RXINEC Received IN Data Interrupt Disable

39.6.62 Host Pipe x Enable Register (Isochronous Pipes)

Name: USBHS_HSTPIPIERx (ISOPIPES)
Offset: 0x05F0 + x*0x04 [x=0..9]
Reset: 0
Property: Read/Write

This register view is relevant only if PTYPE = 0x1 in "Host Pipe x Configuration Register".

For additional information, see "Host Pipe x Mask Register (Isochronous Pipes)".

This register always reads as zero.

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Sets the corresponding bit in USBHS_HSTPIPIMRx.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
						RSTDTS	PFREEZES	PDISHDMAS
Access								
Reset						0	0	0

Bit	15	14	13	12	11	10	9	8
				NBUSYBKES				
Access								
Reset				0				

Bit	7	6	5	4	3	2	1	0
	SHORTPACKETIES	CRCERRES	OVERFIES	NAKEDES	PERRES	UNDERFIES	TXOUTES	RXINES
Access								
Reset	0	0	0	0	0	0	0	0

Bit 18 – RSTDTS Reset Data Toggle Enable

Bit 17 – PFREEZES Pipe Freeze Enable

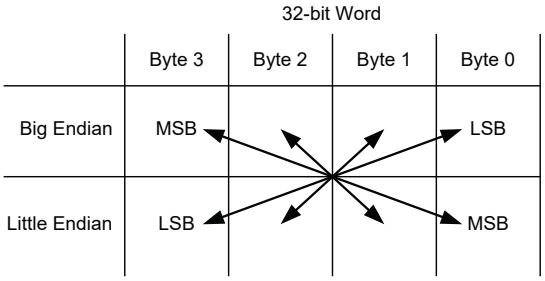
Bit 16 – PDISHDMAS Pipe Interrupts Disable HDMA Request Enable

Bit 12 – NBUSYBKES Number of Busy Banks Enable

Bit 7 – SHORTPACKETIES Short Packet Interrupt Enable

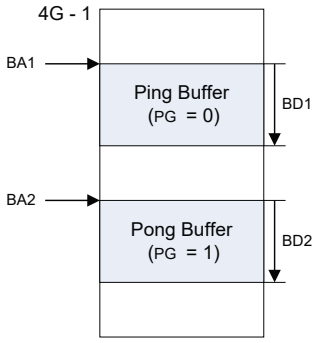
Bit 6 – CRCERRES CRC Error Interrupt Enable

Figure 48-20. Endianness Overview



The following figure shows an example of the ping-pong system memory structure. This system memory structure is similar for all channel types and shows the relationship between the BAn, BDn, and PG descriptor fields.

Figure 48-21. Ping-Pong System Memory Structure



Each ADT entry holds a 32-bit BAn field which defines the start of each ping or pong buffer within system memory. The BDn field is used to indicate the size for the respective ping or pong page. The maximum size is 2k-entries for asynchronous and control channels; 8k-entries for isochronous and synchronous channels.

AHB Synchronous Channel Descriptors

Table 48-21 shows the format for a synchronous ADT entry. The field definitions are defined in Table 48-22. Each synchronous channel buffer can be up to 8k-bytes deep.

Table 48-21. Synchronous ADT Entry Format

Bit Offset	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CE	LE	PG	Reserved												
16	Reserved															
32	RDY1	DNE1	ERR1	BD1[12:0]												
48	RDY2	DNE2	ERR2	BD2[12:0]												
64	BA1[15:0]															
80	BA1[31:16]															
96	BA2[15:0]															
112	BA2[31:16]															

AHB Isochronous Channel Descriptors

49.6.26 MCAN New Data 2

Name: MCAN_NDAT2
Offset: 0x9C
Reset: 0x00000000
Property: Read/Write

Bit	31	30	29	28	27	26	25	24
	ND63	ND62	ND61	ND60	ND59	ND58	ND57	ND56
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	ND55	ND54	ND53	ND52	ND51	ND50	ND49	ND48
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	ND47	ND46	ND45	ND44	ND43	ND42	ND41	ND40
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ND39	ND38	ND37	ND36	ND35	ND34	ND33	ND32
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 – NDx New Data
The register holds the New Data flags of Receive Buffers 32 to 63. The flags are set when the respective Receive Buffer has been updated from a received frame. The flags remain set until the processor clears them. A flag is cleared by writing a ‘1’ to the corresponding bit position. Writing a ‘0’ has no effect. A hard reset will clear the register.

Value	Description
0	Receive Buffer not updated.
1	Receive Buffer updated from new message.

49.6.27 MCAN Receive FIFO 0 Configuration

Name: MCAN_RXF0C
Offset: 0xA0
Reset: 0x00000000
Property: Read/Write

This register can only be written if the bits CCE and INIT are set in MCAN CC Control Register.

Bit	31	30	29	28	27	26	25	24
	F0OM	F0WM[6:0]						
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
		F0S[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	F0SA[13:6]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	F0SA[5:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit 31 – F0OM FIFO 0 Operation Mode
FIFO 0 can be operated in Blocking or in Overwrite mode (see Rx FIFOs).

Value	Description
0	FIFO 0 Blocking mode.
1	FIFO 0 Overwrite mode.

Bits 30:24 – F0WM[6:0] Receive FIFO 0 Watermark

Value	Description
0	Watermark interrupt disabled.
1-64	Level for Receive FIFO 0 watermark interrupt (MCAN_IR.RF0W).
>64	Watermark interrupt disabled.

Bits 22:16 – F0S[6:0] Receive FIFO 0 Size
The Receive FIFO 0 elements are indexed from 0 to F0S-1.

Value	Description
0	No Receive FIFO 0
1-64	Number of Receive FIFO 0 elements.
>64	Values greater than 64 are interpreted as 64.

53.7.2 DACC Mode Register

Name: DACC_MR
Offset: 0x04
Reset: 0x00000000
Property: Read/Write

This register can only be written if the WPEN bit is cleared in the DACC Write Protection Mode Register.

Bit	31	30	29	28	27	26	25	24
					PRESCALER[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DIFF							
Access	R/W							
Reset	0							

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
			ZERO	WORD			MAXS1	MAXS0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 27:24 – PRESCALER[3:0] Peripheral Clock to DAC Clock Ratio
This field defines the division ratio between the peripheral clock and the DAC clock as per the following formula:

$$\text{PRESCALER} = \left(\frac{f_{\text{peripheral clock}}}{f_{\text{DAC}}}\right) - 2$$

Bit 23 – DIFF Differential Mode

Value	Name	Description
0	DISABLED	DAC0 and DAC1 are single-ended outputs.
1	ENABLED	DACP and DACN are differential outputs. The differential level is configured by the channel 0 value.

Bit 5 – ZERO Must always be written to 0.

Bit 4 – WORD Word Transfer Mode

55.6.2 ICM Control Register

Name: ICM_CTRL
Offset: 0x04
Reset: –
Property: Write-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RMEN[3:0]				RMDIS[3:0]			
Access	W	W	W	W	W	W	W	W
Reset	0	0	0	–	0	0	0	–

Bit	7	6	5	4	3	2	1	0
	REHASH[3:0]					SWRST	DISABLE	ENABLE
Access	W	W	W	W		W	W	W
Reset	0	0	0	–		–	–	–

Bits 15:12 – RMEN[3:0] Region Monitoring Enable
Monitoring is activated by default.

Value	Description
0	No effect
1	When bit RMEN[i] is set to one, the monitoring of region with identifier i is activated.

Bits 11:8 – RMDIS[3:0] Region Monitoring Disable

Value	Description
0	No effect
1	When bit RMDIS[i] is set to one, the monitoring of region with identifier i is disabled.

Bits 7:4 – REHASH[3:0] Recompute Internal Hash

Value	Description
0	No effect
1	When REHASH[i] is set to one, Region i digest is re-computed. This bit is only available when region monitoring is disabled.

Bit 2 – SWRST Software Reset

55.6.3 ICM Status Register

Name: ICM_SR
Offset: 0x08
Reset: –
Property: Read-only

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	RMDIS[3:0]				RAWRMDIS[3:0]			
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	–	0	0	0	–

Bit	7	6	5	4	3	2	1	0
								ENABLE
Access								R
Reset								–

Bits 15:12 – RMDIS[3:0] Region Monitoring Disabled Status

Value	Description
0	Region i is being monitored (occurs after integrity check value has been calculated and written to Hash area).
1	Region i monitoring is not being monitored.

Bits 11:8 – RAWRMDIS[3:0] Region Monitoring Disabled Raw Status

Value	Description
0	Region i monitoring has been activated by writing a 1 in RMEN[i] of ICM_CTRL.
1	Region i monitoring has been deactivated by writing a 1 in RMDIS[i] of ICM_CTRL.

Bit 0 – ENABLE ICM Enable Register

Value	Description
0	ICM is disabled.
1	ICM is activated.

Symbol	Parameter	Conditions	Min	Max	Unit
		3.3V domain	2.0		
SPI_8	MOSI Hold time after SCK rises	1.8V domain 3.3V domain	0.4 0.2	–	ns
SPI_9	SCK rising to MISO	1.8V domain 3.3V domain	3.5 3.0	16.2 13.5	ns
SPI_{10}	MOSI Setup time before SCK falls	1.8V domain 3.3V domain	2.2 2.1	–	ns
SPI_{11}	MOSI Hold time after SCK falls	1.8V domain 3.3V domain	0.6 0.4	–	ns
SPI_{12}	NPCS0 setup to SCK rising	1.8V domain 3.3V domain	1.6 0.6	–	ns
SPI_{13}	NPCS0 hold after SCK falling	1.8V domain 3.3V domain	1.1 0.6	–	ns
SPI_{14}	NPCS0 setup to SCK falling	1.8V domain 3.3V domain	1.3 0.6	–	ns
SPI_{15}	NPCS0 hold after SCK rising	1.8V domain 3.3V domain	0.9 0.7	–	ns

Timings are given in the 3.3V domain, with VDDIO from 2.85V to 3.6V, maximum external capacitor = 40 pF.

Table 59-67. USART SPI Timings

Symbol	Parameter	Conditions	Min	Max	Unit
Master Mode					
SPI_0	SCK Period	1.7V domain 3.3V domain	MCK/6 MCK/6	– –	ns
SPI_1	Input Data Setup Time	1.7V domain 3.3V domain	2.8 2.5	– –	ns
SPI_2	Input Data Hold Time	1.7V domain 3.3V domain	0.5 0.2	– –	ns
SPI_3	Chip Select Active to Serial Clock	1.7V domain 3.3V domain	-1.1 -0.9	– –	ns
SPI_4	Output Data Setup Time	1.7V domain 3.3V domain	-1.9 -1.9	10.9 10.4	ns

Date	Changes
	AFEC_TEMPCWR. Section 52.7.2 ”AFEC Mode Register”: updated TRACKTIM description.
	Section 53. ”Digital-to-Analog Converter Controller (DACC)” Table 53-1 “DACC Signal Description” : corrected pin names to VREFP and VREFN (were ADVREFP and ADVREFN).
	Section 54. ”Analog Comparator Controller (ACC)” Table 54-1 “ACC Signal Description” : modified Description for DAC0, DAC1 signals. Section 54.7.7 ”ACC Analog Control Register”: updated HYST definition.
	Section 57. ”Advanced Encryption Standard (AES)” Section 57.2 ”Embedded Characteristics”: replaced “12/14/16 Clock Cycles Encryption/Decryption Processing Time...” with “10/12/14 Clock Cycles Encryption/Decryption Inherent Processing Time...”.
	Section 58. ”Electrical Characteristics” Table 58-3 “DC Characteristics” : removed Note 2 on current injection. Table 58-4 “DC Characteristics” : voltage input level defined for the RST and TEST I/O types. Updated max values for IIL and IIH. Updated Table 58-15 “Typical Current Consumption in Wait Mode” . Table 58-30 “VREFP Electrical Characteristics” : updated V_{VREFP} parameter values. Added new Table 58-34 “AFE INL and DNL, fAFE Clock =<20 MHz max, IBCTL=10” and Table 58-35 “AFE INL and DNL, fAFE Clock >20 MHz to 40 MHz, IBCTL=11” . Inserted new Table 58-36 “AFE Offset and Gain Error, VVREFP = 1.7V to 3.3V” . Updated Table 58-40 “DAC Static Performances (1)” . Updated Table 58-46 “Static Performance Characteristics” Added Section 58.13.1.10: “USART in Asynchronous Mode”.
	Section 62. ”Ordering Information” Added Note (2) on availability.
	Section 63. ”Errata” Added: - Section 63.1.16 ”Universal Synchronous Asynchronous Receiver Transmitter (USART)”: “Bad frame detection issue” - Section 63.2.4 ”ARM Cortex-M7”: “All issues related to the ARM r1p1 core are described on the ARM site” - Section 63.2.6 ”Inter-IC Sound Controller (I2SC)”: “I2SC first sent data corrupted” - Section 63.2.12 ”Universal Synchronous Asynchronous Receiver Transmitter (USART)”: “Bad frame detection issue” Deleted:

Date	Changes
	Section 18.12.10 “Write Protection Status Register”: in WPVS bit description, replaced two instances of “since the last read of the MATRIX_WPSR” with “since the last write of the MATRIX_WPMR”.
	Section 21. “Enhanced Embedded Flash Controller (EEFC)” Section 21.4.3.2 “Write Commands”: added information on DMA write accesses.
	Section 30. “Power Management Controller (PMC)” Section 30.9 “Asynchronous Partial Wake-up”: inserted new sub-section “Asynchronous Partial Wake-up in Wait Mode (SleepWalking)” to better describe SleepWalking. Section 30.10 “Free-Running Processor Clock”: removed reference to MCK.
	Section 31. “Parallel Input/Output Controller (PIO)” Section 31.2 “Embedded Characteristics”: added bullet on Programmable I/O Drive. Added Section 31.5.12 “Programmable I/O Drive”. Section 31.5.15.4 “Programming Sequence”: “With DMA”: in fifth step, replaced reference to BTCx with ‘DMA status flag to indicate that the buffer transfer is complete’ Table 31-5 “Register Mapping”: added PIO_DRIVER register at offset 0x0118 and added Section 31.6.49 “PIO I/O Drive Register”.
	Section 35. “DMA Controller (XDMAC)” Added Section 35.3 “DMA Controller Peripheral Connections”.
	Section 37. “USB High-Speed Interface (USBHS)” Table 37-1 “Description of USB Pipes/Endpoints“; corrected data in columns ‘DMA’ and ‘High Bandwidth’. Modified signal names to HSDM/DM and HSDP/DP in Figure 37-1 “USBHS Block Diagram” and Table 37-2 “Signal Description”. Updated descriptions. Removed Section 37.3.1 “Application Block Diagram” and Figures 37-2, 37-3 and 37-4. Removed Section 37.4.1 “I/O Lines”. Modified Section 37.5.3.3 “Device Detection”. Section 37.6.2 “General Status Register”, Section 37.6.3 “General Status Clear Register”, Section 37.6.4 “General Status Set Register”: removed bit VBUSRQ and bit description. Bit 9 now reserved in these registers.
24-Feb-15	Section 38. “Ethernet MAC (GMAC)” Section 38.8.13 “GMAC Interrupt Mask Register”: corrected general bit description (swapped definitions provided for 0: and 1:)
	Section 40. “Quad SPI Interface (QSPI)” Section 40.5.4 “Direct Memory Access Controller (DMA)”: added Note on 32-bit aligned DMA write accesses. Figure 40-9 “Instruction Transmission Flow Diagram”: modified text if TFRTYP = 0