Analog Devices Inc./Maxim Integrated - MAX32652GWE+T Datasheet

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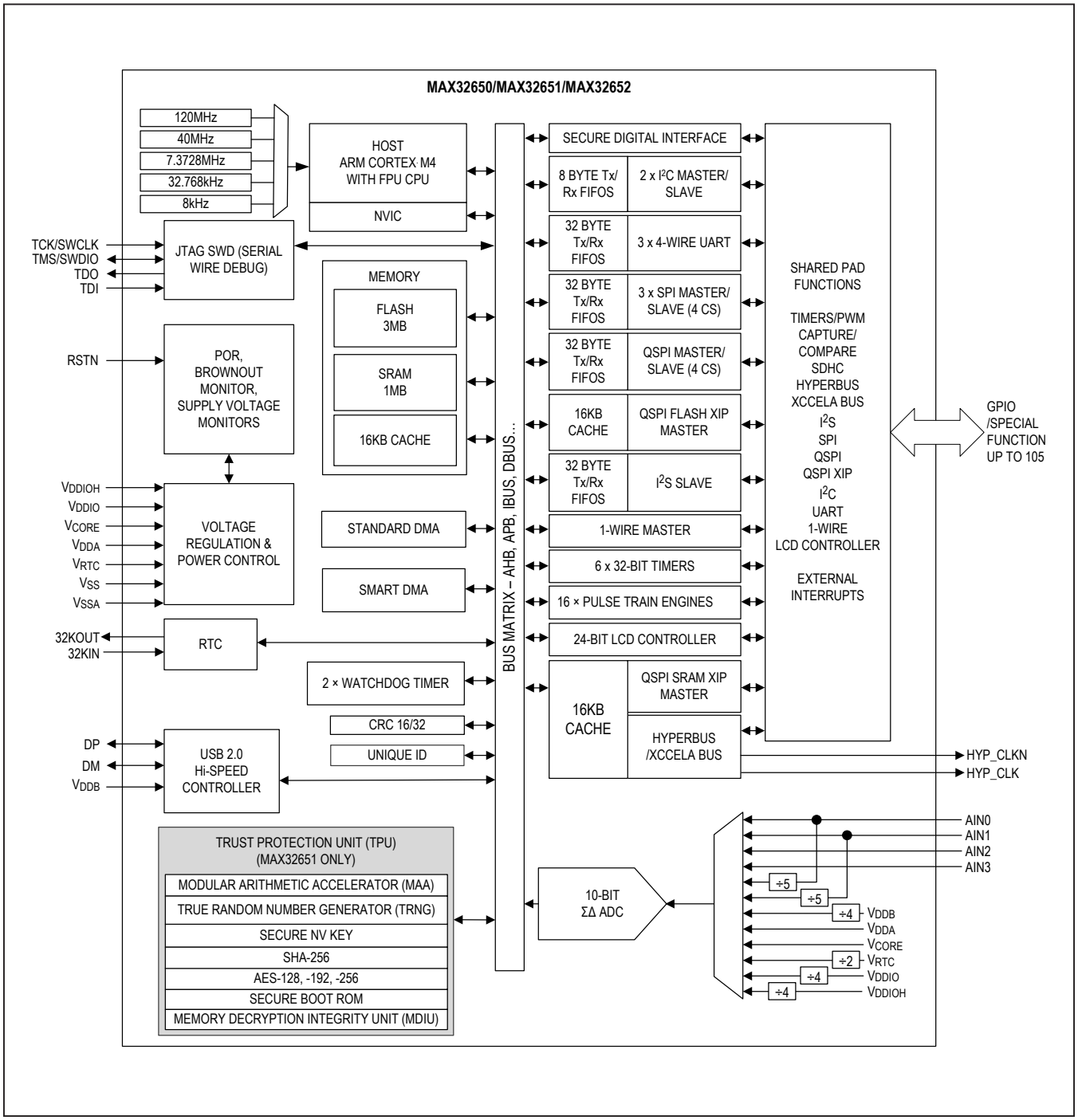
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	1-Wire, EBI/EMI, I²C, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	105
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	0.99V ~ 3.6V
Data Converters	A/D 4x10b Sigma-Delta
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	140-WFBGA, WLBGA
Supplier Device Package	140-WLP (4.47x4.43)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/max32652gwe-t

Simplified Block Diagram



Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General Purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKS						
System Clock Frequency	f_{SYS_CLK}		0.256		120,000	kHz
System Clock Period	t_{SYS_CLK}			$1/f_{SYS\_CLK}$		ns
High-Speed Oscillator Frequency	f_{HSCLK}	Measured at +25°C, 120MHz		120 ±1		MHz
Low-Power Oscillator Frequency	f_{LPCLK}			40		MHz
7MHz Oscillator Frequency	f_{7MCLK}			7.3728		MHz
Nano-Ring Oscillator Frequency	f_{NANO}			8		KHz
RTC Input Frequency	f_{32KIN}	32kHz watch crystal, C_L = 6pF, ESR < 70kΩ		32.768		kHz
RTC Operating Current	I_{RTC_ACTSLP}	Sleep or Active mode		0.39		µA
RTC Power Up Time	t_{RTC_ON}			250		ms
GENERAL-PURPOSE I/O						
Input Low Voltage for All GPIO	V_{IL_VDDIO}	V_{DDIO} selected as I/O supply			0.3 × V_{DDIO}	V
Input Low Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{IL_VDDIOH}	V_{DDIOH} selected as I/O supply			0.3 × V_{DDIOH}	V
Input Low Voltage for RSTN	V_{IL_RSTN}				0.3 × V_{DDIO}	V
Input High Voltage for All GPIO	V_{IH_VDDIO}	V_{DDIO} selected as I/O supply	0.75 × V_{DDIO}			V
Input High Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{IH_VDDIOH}	V_{DDIOH} selected as I/O supply	0.75 × V_{DDIOH}			V
Input High Voltage for RSTN	V_{IH_RSTN}		0.75 x V_{DDIO}			V
Output Low Voltage for All GPIO	V_{OL_VDDIO}	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 11, I_{OL} = 8mA		0.2	0.4	

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{OL_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 11, I_{OL} = 8mA		0.2	0.4	
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				48	mA
Output High Voltage for All GPIO	V_{OH_VDDIO}	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 00, I_{OL} = -1mA	V_{DDIO} - 0.4			V
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 01, I_{OL} = -2mA	V_{DDIO} - 0.4			
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 10, I_{OL} = -4mA	V_{DDIO} - 0.4			
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 00, I_{OL} = -8mA	V_{DDIO} - 0.4			
Output High Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{OH_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 00, I_{OL} = -1mA	V_{DDIOH} - 0.4			V
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 01, I_{OL} = -2mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 10, I_{OL} = -8mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 11, I_{OL} = -8mA	V_{DDIOH} - 0.4			
Combined I_{OH}, All GPIO	I_{OH_TOTAL}				-48	mA
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input Leakage Current Low	I_{IL}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 0V, internal pullup disabled	-1000		+1000	nA
Input Leakage Current High	I_{IH}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 3.6V, internal pulldown disabled	-1000		+1000	nA
	I_{OFF}	V_{DDIO} = 0V, V_{DDIOH} = 0V, V_{DDIO} selected as I/O supply, V_{IN} < 1.89V	-1		+1	µA
	I_{IH3V}	V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, V_{IN} = 3.6V	-2		+2	
Input Pullup Resistor TMS, TCK, TDI	R_{PU_T}			25		kΩ
Input Pullup Resistor RSTN	R_{PU_R}			1		MΩ

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AIN0/AIN1 Resistor Divider Error		ADC_CHSEL = 4 or 5, not including ADC offset/ gain error.		±2		LSb
Full-Scale Voltage	V_{FS}	ADC code = 0x3FF		1.2		V
Bandgap Temperature Coefficient	V_{TEMPCO}	From +25ºC to +105ºC		15		ppm

Electrical Characteristics—SPI

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MASTER MODE						
SPI Master Operating Frequency	f_{MCK}	$f_{MCK(MAX)} = f_{SYS\_CLK}/2$			60	MHz
SPI Master SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns
SLAVE MODE						
SPI Slave Operating Frequency	f_{SCK}				48	MHz
SPI Slave SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		µs

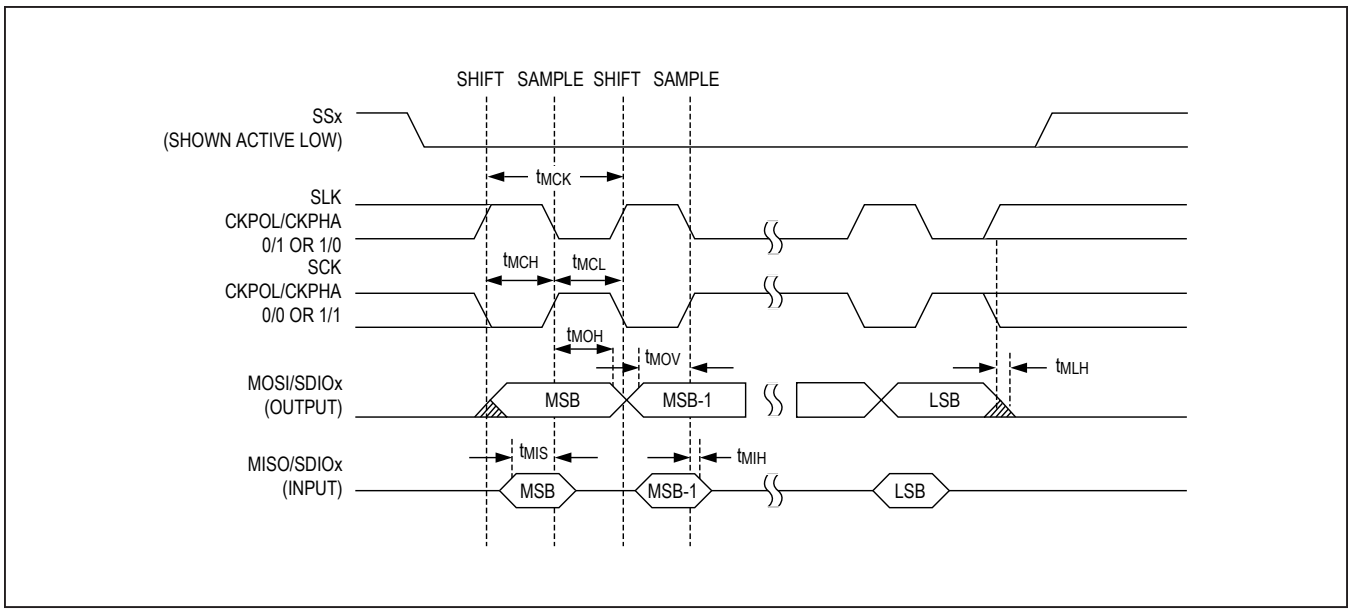


Figure 1. SPI Master Mode Timing Diagram

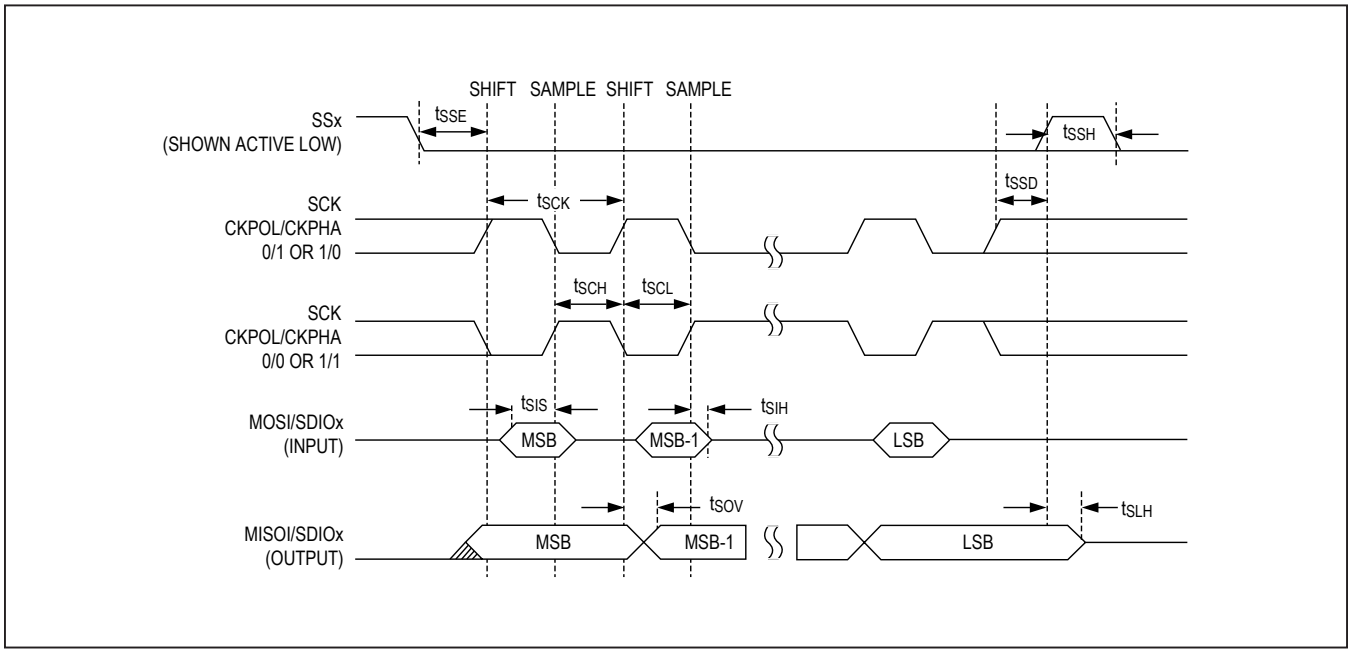


Figure 2. SPI Slave Mode Timing Diagram

Electrical Characteristics—SD/SDIO/SDHC/MMC

(T_A = -40°C to +105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency in Data Transfer Mode	f_{SDHC_CLK}		0		$f_{HSCLK}/2$	MHz
Clock Period	t_{CLK}			$1/f_{SDHC\_CLK}$		ns
Clock Low Time	t_{WCL}			7		ns
Clock High Time	t_{WCH}			7		
Input Setup Time	t_{ISU}			5		ns
Input Hold Time	t_{IHLD}			1		ns
Output Valid Time	t_{OVLD}			5		ns
Output Hold Time	t_{OHLD}			6		ns

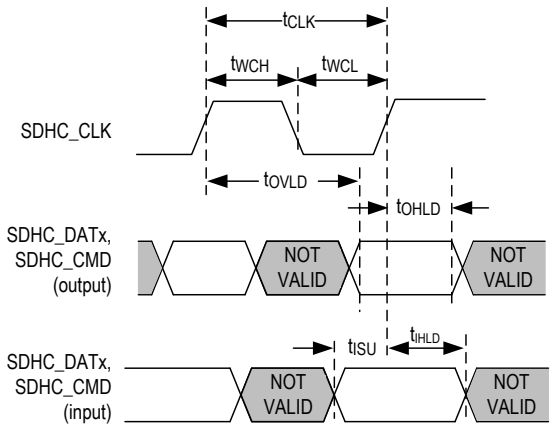


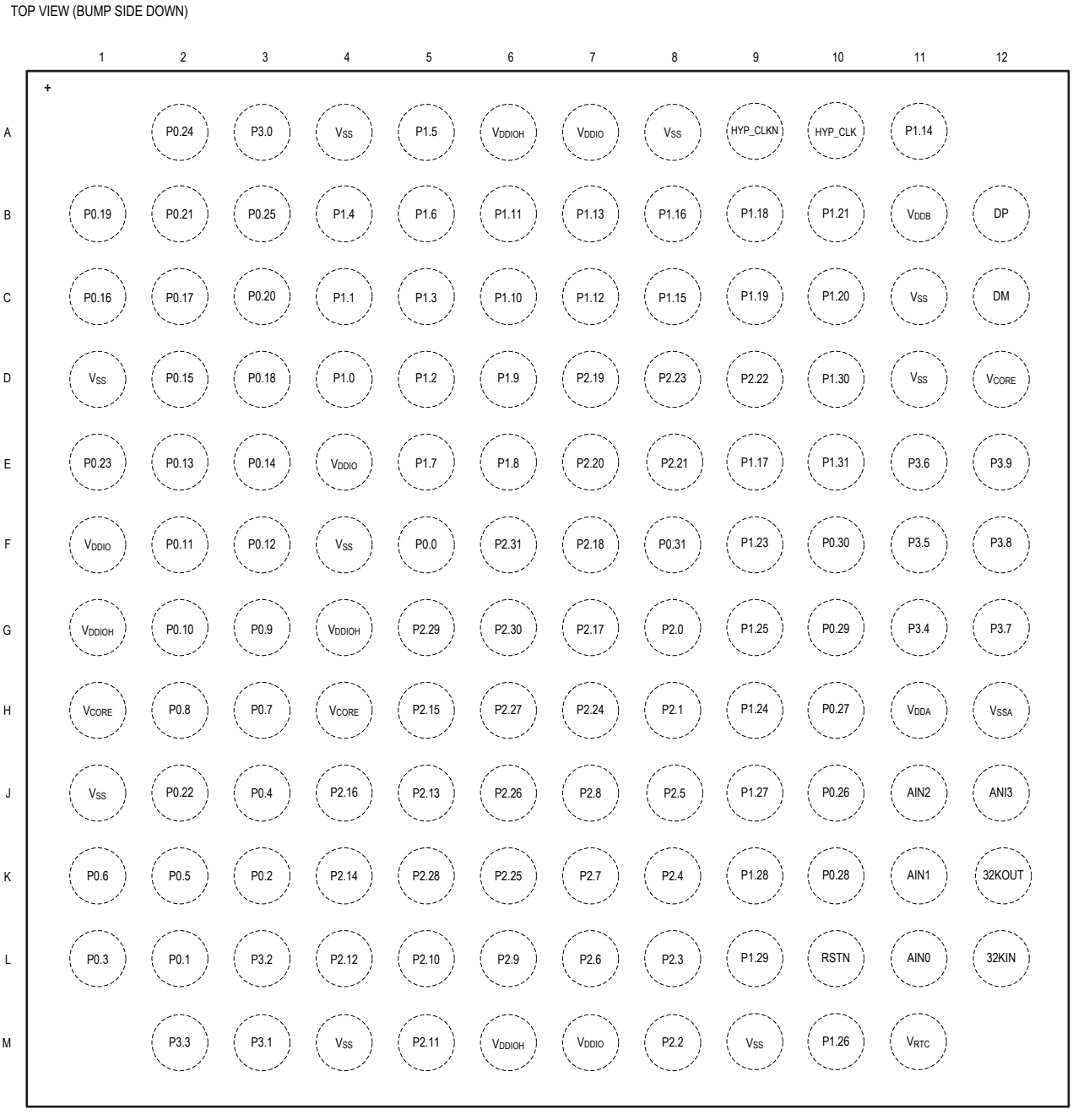
Figure 5. SD/SDIO/SDHC/MMC Timing Diagram

Electrical Characteristics—One Wire Master

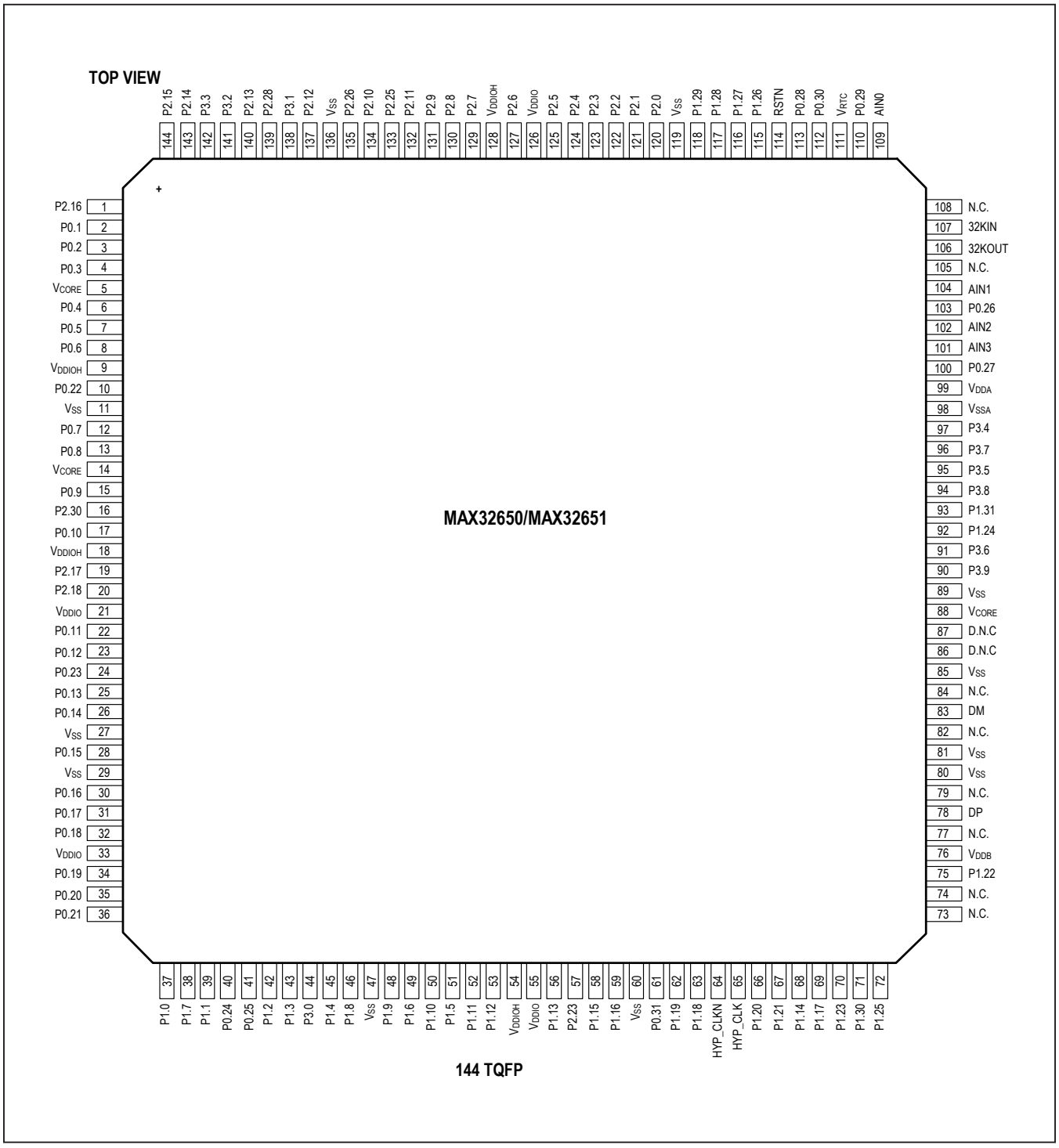
(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write 0 Low Time	t_{W0L}	Standard		60		µs
		Overdrive		8		
Write 1 Low Time	t_{W1L}	Standard		6		µs
		Standard, Long Line mode		8		
		Overdrive		1		
Presence Detect Sample	t_{MSP}	Standard		70		µs
		Standard, Long Line mode		85		
		Overdrive		9		
Read Data Value	t_{MSR}	Standard		15		µs
		Standard, Long Line mode		24		
		Overdrive		3		
Recovery Time	t_{REC0}	Standard		10		µs
		Standard, Long Line mode		20		
		Overdrive		4		
Reset Time High	t_{RSTH}	Standard		480		µs
		Overdrive		58		
Reset Time Low	t_{RSTL}	Standard		600		µs
		Overdrive		70		
Time Slot	t_{SLOT}	Standard		70		µs
		Overdrive		12		

Pin Configurations



Pin Configurations (continued)



Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
C2	E3	31	P0.17	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D3	D2	32	P0.18	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B1	F4	34	P0.19	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C3	A2	35	P0.20	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B2	C2	36	P0.21	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
J2	G5	10	P0.22	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E1	—	24	P0.23	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
A2	—	40	P0.24	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B3	—	41	P0.25	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
J10	F7	103	P0.26	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H10	F8	100	P0.27	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
K10	G6	113	P0.28	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G10	F6	110	P0.29	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F10	G7	112	P0.30	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F8	—	61	P0.31	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
D4	B2	37	P1.0	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C4	D3	39	P1.1	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D5	C3	42	P1.2	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C5	E4	43	P1.3	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B4	C4	45	P1.4	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
A5	D4	51	P1.5	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B5	B4	49	P1.6	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E5	—	38	P1.7	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E6	A3	46	P1.8	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D6	B3	48	P1.9	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C6	A4	50	P1.10	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B6	F5	52	P1.11	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C7	E5	53	P1.12	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B7	K2	56	P1.13	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
A11	A9	68	P1.14	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
C8	C5	58	P1.15	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B8	D5	59	P1.16	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E9	—	69	P1.17	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4and Table 5 GPIO and Alternate Function Matrix tables for details.
B9	B7	63	P1.18	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C9	C6	62	P1.19	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C10	E6	66	P1.20	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B10	B8	67	P1.21	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
—	—	75	P1.22	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F9	C7	70	P1.23	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H9	E7	92	P1.24	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G9	D6	72	P1.25	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
M10	J8	115	P1.26	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
J9	H7	116	P1.27	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
K9	J7	117	P1.28	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and TTable 5 GPIO and Alternate Function Matrix tables for details.
L9	H6	118	P1.29	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
J5	G3	140	P2.13	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
K4	J1	143	P2.14	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H5	H1	144	P2.15	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
J4	G2	1	P2.16	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G7	F2	19	P2.17	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F7	H5	20	P2.18	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D7	—	—	P2.19	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E7	—	—	P2.20	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E8	—	—	P2.21	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D9	—	—	P2.22	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D8	A6	57	P2.23	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H7	—	—	P2.24	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
K6	—	133	P2.25	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
J6	—	135	P2.26	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H6	—	—	P2.27	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
K5	—	139	P2.28	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G5	—	—	P2.29	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G6	—	16	P2.30	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F6	—	—	P2.31	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
A3	—	44	P3.0	General-Purpose I/O, Port 3. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
M3	—	138	P3.1	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
L3	—	141	P3.2	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
M2	—	142	P3.3	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G11	F9	97	P3.4	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F11	E9	95	P3.5	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E11	D9	91	P3.6	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G12	F10	96	P3.7	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F12	E10	94	P3.8	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E12	D10	90	P3.9	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.

Memory

Internal Flash Memory

3MB of internal flash memory provides nonvolatile storage of program and data memory.

Flash can be expanded through the SPIXF flash serial interface backed by 16KB of cache. The SPIXF flash interface can address an additional 128MB.

Internal SRAM

The internal 1MB SRAM provides low-power retention of application information in all power modes except shutdown. The SRAM can be divided into granular banks that create a flexible SRAM retention architecture. This data retention feature is optional and configurable. This granularity allows the application to minimize its power consumption by only retaining the most essential data.

SRAM can be expanded through the SPIXR SRAM serial interface backed by 16KB of cache. The SPIXR SRAM interface can address an additional 512MB.

Secure Digital Interface

The secure digital interface (SDI) provides high-speed, high-density data storage capability for media files and large long-term data logs. This interface supports eMMC, SD, SDHC, and SDXC memory devices up to 4GB at transfer rates up to 30MB/s. The 7-pin interface (4 data, 1 clock, 1 command, 1 write-protect) supports the following specifications:

- SD Host Controller Standard Specification Version 3.00
- SDIO Card Specification Version 3.0
- SD Memory Card Specification Version 3.01
- SD Memory Card Security Specification Version 1.01
- MMC Specification Version 4.51

Spansion HyperBus/Xccela Bus

The Spansion HyperBus/Xccela bus interface provides access to external Cypress Spansion HyperBus and Xccela bus memory products both SRAM and/or flash. This interface provides a means of high-speed execution from external SRAM or flash allowing system expansion when internal memory resources are insufficient. Up to 8MB SRAM or 512MB flash at a speed of up to 60MHz or 120MBps is supported. It is a high-speed low-pin count interface that is memory-mapped into the CPU memory space making access to this external memory as easy as accessing on-chip RAM. Data is transferred over a high-speed, 8-bit bus. Slave memory devices are selected with two chip selects. HyperBus transfers are clocked using a differential clock while Xccela bus transfers use a single-ended clock. This interface supports 1.8V operation only.

Features of the HyperBus/Xccela bus interface include:

- Master/slave system
- 120MBps maximum data transfer rate
- Double data rate (DDR): two data transfers per clock cycle
- Transparent bus operation to the processor
- 16KB write-through cache
- Two chip selects for two memory ports
  - Each port supports memories up to 512MB
- Addresses two external memories, one at a time
- Interfaces to HyperFlash, HyperRAM, and Xccela PSRAM
- Zero wait state burst mode operation
- Low-power Half Sleep mode
  - Puts the external memory device into low power mode while retaining memory contents
- Configurable timing parameters

Clocking Scheme

The high-frequency oscillator operates at a maximum frequency of 120MHz.

Optionally, 4 other oscillators can be selected depending upon power needs:

- 40MHz low-power oscillator
- 8kHz nano-ring oscillator
- 32.768kHz oscillator (external crystal required)
- 7.3728MHz oscillator

This clock is the primary clock source for the digital logic and peripherals. Select the 7.3728MHz internal oscillator to optimize active power consumption. Using the 7.3727MHz oscillator allows UART communications to meet a ±2% baud rate tolerance.

Wakeup is possible from either the 7.3728MHz internal oscillator or the high-frequency oscillator. The device exits power-on reset using the the 40MHz oscillator.

An external 32.768kHz timebase is required when using the RTC.

General-Purpose I/O and Special Function Pins

Most general-purpose I/O (GPIO) pins share both a firmware-controlled I/O function and one or more special function signals associated with peripheral modules. Pins can be individually enabled for GPIO or peripheral special function use. Configuring a pin as a special function usually supersedes its use as a firmware-controlled I/O. Though this multiplexing between peripheral and GPIO functions is usually static, it can also be done dynamically. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where explicitly noted in the electrical characteristics tables.

In GPIO mode, pins are logically divided into ports of 32 pins. Each pin of a port has an interrupt function that can be independently enabled, and configured as a level- or edge-sensitive interrupt. All GPIOs of a given port share the same interrupt vector. Some packages do not have all of the GPIOs available.

When configured as GPIO, the following features are provided. The features can be independently enabled or disabled on a per-pin basis.

- Configurable as input, output, bidirectional, or high impedance
- Optional internal pullup resistor or internal pulldown resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

The MAX32650/MAX32651/MAX32652 provides up to 105 GPIO (140 WLP), 97 GPIO (144 TQFP), and 67 GPIO (96 WLP).

GPIOs, which have any HyperBus alternate functionality (P1.[21:18], P1.[16:11], P3.0), can only be used with the V_{DDIO} supply, whether used as a GPIO or any alternate function.

Standard DMA Controller

The standard DMA (direct memory access) controller provides a means to off-load the CPU for memory/peripheral data transfer leading to a more power-efficient system. It allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The following transfer modes are supported:

- 16 channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

SmartDMA Controller

The SmartDMA controller provides low-power memory/peripheral access control that can run data collection tasks and perform complex background processing on data being transferred, from simple arithmetic to multiply/accumulate, while the CPU is off, significantly reducing power consumption (Background mode). The SmartDMA controller allows peripherals on the AHB to access main system memory (SRAM) independent of the CPU. It is configured through the APB and can configure itself through the AHB-to-APB bridge. The SmartDMA engine runs code from system SRAM. If desired, custom SmartDMA algorithms supporting data post-processing can be developed by the user.

Key features:

- Dedicated 32-bit controller with general-purpose timer
- APB read access to the SmartDMA registers
- Configurable start IP address
- Selects 32 interrupts from peripherals from a total of 80 available interrupts to initiate DMA operations
- Global enable (SDMA_EN) keeps SmartDMA in reset except APB interface
- Synchronous interrupt output to CPU

Analog-to-Digital Converter

The 10-bit delta-sigma ADC provides an integrated reference generator and a single-ended input multiplexer. The multiplexer selects an input channel from either the external analog input signals (AIN0, AIN1, AIN2, and AIN3) or the internal power supply inputs. AIN0 and AIN1 are 5V tolerant, making them suitable for monitoring batteries. An internal 1.22V bandgap or the V_{DDA} analog supply can be chosen as the ADC reference.

An optional feature allows samples captured by the ADC to be automatically compared against user-programmable high and low limits. Up to four channel limit pairs can be configured in this way. The comparison allows the ADC to trigger an interrupt (and potentially wake the CPU from a low-power sleep mode) when a captured sample goes outside the preprogrammed limit range. Since this comparison is performed directly by the sample limit monitors, it can be performed even while the main CPU is suspended in a low power mode.

Real-Time Clock

A real-time clock (RTC) keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software.

The RTC provides a time-of-day alarm that can be programmed to any future value between 1 second and 12 days. When configured for long intervals, the time-of-day alarm can be used as a power-saving timer, allowing the device to remain in an extremely low-power mode but still awaken periodically to perform assigned tasks. A second independent 32-bit 1/256 subsecond alarm can be programmed between 244µs and 256 seconds. Both can be configured as recurring alarms. When enabled, either alarm can cause an interrupt or wake the device from most low power modes.

The time base is generated by a 32.768kHz crystal or an external clock source that must meet the electrical/timing requirements in the *Electrical Characteristics* table.

The RTC calibration feature provides the ability for user software to compensate for minor variations in the RTC oscillator, crystal, temperature, and board layout. Enabling the 32KCAL alternate function outputs a timing signal derived from the RTC. External hardware can measure the frequency and adjust the RTC frequency in increments of ±127ppm with 1ppm resolution. Under most circumstances, the oscillator does not require any calibration.

CRC Module

A cyclic redundancy check (CRC) hardware module provides fast calculations and data integrity checks by application software. The CRC module supports the following polynomials:

- CRC-16-CCITT
- CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$)

Programmable Timers

32-Bit Timer/Counter/PWM (TMR)

General-purpose, 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals with minimal software interaction. Each of the 32-bit timers can also be split into two 16-bit timers.

The timer provides the following features:

- 32-bit up/down autoreload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating or capture
- Timer output pin
- Configurable as 2 × 16-bit general-purpose timers
- Timer interrupt

The MAX32650–MAX32652 provides six instances of the general-purpose 32-bit timer (TMR0–TMR5).

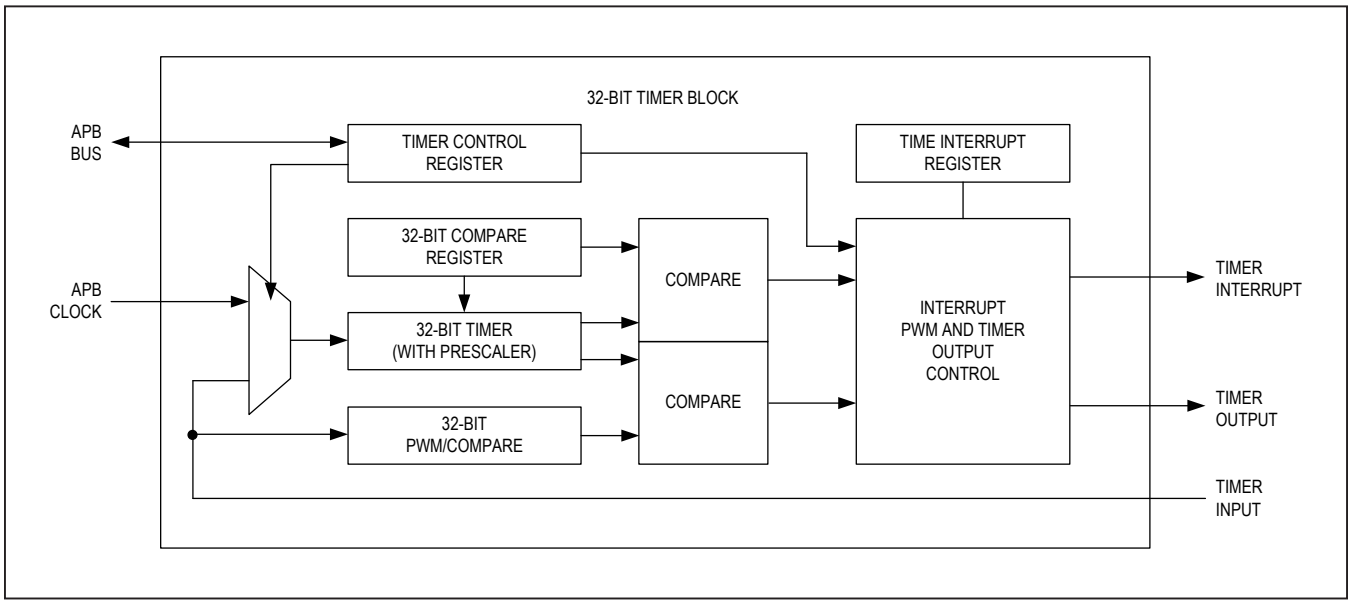


Figure 9. 32-Bit Timer

MAA

The provided high-speed, hardware-based modulo arithmetic accelerator (MAA) performs mathematical computations that support strong cryptographic algorithms. These include:

- 2048-bit DSA
- 4096-bit RSA
- Elliptic curve public key infrastructure

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

The AES keys are automatically generated by the engine and stored in dedicated flash to protect against tampering. Key generation and storage is transparent to the user.

SHA-256

SHA-256 is a cryptographic hash function part of the SHA-2 family of algorithms. It authenticates user data and verifies its integrity. It is used for digital signatures.

The device provides a hardware SHA-256 engine for fast computation of 256-bit digests.

Memory Decryption Integrity Unit

The external SPI flash can optionally be encrypted for additional security. Data can be transparently encrypted when it is loaded and decrypted on-the-fly. Encryption keys are stored in the always-on domain and preserved as long as V_{RTC} is present.

Secure Bootloader

The secure bootloader provides a secure, authenticated communication channel with a system host. The secure communication protocol (SCP) allows the programming of internal and external memory.

The secure bootloader provides the following features:

- Life cycle management
- Authentications using ECDSA P-256, with 256-bit ECC key pairs and SHA-256 secure hash function
- Preprogrammed Maxim manufacturer root key (MRK)
- Programmable customer root key (CRK)
- Support for 2048- or 4096-bit RSA digital signature

Additional Documentation and Technical Support

Designers must have the following documents to use all the features of this device:

- This data sheet, which contains electrical/timing specifications, package information, and pin descriptions
- The corresponding revision-specific errata sheet
- The corresponding user guide, which contains detailed information and programming guidelines for core features and peripherals

Applications Information

GPIO and Alternate Function Matrix, 140 WLP

Table 3. GPIO and Alternate Function Matrix, 140 WLP

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P0.0	PT3	SPIXF_SDIO2**
P0.1	SPIXR_SDIO0**	—
P0.2	SPIXR_SDIO2**	—
P0.3	SPIXR_SCK**	—
P0.4	SPIXR_SDIO3**	—
P0.5	SPIXR_SDIO1**	—
P0.6	SPIXR_SS0**	—
P0.7	SPIXF_SS0**	—
P0.8	SPIXF_SCK**	—
P0.9	SPIXF_SDIO1**	—
P0.10	SPIXF_SDIO0**	—
P0.11	SPIXF_SDIO2**	—
P0.12	SPIXF_SDIO3**	—
P0.13	SPI3_SS1	CLCD_G0
P0.14	SPI3_SS2	CLCD_G1
P0.15	SPI3_SDIO3	CLCD_G2
P0.16	SPI3_SCK	CLCD_G3
P0.17	SPI3_SDIO2	CLCD_G4
P0.18	SPI3_SS3	CLCD_G5
P0.19	SPI3_SS0	CLCD_G6
P0.20	SPI3_SDIO1	CLCD_G7
P0.21	SPI3_SDIO0	—
P0.22	SPI0_SS0	CLCD_VDEN
P0.23	PT15	CLCD_CLK

GPIO and Alternate Function Matrix, 144 TQFP

Table 5. GPIO and Alternate Function Matrix, 144 TQFP

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P0.0*	—	—
P0.1	SPIXR_SDIO0**	—
P0.2	SPIXR_SDIO2**	—
P0.3	SPIXR_SCK**	—
P0.4	SPIXR_SDIO3**	—
P0.5	SPIXR_SDIO1**	—
P0.6	SPIXR_SS0**	—
P0.7	SPIXF_SS0**	—
P0.8	SPIXF_SCK**	—
P0.9	SPIXF_SDIO1**	—
P0.10	SPIXF_SDIO0**	—
P0.11	SPIXF_SDIO2**	—
P0.12	SPIXF_SDIO3**	—
P0.13	SPI3_SS1	CLCD_G0
P0.14	SPI3_SS2	CLCD_G1
P0.15	SPI3_SDIO3	CLCD_G2
P0.16	SPI3_SCK	CLCD_G3
P0.17	SPI3_SDIO2	CLCD_G4
P0.18	SPI3_SS3	CLCD_G5
P0.19	SPI3_SS0	CLCD_G6
P0.20	SPI3_SDIO1	CLCD_G7
P0.21	SPI3_SDIO0	—
P0.22	SPI0_SS0	CLCD_VDEN
P0.23	PT15	CLCD_CLK
P0.24	RXEV	CLCD_HSYNC
P0.25	TXEV	CLCD_B0
P0.26	TDI	—
P0.27	TDO	—
P0.28	TMS (SWDIO)†††	—
P0.29	TCK (SWDCLK)†††	—
P0.30	—	CLCD_B0
P0.31	32KCAL	SDHC_CDN
P1.0	SDHC_CMD	SPIXF_SDIO3**
P1.1	SDHC_DAT2	SPIXF_SDIO1**

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P1.2	SDHC_WP	SPIXF_SS0**
P1.3	SDHC_DAT3	CLCD_CLK
P1.4	SDHC_DAT0	SPIXF_SDIO0**
P1.5	SDHC_CLK	SPIXF_SCK**
P1.6	SDHC_DAT1	PT0
P1.7	UART2_CTS	PT1
P1.8	UART2_RTS	PT2
P1.9	UART2_RX	PT3
P1.10	UART2_TX	PT4
P1.11	HYP_CS0N	SPIXR_SDIO0**
P1.12	HYP_D0	SPIXR_SDIO1**
P1.13	HYP_D4	SPIXR_SS0**
P1.14	HYP_RWDS	PT5
P1.15	HYP_D1	SPIXR_SDIO2**
P1.16	HYP_D5	SPIXR_SCK**
P1.17	PT9	—
P1.18	HYP_D6	PT6
P1.19	HYP_D2	PT7
P1.20	HYP_D3	CLCD_HSYNC
P1.21	HYP_D7	PT8
P1.22	—	—
P1.23	SPI1_SS0	CLCD_B1
P1.24	SPI1_SS2	CLCD_B2
P1.25	SPI1_SS1	CLCD_B3
P1.26	SPI1_SCK	CLCD_B4
P1.27	SPI1_SS3	CLCD_B5
P1.28	SPI1_MISO	CLCD_B6
P1.29	SPI1_MOSI	CLCD_B7
P1.30	OWM_PUPEN	CLCD_R0
P1.31	OWM_IO	CLCD_R1
P2.0	SPI2_SS2	PT9
P2.1	SPI2_SS1	PT10
P2.2	SPI2_SCK (I2S-BCLK)†	CLCD_LEND

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/17	Initial release	—
1	3/18	Updated *General Description* and *Benefits and Features* sections	1

