Analog Devices Inc./Maxim Integrated - MAX32652GWE+ Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	1-Wire, EBI/EMI, I²C, QSPI, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	105
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1M x 8
Voltage - Supply (Vcc/Vdd)	0.99V ~ 3.6V
Data Converters	A/D 4x10b Sigma-Delta
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	140-WFBGA, WLBGA
Supplier Device Package	140-WLP (4.47x4.43)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/max32652gwe

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General Purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER						
Supply Voltage, Core	V_{CORE}	f_{SYS_CLK} = 120MHz	0.99	1.1	1.21	V
Supply Voltage, Analog	V_{DDA}		1.71	1.8	1.89	V
Supply Voltage, RTC	V_{RTC}		1.71	1.8	1.89	V
Supply Voltage, GPIO	V_{DDIO}		1.71	1.8	1.89	V
Supply Voltage, GPIO (High)	V_{DDIOH}		1.71	1.8	3.6	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{CORE}		0.835		V
		Monitors V_{DDA}		1.67		
		Monitors V_{RTC}		1.67		
		Monitors V_{DDIO}		1.67		
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DDB}		2.95		V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DDIOH}		1.67		V
Power-On Reset Voltage	V_{POR}	Monitors V_{CORE}		0.594		V
		Monitors V_{DDA}		1.52		
		Monitors V_{RTC}		1.17		
RAM Data Retention Voltage	V_{DRV}			0.81		V
V_{CORE} Dynamic Current, Active Mode	I_{CORE_DACT}	Total current into V_{CORE} pins, f_{SYS_CLK} = 120MHz, V_{CORE} = 1.1V, CPU in Active mode, executing from cache, inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA		95		µA/MHz
V_{CORE} Fixed Current, Active Mode	I_{CORE_FACT}	120MHz oscillator enabled, total current into V_{CORE} pins, CPU in Active mode 0MHz execution, inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA		1020		µA
		7.3728MHz oscillator enabled, total current into V_{CORE} pins, CPU in Active mode 0MHz execution, inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA		356		
V_{DDA} Fixed Current, Active Mode	I_{DDA_FACT}	120MHz oscillator enabled, total current into V_{DDA} pins, CPU in Active mode 0MHz execution, inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA , V_{CORE} and V_{DDA} voltage monitors enabled		348		µA
		7.3728MHz oscillator enabled, total current into V_{DDA} pins, CPU in Active mode 0MHz execution, inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}, outputs source/sink 0mA , V_{CORE} and V_{DDA} voltage monitors enabled		39		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
USB						
USB Supply Voltage	V_{DDB}		3.0	3.3	3.6	V
D+, D- Pin Capacitance	C_{IN_USB}	Pin to V_{SS}		8		pF
Driver Output Resistance	R_{DRV}	Steady state drive		45 ±10%		Ω
USB/FULL SPEED						
Single-Ended Input High Voltage (DP, DM)	V_{IH_USB}		2.0			V
Single-Ended Input Low Voltage (DP, DM)	V_{IL_USB}				0.6	V
Output High Voltage (DP, DM)	V_{OH_USB}	R_L = 1.5 kΩ from DP and DM to V_{SS}, I_{OH} = -4mA	V_{DDB} - 0.4		V_{DDB}	V
Output Low Voltage (DP, DM)	V_{OL_USB}	R_L = 1.5 kΩ from DP to V_{DDB}, I_{OL} = 4mA	V_{SS}		0.4	V
Differential Input Sensitivity	V_{DI}	|DP to DM|	0.2			V
Common Mode Voltage Range	V_{CM}	Includes V_{DI} range	0.8		2.5	V
Transition Time (Rise/Fall) D+, D- (Note 11)	t_{RF}	C_L = 50pF	4		20	ns
Pullup Resistor on Upstream Ports	R_{PU}		1.05	1.5	1.95	kΩ
USB/HI-SPEED						
Hi-Speed Data Signaling Common-Mode Voltage Range	V_{HSCM}		-50		+500	mV
Hi-Speed Squelch Detection Threshold	V_{HSSQ}	Squelch detected		100		mV
		No squelch detected		200		
Hi-Speed Idle Level Output Voltage	V_{HSOI}		-10		+10	mV
Hi-Speed Low Level Output Voltage	V_{HSOL}		-10		+10	mV
Hi-Speed High Level Output Voltage	V_{HSOH}			400 ± 40		mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}			900 ±200		mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}			-700 ±200		mV

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General Purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKS						
System Clock Frequency	f_{SYS_CLK}		0.256		120,000	kHz
System Clock Period	t_{SYS_CLK}			$1/f_{SYS\_CLK}$		ns
High-Speed Oscillator Frequency	f_{HSCLK}	Measured at +25°C, 120MHz		120 ±1		MHz
Low-Power Oscillator Frequency	f_{LPCLK}			40		MHz
7MHz Oscillator Frequency	f_{7MCLK}			7.3728		MHz
Nano-Ring Oscillator Frequency	f_{NANO}			8		KHz
RTC Input Frequency	f_{32KIN}	32kHz watch crystal, C_L = 6pF, ESR < 70kΩ		32.768		kHz
RTC Operating Current	I_{RTC_ACTSLP}	Sleep or Active mode		0.39		µA
RTC Power Up Time	t_{RTC_ON}			250		ms
GENERAL-PURPOSE I/O						
Input Low Voltage for All GPIO	V_{IL_VDDIO}	V_{DDIO} selected as I/O supply			0.3 × V_{DDIO}	V
Input Low Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{IL_VDDIOH}	V_{DDIOH} selected as I/O supply			0.3 × V_{DDIOH}	V
Input Low Voltage for RSTN	V_{IL_RSTN}				0.3 × V_{DDIO}	V
Input High Voltage for All GPIO	V_{IH_VDDIO}	V_{DDIO} selected as I/O supply	0.75 × V_{DDIO}			V
Input High Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{IH_VDDIOH}	V_{DDIOH} selected as I/O supply	0.75 × V_{DDIOH}			V
Input High Voltage for RSTN	V_{IH_RSTN}		0.75 x V_{DDIO}			V
Output Low Voltage for All GPIO	V_{OL_VDDIO}	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 11, I_{OL} = 8mA		0.2	0.4	

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Low Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{OL_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 11, I_{OL} = 8mA		0.2	0.4	
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				48	mA
Output High Voltage for All GPIO	V_{OH_VDDIO}	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 00, I_{OL} = -1mA	V_{DDIO} - 0.4			V
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 01, I_{OL} = -2mA	V_{DDIO} - 0.4			
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 10, I_{OL} = -4mA	V_{DDIO} - 0.4			
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 00, I_{OL} = -8mA	V_{DDIO} - 0.4			
Output High Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{OH_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 00, I_{OL} = -1mA	V_{DDIOH} - 0.4			V
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 01, I_{OL} = -2mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 10, I_{OL} = -8mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 11, I_{OL} = -8mA	V_{DDIOH} - 0.4			
Combined I_{OH}, All GPIO	I_{OH_TOTAL}				-48	mA
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input Leakage Current Low	I_{IL}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 0V, internal pullup disabled	-1000		+1000	nA
Input Leakage Current High	I_{IH}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 3.6V, internal pulldown disabled	-1000		+1000	nA
	I_{OFF}	V_{DDIO} = 0V, V_{DDIOH} = 0V, V_{DDIO} selected as I/O supply, V_{IN} < 1.89V	-1		+1	µA
	I_{IH3V}	V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, V_{IN} = 3.6V	-2		+2	
Input Pullup Resistor TMS, TCK, TDI	R_{PU_T}			25		kΩ
Input Pullup Resistor RSTN	R_{PU_R}			1		MΩ

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FAST MODE PLUS						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		80		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Low Period SCL Clock	t_{LOW}		0.5			µs
High Time SCL clock	t_{HIGH}		0.26			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			µs
Data Setup Time	$t_{SU;DAT}$			50		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			50		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			µs
Data Valid Time	$t_{VD;DAT}$		0.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.45			µs

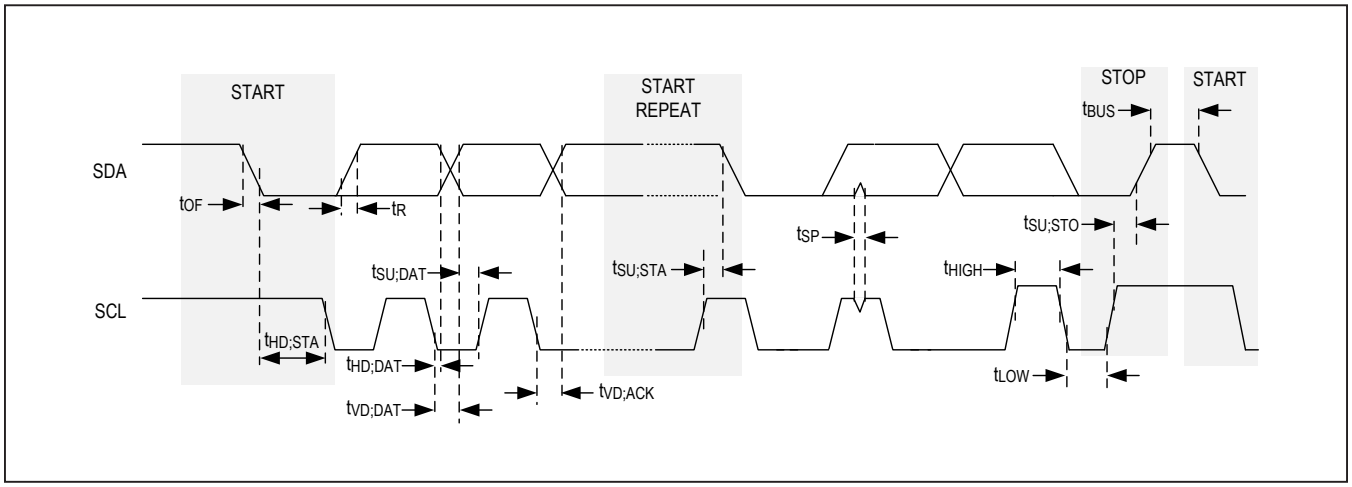


Figure 3. I²C Timing Diagram

Electrical Characteristics—I²C Slave

(Timing specifications are guaranteed by design and not production tested, T_A = -40°C to +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bit Clock Frequency	f_{BCLK}	96kHz LRCLK frequency			3.072	MHz
BCLK High Time	t_{WBCLKH}			0.5		$1/f_{BCLK}$
BCLK Low Time				0.5		$1/f_{BCLK}$
LRCLK Setup Time	t_{LRCLK_BLCK}			25		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDO}			12		ns
Setup Time for SD (Input)	t_{SU_SDI}			6		ns
Hold Time SD (Input)	t_{HD_SDI}			3		ns

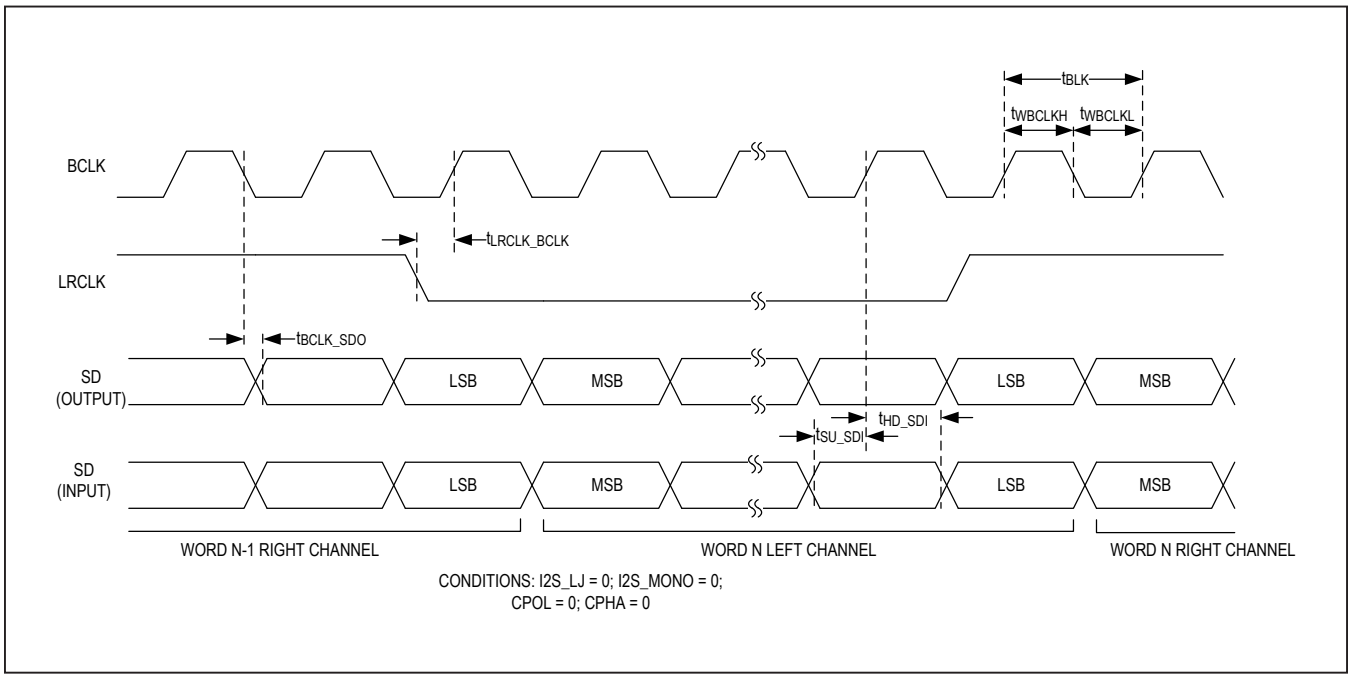


Figure 4. I²S Timing Diagram

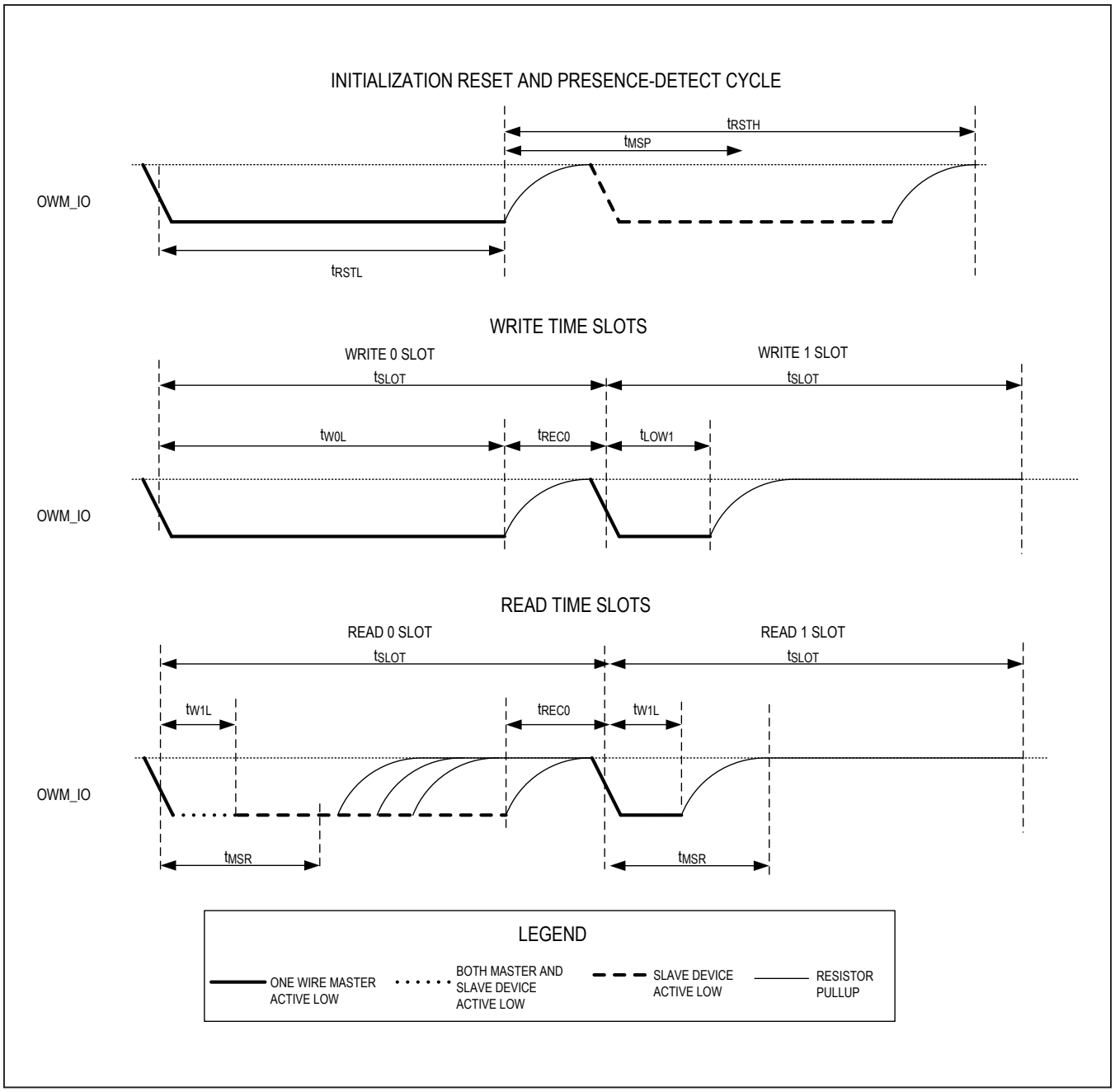


Figure 7. One-Wire Master Data Timing Diagram

Pin Description

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
POWER				
H1, H4, D12	G1, C8	5, 14, 88	V_{CORE}	Core Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
H11	G10	99	V_{DDA}	1.8V Analog Supply Voltage. This pin must be bypassed to V_{SSA} with 1.0µF and 0.01µF capacitors as close as possible to the package.
B11	B9	76	V_{DDB}	USB Transceiver Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
A7	A5	21	V_{DDIO}	GPIO Supply Voltage. This pin must be bypassed to V_{SS} with 1.0µF and 0.01µF capacitors as close as possible to the package.
E4, F1	B1, K5	33, 55		GPIO Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF and a 0.01µF capacitor as close as possible to the package.
M7	—	126		GPIO Supply Voltage. This pin must be bypassed to V_{SS} with 1.0µF and 0.01µF capacitors as close as possible to the package.
A6	B5	9	V_{DDIOH}	GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. This pin must be bypassed to V_{SS} with 1.0µF and 0.01µF capacitorx as close as possible to the package.
G1, G4, M6	F1, K4	18, 54, 128		GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. This pin must be bypassed to V_{SS} with 1.0µF and 0.01µF capacitors as close as possible to the package.
M11	H8	111	V_{RTC}	RTC Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
A4, A8, C11, D1, D11, F4, J1, M4, M9	B6, C1, C9, D8, K7, J2	11, 27, 29, 47, 60, 80, 81, 85, 89, 119, 136	V_{SS}	Digital Ground
H12	G9	98	V_{SSA}	Analog Ground
RESET				
L10	K8	114	RSTN	Hardware Power Reset (Active-Low) Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal pullup to the V_{DDIO} supply.
CLOCK				
L12	J10	107	32KIN	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, an external clock source can be driven on 32KIN if the 32KOUT pin is left unconnected.
K12	H10	106	32KOUT	32kHz Crystal Oscillator Output
GPIO AND ALTERNATE FUNCTIONS				
F5	—	—	P0.0	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
L2	—	2	P0.1	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
K3	—	3	P0.2	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
L1	—	4	P0.3	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
J3	—	6	P0.4	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
K2	—	7	P0.5	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
K1	—	8	P0.6	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H3	—	12	P0.7	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H2	—	13	P0.8	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G3	—	15	P0.9	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G2	—	17	P0.10	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F2	E2	22	P0.11	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F3	—	23	P0.12	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E2	E1	25	P0.13	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E3	D1	26	P0.14	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D2	G4	28	P0.15	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C1	F3	30	P0.16	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
C8	C5	58	P1.15	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B8	D5	59	P1.16	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E9	—	69	P1.17	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4and Table 5 GPIO and Alternate Function Matrix tables for details.
B9	B7	63	P1.18	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C9	C6	62	P1.19	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
C10	E6	66	P1.20	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
B10	B8	67	P1.21	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
—	—	75	P1.22	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F9	C7	70	P1.23	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H9	E7	92	P1.24	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G9	D6	72	P1.25	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
M10	J8	115	P1.26	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
J9	H7	116	P1.27	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
K9	J7	117	P1.28	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and TTable 5 GPIO and Alternate Function Matrix tables for details.
L9	H6	118	P1.29	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
J5	G3	140	P2.13	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
K4	J1	143	P2.14	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H5	H1	144	P2.15	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
J4	G2	1	P2.16	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
G7	F2	19	P2.17	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
F7	H5	20	P2.18	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D7	—	—	P2.19	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E7	—	—	P2.20	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
E8	—	—	P2.21	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D9	—	—	P2.22	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
D8	A6	57	P2.23	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H7	—	—	P2.24	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
K6	—	133	P2.25	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
J6	—	135	P2.26	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.
H6	—	—	P2.27	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 3, Table 4 and Table 5 GPIO and Alternate Function Matrix tables for details.

Memory

Internal Flash Memory

3MB of internal flash memory provides nonvolatile storage of program and data memory.

Flash can be expanded through the SPIXF flash serial interface backed by 16KB of cache. The SPIXF flash interface can address an additional 128MB.

Internal SRAM

The internal 1MB SRAM provides low-power retention of application information in all power modes except shutdown. The SRAM can be divided into granular banks that create a flexible SRAM retention architecture. This data retention feature is optional and configurable. This granularity allows the application to minimize its power consumption by only retaining the most essential data.

SRAM can be expanded through the SPIXR SRAM serial interface backed by 16KB of cache. The SPIXR SRAM interface can address an additional 512MB.

Secure Digital Interface

The secure digital interface (SDI) provides high-speed, high-density data storage capability for media files and large long-term data logs. This interface supports eMMC, SD, SDHC, and SDXC memory devices up to 4GB at transfer rates up to 30MB/s. The 7-pin interface (4 data, 1 clock, 1 command, 1 write-protect) supports the following specifications:

- SD Host Controller Standard Specification Version 3.00
- SDIO Card Specification Version 3.0
- SD Memory Card Specification Version 3.01
- SD Memory Card Security Specification Version 1.01
- MMC Specification Version 4.51

Spansion HyperBus/Xccela Bus

The Spansion HyperBus/Xccela bus interface provides access to external Cypress Spansion HyperBus and Xccela bus memory products both SRAM and/or flash. This interface provides a means of high-speed execution from external SRAM or flash allowing system expansion when internal memory resources are insufficient. Up to 8MB SRAM or 512MB flash at a speed of up to 60MHz or 120MBps is supported. It is a high-speed low-pin count interface that is memory-mapped into the CPU memory space making access to this external memory as easy as accessing on-chip RAM. Data is transferred over a high-speed, 8-bit bus. Slave memory devices are selected with two chip selects. HyperBus transfers are clocked using a differential clock while Xccela bus transfers use a single-ended clock. This interface supports 1.8V operation only.

Features of the HyperBus/Xccela bus interface include:

- Master/slave system
- 120MBps maximum data transfer rate
- Double data rate (DDR): two data transfers per clock cycle
- Transparent bus operation to the processor
- 16KB write-through cache
- Two chip selects for two memory ports
  - Each port supports memories up to 512MB
- Addresses two external memories, one at a time
- Interfaces to HyperFlash, HyperRAM, and Xccela PSRAM
- Zero wait state burst mode operation
- Low-power Half Sleep mode
  - Puts the external memory device into low power mode while retaining memory contents
- Configurable timing parameters

Clocking Scheme

The high-frequency oscillator operates at a maximum frequency of 120MHz.

Optionally, 4 other oscillators can be selected depending upon power needs:

- 40MHz low-power oscillator
- 8kHz nano-ring oscillator
- 32.768kHz oscillator (external crystal required)
- 7.3728MHz oscillator

This clock is the primary clock source for the digital logic and peripherals. Select the 7.3728MHz internal oscillator to optimize active power consumption. Using the 7.3727MHz oscillator allows UART communications to meet a ±2% baud rate tolerance.

Wakeup is possible from either the 7.3728MHz internal oscillator or the high-frequency oscillator. The device exits power-on reset using the the 40MHz oscillator.

An external 32.768kHz timebase is required when using the RTC.

USB Controller

The integrated USB device controller is compliant with the Hi-Speed (480Mbps) USB 2.0 specification. The integrated USB physical interface (PHY) reduces board space and system cost. An integrated voltage regulator enables smart switching between the main supply and V_{DDB} when connected to a USB host controller.

- Supports DMA for the endpoint buffers. A total of 12 endpoint buffers are supported with configurable selection of IN or OUT in addition to endpoint 0.
- Isochronous, bulk, interrupt, and control transfers
- Automatic packet splitting and combining
- FIFOs up to 4096 bytes deep
- Double packet buffering
- USB 2.0 test mode support

I²C Interface

The I²C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many or many-to-many communications medium. Two I²C master/slave interface to a wide variety of I²C-compatible peripherals. These engines support standard mode, fast mode, and fast mode plus I²C speeds. It provides the following features:

- Master or slave mode operation
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive Receive mode
- Tx FIFO preloading
- Support for clock stretching to allow slower slave devices to operate on higher speed busses
- Multiple transfer rates
  - Standard mode: 100kbps
  - Fast mode: 400kbps
  - Fast mode plus: 1000kbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes

The MAX32650–MAX32652 provide two instances of the I²C peripheral (I2C0 and I2C1).

UART

The universal asynchronous receiver-transmitter (UART) interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry standard request to send (RTS) and clear to send (CTS) flow control signaling. Each UART is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 32-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for frame error, parity error, CTS, Rx FIFO overrun and FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Baud rate generation with ±2% optionally utilizing the 7.3727MHz relaxation oscillator
- Maximum baud rate 4000kB
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

The MAX32650–MAX32652 provide three instances of the UART peripheral (UART0, UART1, and UART2) according to the specifications in Table 2.

Serial Peripheral Interface Execute in Place (SPIX) Master

There are two SPI execute-in-place master interfaces. One for SRAM (SPIXR) and one for flash (SPIXF) with dedicated slave selects. This feature allows the CPU to transparently execute instructions stored in an external SPI memory device. Instructions fetched through the SPI master are cached like instructions fetched from internal program memory. The SPI SRAM master provides write-back capability. These two SPI execute in place master interfaces can also be used to access large amounts of external static data that would otherwise reside in internal data memory.

Table 2. UART Configuration Options

INSTANCE	FLOW CONTROL			MAXIMUM BAUD RATE (KB)
	144 TQFP	140 WLP	96 WLP	
UART0	YES	YES	NO	4000
UART1	YES	YES	YES	4000
UART2	YES	YES	NO	4000

1-Wire Master

Maxim's 1-wire bus consists of a single line to provide both power and data communications and a ground return. The bus supports a serial, multidrop communication protocol between a master and one or more slave devices with the minimum amount of interconnection.

Maxim's 1-wire bus consists of one signal that carries data and also supplies power to the slave devices, and a ground return. The bus master communicates serially with one or more slave devices through the bidirectional, multidrop 1-Wire bus. The single contact serial interface is ideal for communication networks requiring minimal interconnection.

The provided 1-Wire master supports the following features:

- Single contact for control and operation
- Unique factory identifier for any 1-Wire device
- Multiple device capability on a single line

The MAX32650–MAX32652 1-Wire master supports both the standard (15.6kbps) and overdrive (110kbps) speeds.

24-Bit Color TFT Controller

The 24-bit color TFT controller is controlled by the CPU through the APB and fed graphic data through the AHB. The controller supports the following display types:

- Active matrix TFT panels with up to 24-bit bus interface
- Single/dual-panel monochrome STN panels (4-bit and 8-bit bus interface)
- Single/dual-panel color STN panels, 8-bit bus interface
- TFT panels up to 24bpp, direct 8:8:8 RGB
- Color STN panels up to 16bpp, direct 5:5:5 with one bit not being used
- Mono STN panels up to 4bpp, pelletized, 16 gray scales selected from 16

The controller can be programmed to operate a wide range of panel resolutions (including, but not limited to the following settings):

- 320 x 200, 320 x 240,
- 640 x 200, 640 x 240, 640 x 480
- 800 x 600
- 1024 x 768
- 2048 x 2048
- 4096 x 4096

Debug and Development Interface (SWD/JTAG)

Special versions of the device are available with a serial wire debug or JTAG interface that is used only during application development and debugging. The interface is used for code loading, ICE debug activities, and control of boundary scan activities. Devices in mass production must have the debugging/development interface disabled.

The *Ordering Information* contains unique part numbers for devices with the debugging/development interface enabled or disabled.

Trust Protection Unit (MAX32651 Only)

True Random Number Generator

Random numbers are a vital part of a secure application, providing random numbers that can be used for cryptographic seeds or strong encryption keys to ensure data privacy.

Software can use random numbers to trigger asynchronous events that result in nondeterministic behavior. This is helpful in thwarting replay attacks or key search approaches. An effective true random number generator (TRNG) must be continuously updated by a high-entropy source.

The provided TRNG is continuously driven by a physically-unpredictable entropy source. It generates a 128-bit true random number in 128 system clock cycles.

The TRNG can support the system-level validation of many security standards such as FIPS 140-2, PCI-PED, and Common Criteria. Contact Maxim for details of compliance with specific standards.

MAA

The provided high-speed, hardware-based modulo arithmetic accelerator (MAA) performs mathematical computations that support strong cryptographic algorithms. These include:

- 2048-bit DSA
- 4096-bit RSA
- Elliptic curve public key infrastructure

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

The AES keys are automatically generated by the engine and stored in dedicated flash to protect against tampering. Key generation and storage is transparent to the user.

SHA-256

SHA-256 is a cryptographic hash function part of the SHA-2 family of algorithms. It authenticates user data and verifies its integrity. It is used for digital signatures.

The device provides a hardware SHA-256 engine for fast computation of 256-bit digests.

Memory Decryption Integrity Unit

The external SPI flash can optionally be encrypted for additional security. Data can be transparently encrypted when it is loaded and decrypted on-the-fly. Encryption keys are stored in the always-on domain and preserved as long as V_{RTC} is present.

Secure Bootloader

The secure bootloader provides a secure, authenticated communication channel with a system host. The secure communication protocol (SCP) allows the programming of internal and external memory.

The secure bootloader provides the following features:

- Life cycle management
- Authentications using ECDSA P-256, with 256-bit ECC key pairs and SHA-256 secure hash function
- Preprogrammed Maxim manufacturer root key (MRK)
- Programmable customer root key (CRK)
- Support for 2048- or 4096-bit RSA digital signature

Additional Documentation and Technical Support

Designers must have the following documents to use all the features of this device:

- This data sheet, which contains electrical/timing specifications, package information, and pin descriptions
- The corresponding revision-specific errata sheet
- The corresponding user guide, which contains detailed information and programming guidelines for core features and peripherals

Applications Information

GPIO and Alternate Function Matrix, 140 WLP

Table 3. GPIO and Alternate Function Matrix, 140 WLP

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P0.0	PT3	SPIXF_SDIO2**
P0.1	SPIXR_SDIO0**	—
P0.2	SPIXR_SDIO2**	—
P0.3	SPIXR_SCK**	—
P0.4	SPIXR_SDIO3**	—
P0.5	SPIXR_SDIO1**	—
P0.6	SPIXR_SS0**	—
P0.7	SPIXF_SS0**	—
P0.8	SPIXF_SCK**	—
P0.9	SPIXF_SDIO1**	—
P0.10	SPIXF_SDIO0**	—
P0.11	SPIXF_SDIO2**	—
P0.12	SPIXF_SDIO3**	—
P0.13	SPI3_SS1	CLCD_G0
P0.14	SPI3_SS2	CLCD_G1
P0.15	SPI3_SDIO3	CLCD_G2
P0.16	SPI3_SCK	CLCD_G3
P0.17	SPI3_SDIO2	CLCD_G4
P0.18	SPI3_SS3	CLCD_G5
P0.19	SPI3_SS0	CLCD_G6
P0.20	SPI3_SDIO1	CLCD_G7
P0.21	SPI3_SDIO0	—
P0.22	SPI0_SS0	CLCD_VDEN
P0.23	PT15	CLCD_CLK

Table 3. GPIO and Alternate Function Matrix, 140 WLP (continued)

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P3.4	TMR0	—
P3.5	TMR2	—
P3.6	TMR4	—
P3.7	TMR1	—
P3.8	TMR3	—
P3.9	TMR5	—

*GPIO not pinned out.
**This signal can be mapped to more than one GPIO, but there is only one instance of this peripheral.
†I2S_BCLK, I2S_LRCLK, I2S_SDI, and I2S_SDO when enabled.
††Single-wire debug when enabled.

GPIO and Alternate Function Matrix, 96 WLP

Table 4. GPIO and Alternate Function Matrix, 96 WLP

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P0.0*	—	—
P0.1*	—	—
P0.2*	—	—
P0.3*	—	—
P0.4*	—	—
P0.5*	—	—
P0.6*	—	—
P0.7*	—	—
P0.8*	—	—
P0.9*	—	—
P0.10*	—	—
P0.11	SPIXF_SDIO2**	P0.11
P0.12*	—	—
P0.13	SPI3_SS1	CLCD_G0
P0.14	SPI3_SS2	CLCD_G1
P0.15	SPI3_SDIO3	CLCD_G2
P0.16	SPI3_SCK	CLCD_G3
P0.17	SPI3_SDIO2	CLCD_G4
P0.18	SPI3_SS3	CLCD_G5
P0.19	SPI3_SS0	CLCD_G6
P0.20	SPI3_SDIO1	CLCD_G7
P0.21	SPI3_SDIO0	—
P0.22	SPI0_SS0	CLCD_VDEN
P0.23*	—	—
P0.24*	—	—
P0.25*	—	—
P0.26	TDI	—
P0.27	TDO	—
P0.28	TMS (SWDIO)††	—
P0.29	TCK (SWDCLK)††	—
P0.30	—	CLCD_B0
P0.31*	—	—
P1.0	SDHC_CMD	SPIXF_SDIO3**
P1.1	SDHC_DAT2	SPIXF_SDIO1**
P1.2	SDHC_WP	SPIXF_SS0**
P1.3	SDHC_DAT3	CLCD_CLK
P1.4	SDHC_DAT0	SPIXF_SDIO0**
P1.5	SDHC_CLK	SPIXF_SCK**
P1.6	SDHC_DAT1	PT0
P1.7*	—	—
P1.8	UART2_RTS	PT2
P1.9	UART2_RX	PT3
P1.10	UART2_TX	PT4
P1.11	—	SPIXR_SDIO0**
P1.12	—	SPIXR_SDIO1**
P1.13	—	SPIXR_SS0**
P1.14	—	PT5
P1.15	—	SPIXR_SDIO2**
P1.16	—	SPIXR_SCK**
P1.17*	—	—
P1.18	—	PT6
P1.19	—	PT7
P1.20	—	CLCD_HSYNC
P1.21	—	PT8

Table 4. GPIO and Alternate Function Matrix, 96 WLP (continued)

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P1.22*	—	—
P1.23	SPI1_SS0	CLCD_B1
P1.24	SPI1_SS2	CLCD_B2
P1.25	SPI1_SS1	CLCD_B3
P1.26	SPI1_SCK	CLCD_B4
P1.27	SPI1_SS3	CLCD_B5
P1.28	SPI1_MISO	CLCD_B6
P1.29	SPI1_MOSI	CLCD_B7
P1.30	OWM_PUPEN	CLCD_R0
P1.31	OWM_IO	CLCD_R1
P2.0	SPI2_SS2	PT9
P2.1*	—	—
P2.2	SPI2_SCK (I2S-BCLK)†	CLCD_LEND
P2.3	SPI2_MISO (I2S-SDI)†	CLCD_PWREN
P2.4	SPI2_MOSI (I2S-SDO)†	—
P2.5	SPI2_SS0 (I2S_LR-CLK)†	PT11
P2.6	SPI2_SS3	CLCD_VSYNC
P2.7*	—	—
P2.8*	—	—
P2.9	UART0_CTS	PT12
P2.10*	—	—
P2.11	UART0_RX	PT13
P2.12	UART0_TX	PT15
P2.13	UART1_CTS	CLCD_R2
P2.14	UART1_RX	CLCD_R3

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P2.15	UART1_RTS	CLCD_R4
P2.16	UART1_TX	CLCD_R5
P2.17	I2C1_SDA	CLCD_R6
P2.18	I2C1_SCL	CLCD_R7
P2.19*	—	—
P2.20*	—	—
P2.21*	—	—
P2.22*	—	—
P2.23	PT6	SPIXR_SDIO3**
P2.24*	—	—
P2.25*	—	—
P2.26*	—	—
P2.27*	—	—
P2.28*	—	—
P2.29*	—	—
P2.30*	—	—
P2.31*	—	—
P3.0*	—	—
P3.1*	—	—
P3.2*	—	—
P3.3*	—	—
P3.4	TMR0	—
P3.5	TMR2	—
P3.6	TMR4	—
P3.7	TMR1	—
P3.8	TMR3	—
P3.9	TMR5	—

**GPIO not pinned out.*
***This signal can be mapped to more than one GPIO, but there is only one instance of this peripheral.*
†I2S_BCLK, I2S_LRCLK, I2S_SDI, I2S_SDO when enabled.
††Single-wire debug when enabled.

GPIO and Alternate Function Matrix, 144 TQFP

Table 5. GPIO and Alternate Function Matrix, 144 TQFP

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P0.0*	—	—
P0.1	SPIXR_SDIO0**	—
P0.2	SPIXR_SDIO2**	—
P0.3	SPIXR_SCK**	—
P0.4	SPIXR_SDIO3**	—
P0.5	SPIXR_SDIO1**	—
P0.6	SPIXR_SS0**	—
P0.7	SPIXF_SS0**	—
P0.8	SPIXF_SCK**	—
P0.9	SPIXF_SDIO1**	—
P0.10	SPIXF_SDIO0**	—
P0.11	SPIXF_SDIO2**	—
P0.12	SPIXF_SDIO3**	—
P0.13	SPI3_SS1	CLCD_G0
P0.14	SPI3_SS2	CLCD_G1
P0.15	SPI3_SDIO3	CLCD_G2
P0.16	SPI3_SCK	CLCD_G3
P0.17	SPI3_SDIO2	CLCD_G4
P0.18	SPI3_SS3	CLCD_G5
P0.19	SPI3_SS0	CLCD_G6
P0.20	SPI3_SDIO1	CLCD_G7
P0.21	SPI3_SDIO0	—
P0.22	SPI0_SS0	CLCD_VDEN
P0.23	PT15	CLCD_CLK
P0.24	RXEV	CLCD_HSYNC
P0.25	TXEV	CLCD_B0
P0.26	TDI	—
P0.27	TDO	—
P0.28	TMS (SWDIO)†††	—
P0.29	TCK (SWDCLK)†††	—
P0.30	—	CLCD_B0
P0.31	32KCAL	SDHC_CDN
P1.0	SDHC_CMD	SPIXF_SDIO3**
P1.1	SDHC_DAT2	SPIXF_SDIO1**

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P1.2	SDHC_WP	SPIXF_SS0**
P1.3	SDHC_DAT3	CLCD_CLK
P1.4	SDHC_DAT0	SPIXF_SDIO0**
P1.5	SDHC_CLK	SPIXF_SCK**
P1.6	SDHC_DAT1	PT0
P1.7	UART2_CTS	PT1
P1.8	UART2_RTS	PT2
P1.9	UART2_RX	PT3
P1.10	UART2_TX	PT4
P1.11	HYP_CS0N	SPIXR_SDIO0**
P1.12	HYP_D0	SPIXR_SDIO1**
P1.13	HYP_D4	SPIXR_SS0**
P1.14	HYP_RWDS	PT5
P1.15	HYP_D1	SPIXR_SDIO2**
P1.16	HYP_D5	SPIXR_SCK**
P1.17	PT9	—
P1.18	HYP_D6	PT6
P1.19	HYP_D2	PT7
P1.20	HYP_D3	CLCD_HSYNC
P1.21	HYP_D7	PT8
P1.22	—	—
P1.23	SPI1_SS0	CLCD_B1
P1.24	SPI1_SS2	CLCD_B2
P1.25	SPI1_SS1	CLCD_B3
P1.26	SPI1_SCK	CLCD_B4
P1.27	SPI1_SS3	CLCD_B5
P1.28	SPI1_MISO	CLCD_B6
P1.29	SPI1_MOSI	CLCD_B7
P1.30	OWM_PUPEN	CLCD_R0
P1.31	OWM_IO	CLCD_R1
P2.0	SPI2_SS2	PT9
P2.1	SPI2_SS1	PT10
P2.2	SPI2_SCK (I2S-BCLK)†	CLCD_LEND

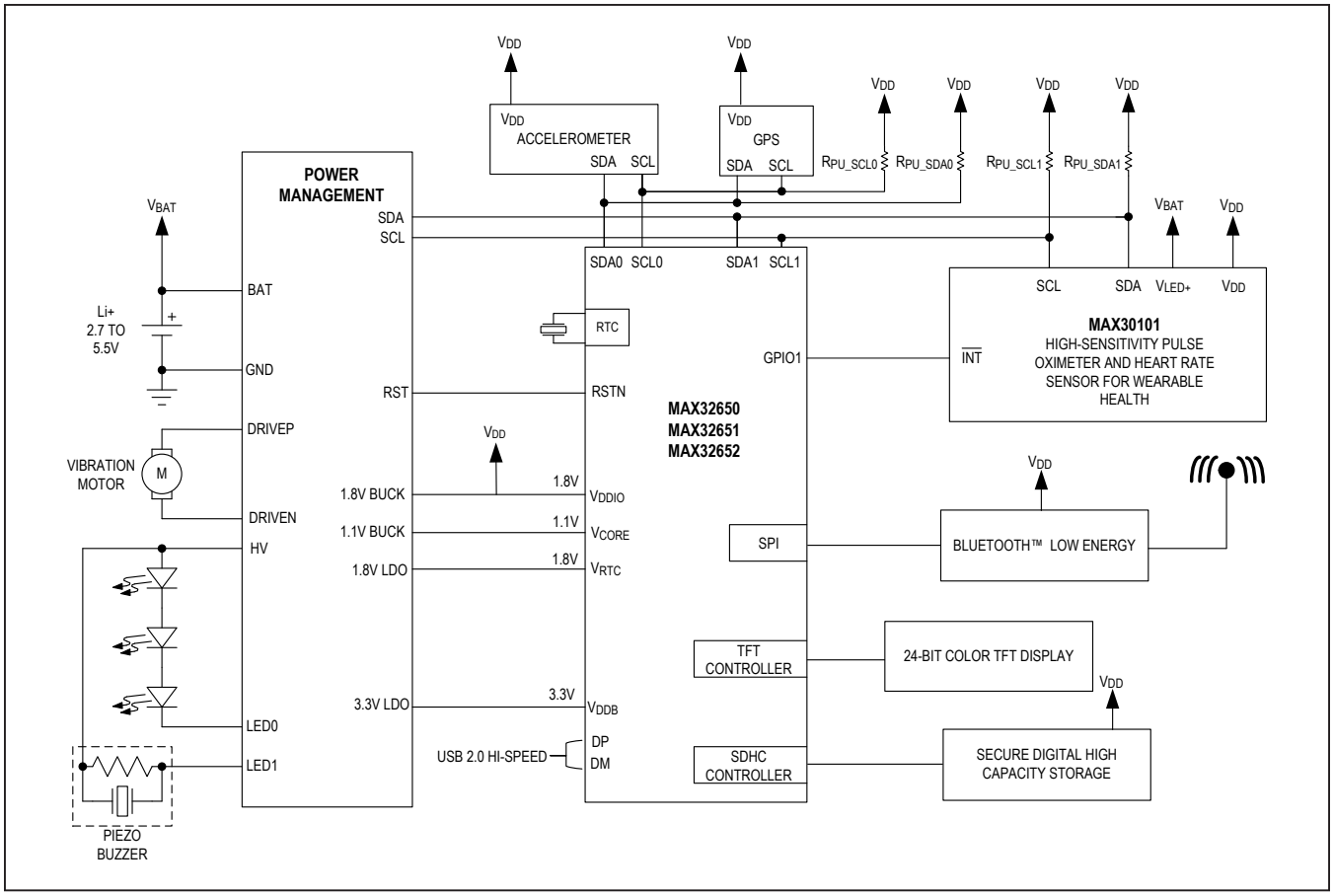
Table 5. GPIO and Alternate Function Matrix, 144 TQFP (continued)

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P2.3	SPI2_MISO (I2S-SDI)†	CLCD_PWREN
P2.4	SPI2_MOSI (I2S-SDO)†	—
P2.5	SPI2_SS0 (I2S_LR-CLK)†	PT11
P2.6	SPI2_SS3	CLCD_VSYNC
P2.7	I2C0_SDA	—
P2.8	I2C0_SCL	—
P2.9	UART0_CTS	PT12
P2.10	UART0_RTS	PT14
P2.11	UART0_RX	PT13
P2.12	UART0_TX	PT15
P2.13	UART1_CTS	CLCD_R2
P2.14	UART1_RX	CLCD_R3
P2.15	UART1_RTS	CLCD_R4
P2.16	UART1_TX	CLCD_R5
P2.17	I2C1_SDA	CLCD_R6
P2.18	I2C1_SCL	CLCD_R7
P2.19*	—	—
P2.20*	—	—
P2.21*	—	—
P2.22*	—	—
P2.23	PT6	SPIXR_SDIO3**
P2.24*	—	—
P2.25	PT11	—
P2.26	PT12	—
P2.27*	—	—
P2.28	PT14	—
P2.29*	—	—
P2.30	PT1	—
P2.31*	—	—
P3.0	PDOWN	HYP_CS1N
P3.1	SPI0_MISO	—
P3.2	SPI0_MOSI	—
P3.3	SPI0_SCK	—
P3.4	TMR0	—
P3.5	TMR2	—
P3.6	TMR4	—
P3.7	TMR1	—
P3.8	TMR3	—
P3.9	TMR5	—

**GPIO not pinned out.*
***This signal can be mapped to more than one GPIO, but there is only one instance of this peripheral.*
†I2S_BCLK, I2S_LRCLK, I2S_SDI, I2S_SDO when enabled.
††PBM Interface signal when enabled.
†††Single-wire debug when enabled.

Typical Application Circuit

Pulse Oximeter and Heart Rate Monitor with BLE and GPS Location



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Ordering Information

PART	TRUST PROTECTION UNIT WITH SECURE BOOTLOADER	PIN-PACKAGE
MAX32650GWQ+*	No	96 WLP (0.4mm pitch)
MAX32650GWQ+T*	No	96 WLP (0.4mm pitch)
MAX32650GCE+*	No	144 TQFP
MAX32651GWQ+*	Yes	96 WLP (0.4mm pitch)

PART	TRUST PROTECTION UNIT WITH SECURE BOOTLOADER	PIN-PACKAGE
MAX32651GWQ+T*	Yes	96 WLP (0.4mm pitch)
MAX32651GCE+*	Yes	144 TQFP
MAX32652GWE+	No	140 WLP (0.35mm pitch)
MAX32652GWE+T	No	140 WLP (0.35mm pitch)

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**Future product—contact factory for availability.*