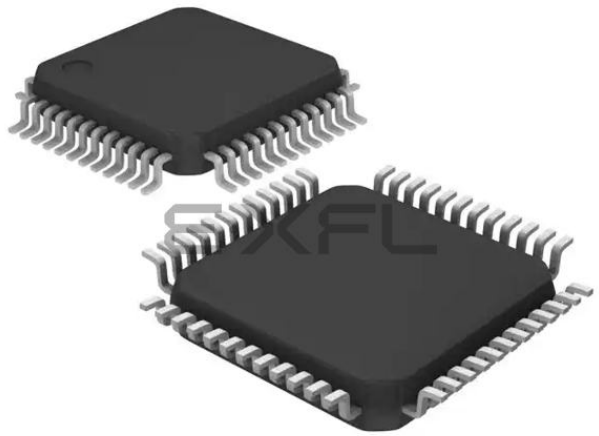

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l053c6t6

List of tables

2.2 Ultra-low-power device continuum

The ultra-low-power family offers a large choice of core and features, from 8-bit proprietary core up to ARM® Cortex®-M4, including ARM® Cortex®-M3 and ARM® Cortex®-M0+. The STM32Lx series are the best choice to answer your needs in terms of ultra-low-power features. The STM32 ultra-low-power series are the best solution for applications such as gaz/water meter, keyboard/mouse or fitness and healthcare application. Several built-in features like LCD drivers, dual-bank memory, low-power run mode, operational amplifiers, 128-bit AES, DAC, crystal-less USB and many other definitely help you building a highly cost optimized application by reducing BOM cost. STMicroelectronics, as a reliable and long-term manufacturer, ensures as much as possible pin-to-pin compatibility between all STM8Lx and STM32Lx on one hand, and between all STM32Lx and STM32Fx on the other hand. Thanks to this unprecedented scalability, your legacy application can be upgraded to respond to the latest market feature and efficiency requirements.

3 Functional overview

3.1 Low-power modes

The ultra-low-power STM32L053x6/8 support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

  This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

  Stop mode with RTC

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSE crystal and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USB/USART/I2C/LPUART/LPTIMER wakeup events.

Table 4. Functionalities depending on the working mode (from Run/active down to standby) (continued)(1)

IPs	Run/Active	Sleep	Low-power run	Low-power sleep	Stop		Standby	
						Wakeup capability		Wakeup capability
DAC	O	O	O	O	O		--	
Temperature sensor	O	O	O	O	O		--	
Comparators	O	O	O	O	O	O	--	
16-bit timers	O	O	O	O	--		--	
LPTIMER	O	O	O	O	O	O		
IWDG	O	O	O	O	O	O	O	O
WWDG	O	O	O	O	--		--	
Touch sensing controller (TSC)	O	O	--	--	--		--	
SysTick Timer	O	O	O	O			--	
GPIOs	O	O	O	O	O	O		2 pins
Wakeup time to Run mode	0 µs	0.36 µs	3 µs	32 µs	3.5 µs		50 µs	
Consumption V_{DD}=1.8 to 3.6 V (Typ)	Down to 140 µA/MHz (from Flash memory)	Down to 37 µA/MHz (from Flash memory)	Down to 8 µA	Down to 4.5 µA	0.4 µA (No RTC) V_{DD}=1.8 V		0.28 µA (No RTC) V_{DD}=1.8 V	
					0.8 µA (with RTC) V_{DD}=1.8 V		0.65 µA (with RTC) V_{DD}=1.8 V	
					0.4 µA (No RTC) V_{DD}=3.0 V		0.29 µA (No RTC) V_{DD}=3.0 V	
					1 µA (with RTC) V_{DD}=3.0 V		0.85 µA (with RTC) V_{DD}=3.0 V	

1. Legend:
   "Y" = Yes (enable).
   "O" = Optional can be enabled/disabled by software)
   "-" = Not available

2. Some peripherals with wakeup from Stop capability can request HSI to be enabled. In this case, HSI is woken up by the peripheral, and only feeds the peripheral which requested it. HSI is automatically put off when the peripheral does not need it anymore.

3. UART and LPUART reception is functional in Stop mode. It generates a wakeup interrupt on Start. To generate a wakeup on address match or received frame event, the LPUART can run on LSE clock while the UART has to wake up or keep running the HSI clock.

4. I2C address detection is functional in Stop mode. It generates a wakeup interrupt in case of address match. It will wake up the HSI during reception.

3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 28 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 51 GPIOs can be connected to the 16 configurable interrupt/event lines. The 12 other lines are connected to PVD, RTC, USB, USARTs, LPUART, LPTIMER or comparator events.

3.18.6 Window watchdog (WWDG)

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.19 Communication interfaces

3.19.1 I²C bus

two I²C interface (I2C1, I2C2) can operate in multimaster or slave modes.

Each I²C interface can support Standard mode (Sm, up to 100 kbit/s), Fast mode (Fm, up to 400 kbit/s) and Fast Mode Plus (Fm+, up to 1 Mbit/s) with 20 mA output drive on some I/Os.

7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask) are also supported as well as programmable analog and digital noise filters.

Table 10. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBus 2.0 and PMBus 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

Each I2C interface can be served by the DMA controller.

Refer to *Table 11* for an overview of I2C interface features.

Table 11. STM32L053x6/8 I²C implementation

I2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X(2)
Independent clock	X	-

Table 14. Legend/abbreviations used in the pinout table (continued)

Name		Abbreviation	Definition
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 15. STM32L053x6/8 pin definitions

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64						
1	1	B2	VLCD	S	-	-	-	-
2	2	A2	PC13	I/O	FT	-	-	RTC_TAMP1/RTC_TS/RTC_OUT/WKUP2
3	3	A1	PC14-OSC32_IN (PC14)	I/O	FT	-	-	OSC32_IN
4	4	B1	PC15-OSC32_OUT (PC15)	I/O	TC	-	-	OSC32_OUT
5	5	C1	PH0-OSC_IN (PH0)	I/O	TC	-	USB_CRS_SYNC	OSC_IN
6	6	D1	PH1-OSC_OUT (PH1)	I/O	TC	-	-	OSC_OUT
7	7	E1	NRST	I/O	RST	-	-	-
-	8	E3	PC0	I/O	FT	-	LPTIM1_IN1, LCD_SEG18, EVENTOUT, TSC_G7_IO1	ADC_IN10
-	9	E2	PC1	I/O	FT	-	LPTIM1_OUT, LCD_SEG19, EVENTOUT, TSC_G7_IO2	ADC_IN11
-	10	F2	PC2	I/O	FT	-	LPTIM1_IN2, LCD_SEG20, SPI2_MISO/I2S2_MCK, TSC_G7_IO3	ADC_IN12
-	11	-	PC3	I/O	FT	-	LPTIM1_ETR, LCD_SEG21, SPI2_MOSI/I2S2_SD, TSC_G7_IO4	ADC_IN13

Table 22. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD} (2)	Total current into sum of all V_{DD} power lines (source)(1)	105	mA
ΣI_{VSS} (2)	Total current out of sum of all V_{SS} ground lines (sink)(1)	105	
ΣI_{VDD_USB}	Total current into V_{DD_USB} power lines (source)	25	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin except FTf pins	16	
	Output current sunk by FTf pins	22	
	Output current sourced by any I/O and control pin	-16	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins except PA11 and PA12(2)	90	
	Total output current sunk by PA11 and PA12	25	
	Total output current sourced by sum of all IOs and control pins(2)	-90	
$I_{INJ(PIN)}$	Injected current on FT, FTf, RST and B pins	-5/+0(3)	
	Injected current on TC pin	± 5(4)	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 21* for maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 21: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 23. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 30. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	1 MHz	135	170	µA
				2 MHz	240	270	
				4 MHz	450	480	
			Range 2, V_{CORE}=1.5 ,V, VOS[1:0]=10	4 MHz	0.52	0.6	mA
				8 MHz	1	1.2	
				16 MHz	2	2.3	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	1.25	1.4	
				16 MHz	2.45	2.8	
				32 MHz	5.1	5.4	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	34.5	75	µA
				524 kHz	83	120	
				4.2 MHz	485	540	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	16 MHz	2.1	2.3	mA
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	5.1	5.6	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 31. Current consumption in Run mode vs code type, code with data processing running from RAM(1)

Symbol	Parameter	Conditions			f_{HCLK}	Typ	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	450	µA
				CoreMark		575	
				Fibonacci		370	
				while(1)		340	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	Dhrystone	32 MHz	5.1	mA
				CoreMark		6.25	
				Fibonacci		4.4	
				while(1)		4.7	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Low-speed external user clock generated from an external source

The characteristics given in the following table result from tests performed using a low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 24*.

Table 42. Low-speed external user clock characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	1	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time		465	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time		-	-	10	
$C_{IN(LSE)}$	OSC32_IN input capacitance	-	-	0.6	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production

Figure 18. Low-speed external clock source AC timing diagram

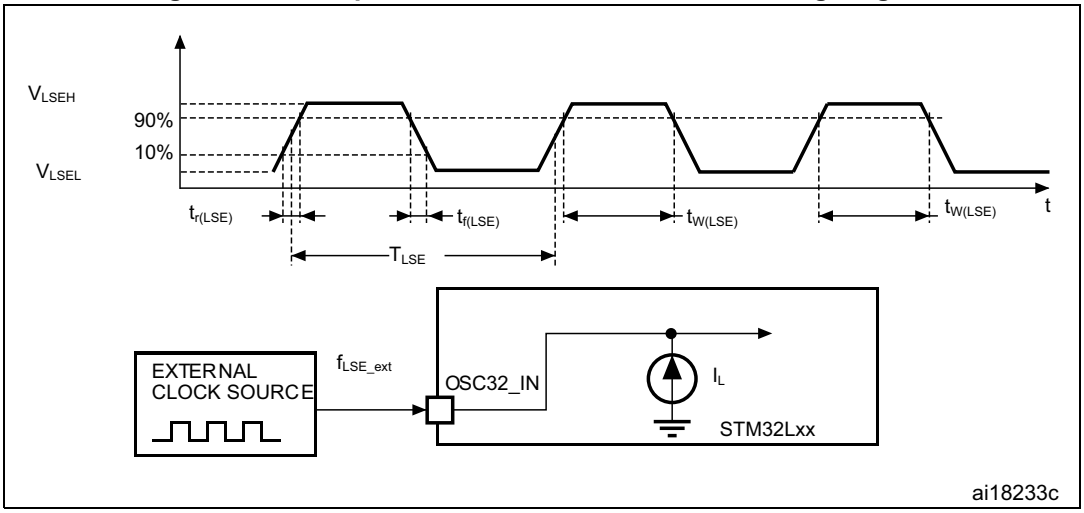


Table 48. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤T_A ≤85 °C	-	±3	-	%
	MSI oscillator frequency drift V_{DD} = 3.3 V, − 40 °C ≤T_A ≤110 °C	MSI range 0	− 8.9	+7.0	
		MSI range 1	− 7.1	+5.0	
		MSI range 2	− 6.4	+4.0	
		MSI range 3	− 6.2	+3.0	
		MSI range 4	− 5.2	+3.0	
		MSI range 5	− 4.8	+2.0	
		MSI range 6	− 4.7	+2.0	
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤V_{DD} ≤3.6 V, T_A = 25 °C	-	-	2.5	%/V
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 24* and *Table 60*, respectively.

Unless otherwise specified, the parameters given in *Table 60* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 60. I/O AC characteristics(1)

OSPEEDRx[1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Max(2)	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	400	kHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	100	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	125	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	320	
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	2	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	0.6	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	65	
10	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	10	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	2	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	13	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	28	
11	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	35	MHz
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	10	
	$t_{f(IO)out}$ $t_{r(IO)out}$	Output rise and fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	6	ns
			C_L = 50 pF, V_{DD} = 1.65 V to 2.7 V	-	17	
Fm+ configuration(4)	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 2.5 V to 3.6 V	-	1	MHz
	$t_{f(IO)out}$	Output fall time		-	10	ns
	$t_{r(IO)out}$	Output rise time		-	30	
	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} = 1.65 V to 3.6 V	-	350	KHz
	$t_{f(IO)out}$	Output fall time		-	15	ns
	$t_{r(IO)out}$	Output rise time		-	60	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	8	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the line reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. The maximum frequency is defined in *Figure 24*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the line reference manual for a detailed description of Fm+ I/O configuration.

Table 65. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes till DAC_OUT reaches final value ±1LSB	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	7	12	µs
Update rate	Max frequency for a correct DAC_OUT change (95% of final value) with 1 LSB variation in the input code	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-	1	Msps
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC Control register)(9)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	9	15	µs
PSRR+	V_{DDA} supply rejection ratio (static DC measurement)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ	-	-60	-35	dB

1. Guaranteed by characterization results.
2. Guaranteed by design, not tested in production.
3. Connected between DAC_OUT and V_{SSA}.
4. Difference between two consecutive codes - 1 LSB.
5. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 4095.
6. Difference between the value measured at Code (0x800) and the ideal value = $V_{REF+}/2$.
7. Difference between the value measured at Code (0x001) and the ideal value.
8. Difference between ideal slope of the transfer function and measured slope computed from code 0x000 and 0xFFF when buffer is OFF, and from code giving 0.2 V and (V_{DDA} – 0.2) V when buffer is ON.
9. In buffered mode, the output can overshoot above the final value for low input code (starting from min value).

Figure 30. 12-bit buffered/non-buffered DAC

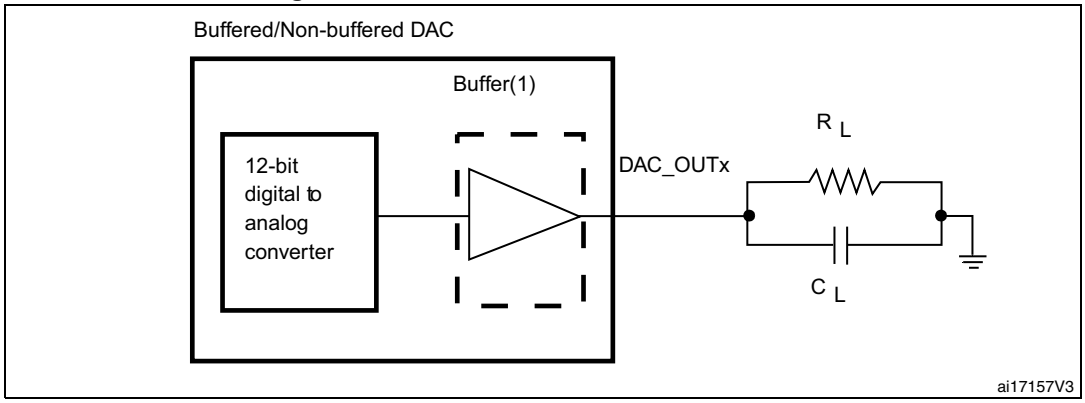
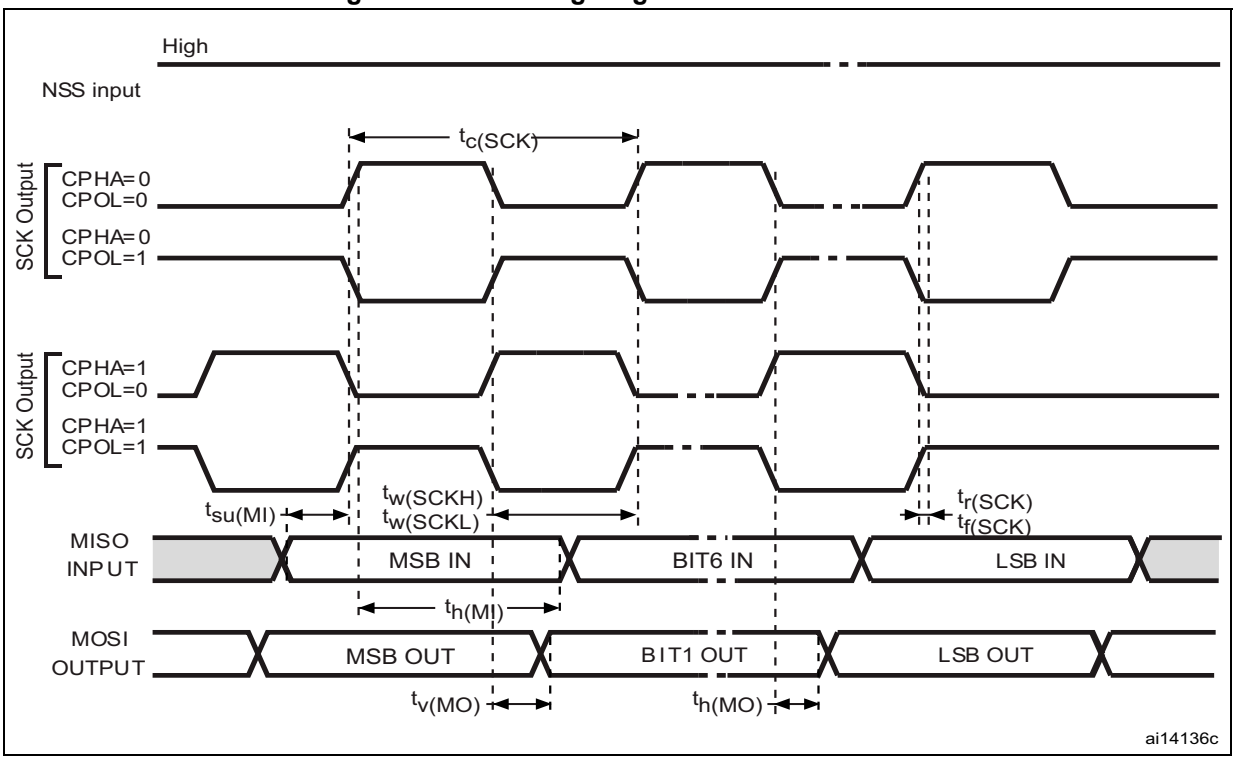


Figure 33. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 36. USB timings: definition of data signal rise and fall time

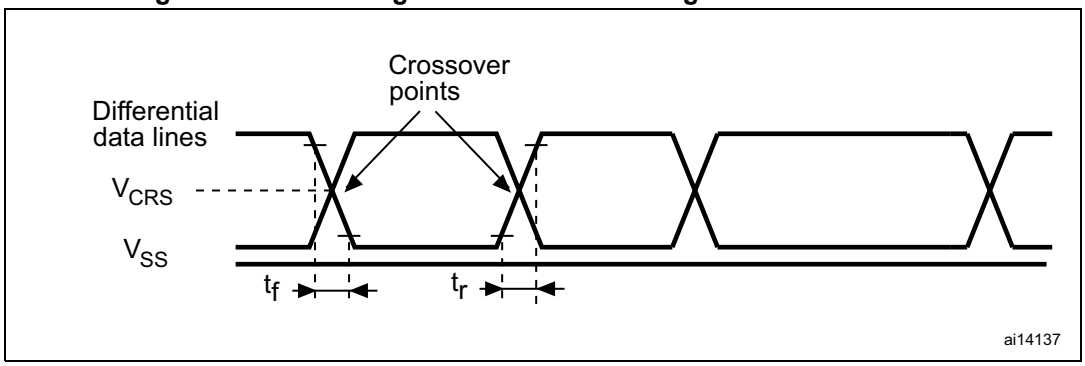


Table 79. USB: full speed electrical characteristics

Driver characteristics[1]					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time[2]	C_L = 50 pF	4	20	ns
t_f	Fall Time[2]	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

6.3.21 LCD controller

The devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the V_{LCD} pin to decouple this converter.

Table 80. LCD controller characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage	-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0	-	2.6	-	
V_{LCD1}	LCD internal reference voltage 1	-	2.73	-	
V_{LCD2}	LCD internal reference voltage 2	-	2.86	-	
V_{LCD3}	LCD internal reference voltage 3	-	2.98	-	
V_{LCD4}	LCD internal reference voltage 4	-	3.12	-	
V_{LCD5}	LCD internal reference voltage 5	-	3.26	-	
V_{LCD6}	LCD internal reference voltage 6	-	3.4	-	
V_{LCD7}	LCD internal reference voltage 7	-	3.55	-	
C_{ext}	V_{LCD} external capacitance	0.1	-	2	µF

Table 80. LCD controller characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit
I_{LCD}(1)	Supply current at V_{DD} = 2.2 V	-	3.3	-	µA
	Supply current at V_{DD} = 3.0 V	-	3.1	-	
R_{Htot}(2)	Low drive resistive network overall value	5.28	6.6	7.92	MΩ
R_L(2)	High drive resistive network total value	192	240	288	kΩ
V_{44}	Segment/Common highest level voltage	-	-	V_{LCD}	V
V_{34}	Segment/Common 3/4 level voltage	-	3/4 V_{LCD}	-	V
V_{23}	Segment/Common 2/3 level voltage	-	2/3 V_{LCD}	-	
V_{12}	Segment/Common 1/2 level voltage	-	1/2 V_{LCD}	-	
V_{13}	Segment/Common 1/3 level voltage	-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage	-	1/4 V_{LCD}	-	
V_0	Segment/Common lowest level voltage	0	-	-	
ΔVxx(3)	Segment/Common level voltage error T_A = -40 to 85 °C	-	-	±50	mV

1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected.
2. Guaranteed by design.
3. Guaranteed by characterization results.

9 Revision history

Table 87. Document revision history

Date	Revision	Changes
07-Feb-2014	1	Initial release.
29-Apr-2014	2	Updated *Table 4: Functionalities depending on the working mode (from Run/active down to standby)*. Added *Section 3.2: Interconnect matrix*. Updated *Figure 4: STM32L053x6/8 TFBGA64 ballout - 5x 5 mm*. Added VREF_OUT additional function to PB0 and PB1, replaced TTa I/O structure by TC, and updated PA0/4/5 and PC5/14 I/O structure, and added note 2 in *Table 15: STM32L053x6/8 pin definitions*. Updated *Table 24: General operating conditions*, *Table 21: Voltage characteristics* and *Table 22: Current characteristics*. Modified conditions in *Table 27: Embedded internal reference voltage*. Updated *Table 28: Current consumption in Run mode, code with data processing running from Flash*, *Table 30: Current consumption in Run mode, code with data processing running from RAM*, *Table 32: Current consumption in Sleep mode*, *Table 33: Current consumption in Low-power run mode*, *Table 34: Current consumption in Low-power sleep mode*,*Table 35: Typical and maximum current consumptions in Stop mode* and *Table 36: Typical and maximum current consumptions in Standby mode*. Added *Figure 12: IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSE, 1WS*, *Figure 13: IDD vs VDD, at TA= 25/55/85/105 °C, Run mode, code running from Flash memory, Range 2, HSI16, 1WS*, *Figure 14: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS*, *Figure 15: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive* and *Figure 16: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF*. Updated *Table 43: HSE oscillator characteristics* and *Table 44: LSE oscillator characteristics*. Added *Figure 21: HSI16 minimum and maximum value versus temperature*. Updated *Table 55: ESD absolute maximum ratings*, *Table 57: I/O current injection susceptibility*, *Table 58: I/O static characteristics*. Added *Figure 22: VIH/VIL versus VDD (CMOS I/Os)* and *Figure 23: VIH/VIL versus VDD (TTL I/Os)*. Updated *Table 59: Output voltage characteristics*, *Table 60: I/O AC characteristics* and *Figure 24: I/O AC characteristics definition*. Updated *Table 62: ADC characteristics*, *Table 64: ADC accuracy*, and *Figure 27: Typical connection diagram using the ADC*. Updated *Table 66: Temperature sensor calibration values*. Updated *Table 73: SPI characteristics in voltage Range 1* and *Table 76: I2S characteristics*. Added *Figure 46: Thermal resistance*.

Table 87. Document revision history (continued)

Date	Revision	Changes
08-Sep-2015	5	Updated all pinout/ballout schematics to highlight pin/ball supplied through VDD_USB. Updated current consumption in Run mode in *Section : Features*. Renamed BOOT1 into nBOOT1. Changed USARTx_RTS into USARTx_RTS_DE and LPUARTx_RTS into LPUARTx_RTS_DE. Updated VLCD in *Section 3.12: Analog-to-digital converter (ADC)* ADC no more available in Low-power run and Low-power Sleep modes in *Table 4: Functionalities depending on the working mode (from Run/active down to standby)*. Updated *Figure 3: STM32L053x6/8 LQFP64 pinout - 10 x 10 mm*, *Figure 4: STM32L053x6/8 TFBGA64 ballout - 5x 5 mm* and *Figure 5: STM32L053x6/8 LQFP48 pinout - 7 x 7 mm*. Changed I/O structure for PC5 and modified E5 and E6 signals for TFBGA64 in *Table 15: STM32L053x6/8 pin definitions*. Added ΣI_{VDD_USB} and updated $\Sigma I_{IO(PIN)}$ in *Table 22: Current characteristics* Updated V_{DD_USB} in *Table 22: Current characteristics*. Changed temperature condition in *Table 7: Internal voltage reference measured values* and *Table 26: Embedded internal reference voltage calibration values*. Updated T_{Coeff} in *Table 27: Embedded internal reference voltage*. Added note related to Standby mode in *Table 39: Peripheral current consumption in Stop and Standby mode*. Updated *Figure 14: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS*, *Figure 15: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive* and *Figure 16: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF*. Updated *Table 40: Low-power mode wakeup timings*. Updated MSI oscillator temperature frequency drift in *Table 48: MSI oscillator characteristics*. Updated *Table 62: ADC characteristics*, *Table 54: EMI characteristics* and *Table 55: ESD absolute maximum ratings*. Added t_{UP_LDO} in *Table 62: ADC characteristics*. Updated *Table 57: I/O current injection susceptibility*, *Table 58: I/O static characteristics* (I_{lkg}) and *Table 60: I/O AC characteristics*. *Section : I2C interface characteristics*: updated introduction and *Table 71: I2C analog filter characteristics*. Updated *Figure 31: SPI timing diagram - slave mode and CPHA = 0*. Added *Section : Device marking for LQFP64*, updated *Figure 42: TFBGA64 marking example (package top view)* and *Figure 45: LQFP48 marking example (package top view)* as well as notes below schematics.