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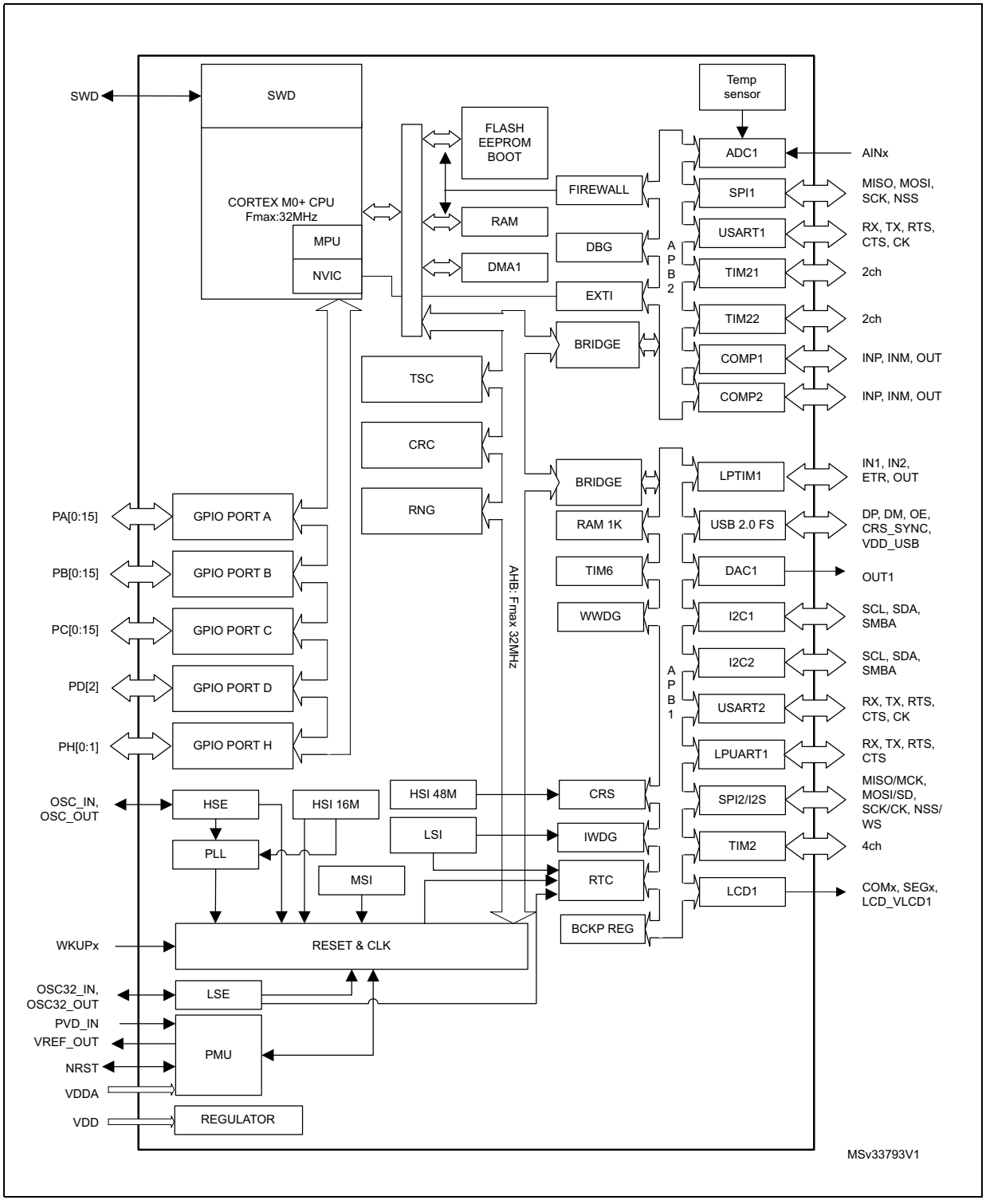
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	37
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l053c8t6d

Contents

Figure 1. STM32L053x6/8 block diagram



3 Functional overview

3.1 Low-power modes

The ultra-low-power STM32L053x6/8 support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply.

There are three power consumption ranges:

- Range 1 (V_{DD} range limited to 1.71-3.6 V), with the CPU running at up to 32 MHz
- Range 2 (full V_{DD} range), with a maximum CPU frequency of 16 MHz
- Range 3 (full V_{DD} range), with a maximum CPU frequency limited to 4.2 MHz

Seven low-power modes are provided to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. Sleep mode power consumption at 16 MHz is about 1 mA with all peripherals off.

- **Low-power run mode**

  This mode is achieved with the multispeed internal (MSI) RC oscillator set to the low-speed clock (max 131 kHz), execution from SRAM or Flash memory, and internal regulator in low-power mode to minimize the regulator's operating current. In Low-power run mode, the clock frequency and the number of enabled peripherals are both limited.

- **Low-power sleep mode**

  This mode is achieved by entering Sleep mode with the internal voltage regulator in low-power mode to minimize the regulator's operating current. In Low-power sleep mode, both the clock frequency and the number of enabled peripherals are limited; a typical example would be to have a timer running at 32 kHz.

  When wakeup is triggered by an event or an interrupt, the system reverts to the Run mode with the regulator on.

  Stop mode with RTC

  The Stop mode achieves the lowest power consumption while retaining the RAM and register contents and real time clock. All clocks in the V_{CORE} domain are stopped, the PLL, MSI RC, HSE crystal and HSI RC oscillators are disabled. The LSE or LSI is still running. The voltage regulator is in the low-power mode.

  Some peripherals featuring wakeup capability can enable the HSI RC during Stop mode to detect their wakeup condition.

  The device can be woken up from Stop mode by any of the EXTI line, in 3.5 µs, the processor can serve the interrupt or resume the code. The EXTI line source can be any GPIO. It can be the PVD output, the comparator 1 event or comparator 2 event (if internal reference voltage is on), it can be the RTC alarm/tamper/timestamp/wakeup events, the USB/USART/I2C/LPUART/LPTIMER wakeup events.

Table 2. Functionalities depending on the operating power supply range

Operating power supply range	Functionalities depending on the operating power supply range			
	DAC and ADC operation	Dynamic voltage scaling range	I/O operation	USB
V_{DD} = 1.65 to 1.71 V	ADC only, conversion time up to 570 ksps	Range 2 or range 3	Degraded speed performance	Not functional
V_{DD} = 1.71 to 1.8 V(1)	ADC only, conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Degraded speed performance	Functional(2)
V_{DD} = 1.8 to 2.0 V(1)	Conversion time up to 1.14 Msps	Range1, range 2 or range 3	Degraded speed performance	Functional(2)
V_{DD} = 2.0 to 2.4 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation	Functional(2)
V_{DD} = 2.4 to 3.6 V	Conversion time up to 1.14 Msps	Range 1, range 2 or range 3	Full speed operation	Functional(2)

1. CPU frequency changes from initial to final must respect "fcpu initial <4*fcpu final". It must also respect 5 µs delay between two changes. For example to switch from 4.2 MHz to 32 MHz, you can switch from 4.2 MHz to 16 MHz, wait 5 µs, then switch from 16 MHz to 32 MHz.
2. To be USB compliant from the I/O voltage standpoint, the minimum V_{DD_USB} is 3.0 V.

Table 3. CPU frequency range depending on dynamic voltage scaling

CPU frequency range	Dynamic voltage scaling range
16 MHz to 32 MHz (1ws) 32 kHz to 16 MHz (0ws)	Range 1
8 MHz to 16 MHz (1ws) 32 kHz to 8 MHz (0ws)	Range 2
32 kHz to 4.2 MHz (0ws)	Range 3

3.2 Interconnect matrix

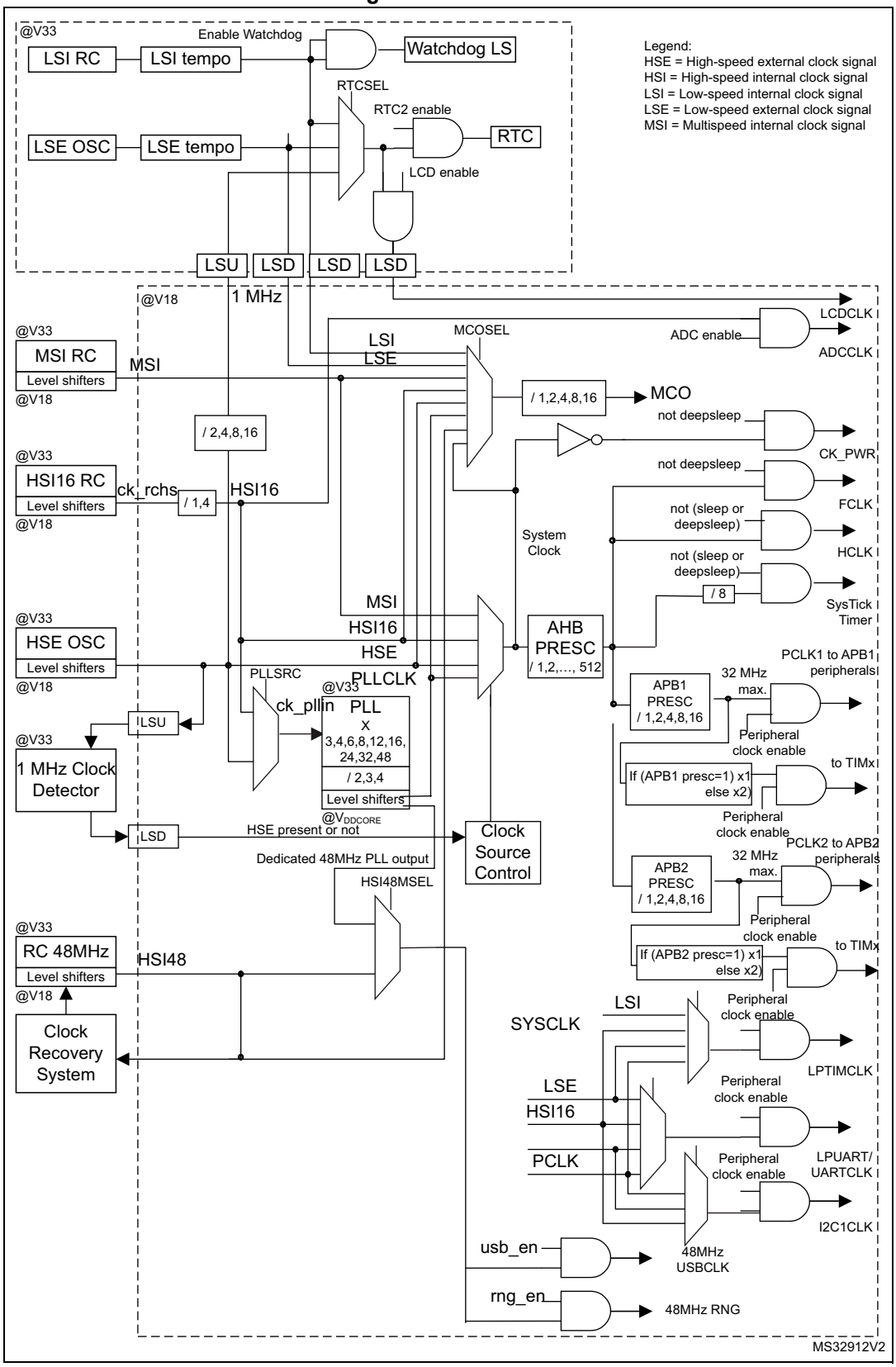
Several peripherals are directly interconnected. This allows autonomous communication between peripherals, thus saving CPU resources and power consumption. In addition, these hardware connections allow fast and predictable latency.

Depending on peripherals, these interconnections can operate in Run, Sleep, Low-power run, Low-power sleep and Stop modes.

Table 5. STM32L0xx peripherals interconnect matrix

Interconnect source	Interconnect destination	Interconnect action	Run	Sleep	Low-power run	Low-power sleep	Stop
COMPx	TIM2,TIM21, TIM22	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	-
	LPTIM	Timer input channel, trigger from analog signals comparison	Y	Y	Y	Y	Y
TIMx	TIMx	Timer triggered by other timer	Y	Y	Y	Y	-
RTC	TIM21	Timer triggered by Auto wake-up	Y	Y	Y	Y	-
	LPTIM	Timer triggered by RTC event	Y	Y	Y	Y	Y
All clock source	TIMx	Clock source used as input channel for RC measurement and trimming	Y	Y	Y	Y	-
USB	CRS/HSI48	the clock recovery system trims the HSI48 based on USB SOF	Y	Y	-	-	-
GPIO	TIMx	Timer input channel and trigger	Y	Y	Y	Y	-
	LPTIM	Timer input channel and trigger	Y	Y	Y	Y	Y
	ADC,DAC	Conversion trigger	Y	Y	Y	Y	-

Figure 2. Clock tree



3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 28 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 51 GPIOs can be connected to the 16 configurable interrupt/event lines. The 12 other lines are connected to PVD, RTC, USB, USARTs, LPUART, LPTIMER or comparator events.

3.8 Memories

The STM32L053x6/8 devices have the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states. With the enhanced bus matrix, operating the RAM does not lead to any performance penalty during accesses to the system bus (AHB and APB buses).
- The non-volatile memory is divided into three arrays:
  - 32 or 64 Kbytes of embedded Flash program memory
  - 2 Kbytes of data EEPROM
  - Information block containing 32 user and factory options bytes plus 4 Kbytes of system memory

The user options bytes are used to write-protect or read-out protect the memory (with 4 Kbyte granularity) and/or readout-protect the whole memory with the following options:

- **Level 0**: no protection
- **Level 1**: memory readout protected.

  The Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- **Level 2**: chip readout protected, debug features (Cortex-M0+ serial wire) and boot in RAM selection disabled (debugline fuse)

The firewall protects parts of code/data from access by the rest of the code that is executed outside of the protected area. The granularity of the protected code segment or the non-volatile data segment is 256 bytes (Flash memory or EEPROM) against 64 bytes for the volatile data segment (RAM).

The whole non-volatile memory embeds the error correction code (ECC) feature.

3.9 Boot modes

At startup, BOOT0 pin and nBOOT1 option bit are used to select one of three boot options:

- Boot from Flash memory
- Boot from System memory
- Boot from embedded RAM

The boot loader is located in System memory. It is used to reprogram the Flash memory by using SPI1(PA4, PA5, PA6, PA7) or SPI2 (PB12, PB13, PB14, PB15), USART1(PA9, PA10) or USART2(PA2, PA3). See STM32™ microcontroller system memory boot mode AN2606 for details.

3.13.2 V_{LCD} voltage monitoring

This embedded hardware feature allows the application to measure the V_{LCD} supply voltage using the internal ADC channel ADC_IN16. As the V_{LCD} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the ADC input is connected to LCD_VLCD2 (which provides $1/3V_{LCD}$ when the LCD is configured 1/3Bias and $1/4V_{LCD}$ when the LCD is configured 1/4Bias or 1/2Bias).

3.14 Digital-to-analog converter (DAC)

One 12-bit buffered DAC can be used to convert digital signal into analog voltage signal output. An optional amplifier can be used to reduce the output signal impedance.

This digital Interface supports the following features:

- One data holding register
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- DMA capability (including the underrun interrupt)
- External triggers for conversion
- Input reference voltage V_{REF+}

Four DAC trigger inputs are used in the STM32L053x6/8. The DAC channel is triggered through the timer update outputs that are also connected to different DMA channels.

3.15 Ultra-low-power comparators and reference voltage

The STM32L053x6/8 embed two comparators sharing the same current bias and reference voltage. The reference voltage can be internal or external (coming from an I/O).

- One comparator with ultra low consumption
- One comparator with rail-to-rail inputs, fast or slow mode.
- The threshold can be one of the following:
  - DAC output
  - External I/O pins
  - Internal reference voltage (V_{REFINT})
  - submultiple of Internal reference voltage(1/4, 1/2, 3/4) for the rail to rail comparator.

Both comparators can wake up the devices from Stop mode, and be combined into a window comparator.

The internal reference voltage is available externally via a low-power / low-current output buffer (driving current capability of 1 µA typical).

Table 14. Legend/abbreviations used in the pinout table (continued)

Name		Abbreviation	Definition
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 15. STM32L053x6/8 pin definitions

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64						
1	1	B2	VLCD	S	-	-	-	-
2	2	A2	PC13	I/O	FT	-	-	RTC_TAMP1/RTC_TS/RTC_OUT/WKUP2
3	3	A1	PC14-OSC32_IN (PC14)	I/O	FT	-	-	OSC32_IN
4	4	B1	PC15-OSC32_OUT (PC15)	I/O	TC	-	-	OSC32_OUT
5	5	C1	PH0-OSC_IN (PH0)	I/O	TC	-	USB_CRS_SYNC	OSC_IN
6	6	D1	PH1-OSC_OUT (PH1)	I/O	TC	-	-	OSC_OUT
7	7	E1	NRST	I/O	RST	-	-	-
-	8	E3	PC0	I/O	FT	-	LPTIM1_IN1, LCD_SEG18, EVENTOUT, TSC_G7_IO1	ADC_IN10
-	9	E2	PC1	I/O	FT	-	LPTIM1_OUT, LCD_SEG19, EVENTOUT, TSC_G7_IO2	ADC_IN11
-	10	F2	PC2	I/O	FT	-	LPTIM1_IN2, LCD_SEG20, SPI2_MISO/I2S2_MCK, TSC_G7_IO3	ADC_IN12
-	11	-	PC3	I/O	FT	-	LPTIM1_ETR, LCD_SEG21, SPI2_MOSI/I2S2_SD, TSC_G7_IO4	ADC_IN13

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.6 V (for the 1.65 V ≤V_{DD} ≤3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 7. Pin loading conditions

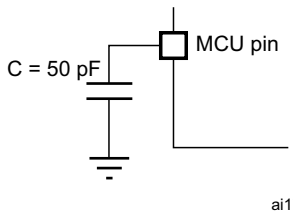


Figure 8. Pin input voltage

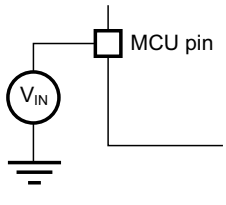


Table 22. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD} (2)	Total current into sum of all V_{DD} power lines (source)(1)	105	mA
ΣI_{VSS} (2)	Total current out of sum of all V_{SS} ground lines (sink)(1)	105	
ΣI_{VDD_USB}	Total current into V_{DD_USB} power lines (source)	25	
$I_{VDD(PIN)}$	Maximum current into each V_{DD} power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each V_{SS} ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin except FTf pins	16	
	Output current sunk by FTf pins	22	
	Output current sourced by any I/O and control pin	-16	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all IOs and control pins except PA11 and PA12(2)	90	
	Total output current sunk by PA11 and PA12	25	
	Total output current sourced by sum of all IOs and control pins(2)	-90	
$I_{INJ(PIN)}$	Injected current on FT, FTf, RST and B pins	-5/+0(3)	
	Injected current on TC pin	± 5(4)	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Positive current injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 21* for maximum allowed input voltage values.
4. A positive injection is induced by $V_{IN} > V_{DD}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 21: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 23. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 32. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	1 MHz	43.5	90	µA
				2 MHz	72	120	
				4 MHz	130	180	
			Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	4 MHz	160	210	
				8 MHz	305	370	
				16 MHz	590	710	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	370	430	
				16 MHz	715	860	
				32 MHz	1650	1900	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	18	65	
				524 kHz	31.5	75	
				4.2 MHz	140	210	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	16 MHz	665	830	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	1750	2100	
	Supply current in Sleep mode, Flash ON	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	1 MHz	57.5	130	
				2 MHz	84	170	
				4 MHz	150	280	
			Range 2, CORE=1.5 V, VOS[1:0]=10	4 MHz	170	310	
				8 MHz	315	420	
				16 MHz	605	770	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	380	460	
				16 MHz	730	950	
				32 MHz	1650	2400	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	29.5	110	
				524 kHz	44.5	130	
				4.2 MHz	150	270	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	16 MHz	680	950	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	1750	2100	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

Figure 14. I_{DD} vs V_{DD}, at T_A= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS

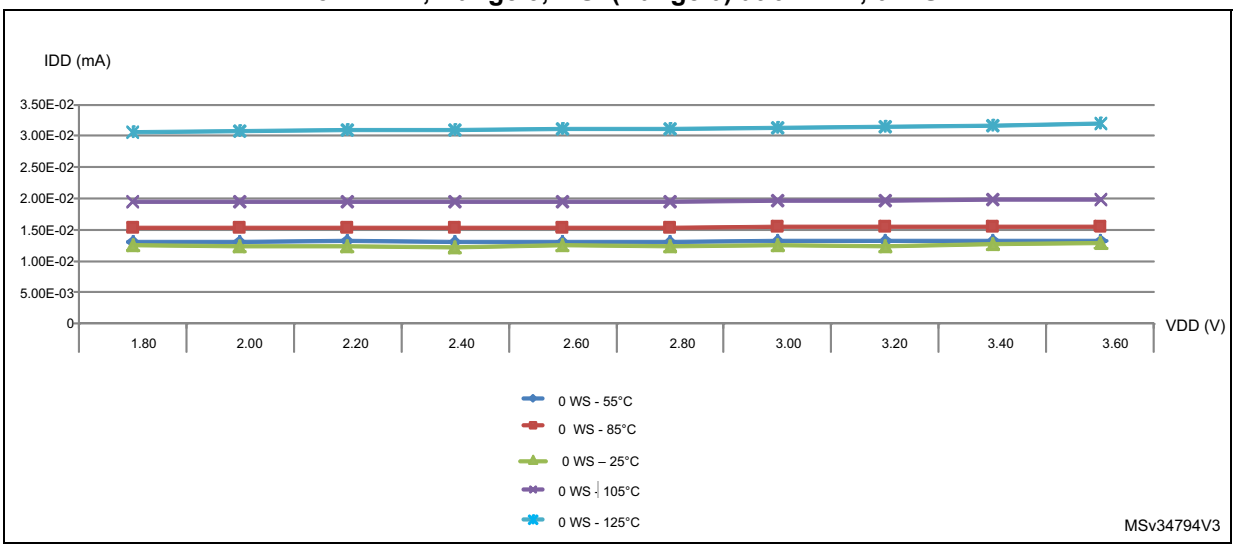


Table 34. Current consumption in Low-power sleep mode

Symbol	Parameter	Conditions			Typ	Max(1)	Unit
I_{DD} (LP Sleep)	Supply current in Low-power sleep mode	All peripherals OFF, V_{DD} from 1.65 to 3.6 V	MSI clock = 65 kHz, f_{HCLK} = 32 kHz, Flash OFF	T_A = − 40 to 25°C	4.7(2)	-	µA
			MSI clock = 65 kHz, f_{HCLK} = 32 kHz, Flash ON	T_A = − 40 to 25°C	17	23	
				T_A = 85 °C	19.5	63	
				T_A = 105 °C	23	69	
				T_A = 125 °C	32.5	90	
			MSI clock =65 kHz, f_{HCLK} = 65 kHz, Flash ON	T_A = − 40 to 25°C	17	23	
				T_A = 85 °C	20	63	
				T_A = 105 °C	23.5	69	
				T_A = 125 °C	32.5	90	
			MSI clock = 131 kHz, f_{HCLK} = 131 kHz, Flash ON	T_A = − 40 to 25°C	19.5	36	
				T_A = 55 °C	20.5	64	
				T_A = 85 °C	22.5	66	
				T_A = 105 °C	26	72	
				T_A = 125 °C	35	95	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. As the CPU is in Sleep mode, the difference between the current consumption with Flash ON and OFF (nearly 12 µA) is the same whatever the clock frequency.

Table 38. Peripheral current consumption in Run or Sleep mode(1) (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
Cortex-M0+ core I/O port	GPIOA	3.5	3	2.5	2.5	µA/MHz (f_{HCLK})
	GPIOB	3.5	2.5	2	2.5	
	GPIOC	8.5	6.5	5.5	7	
	GPIOD	1	0.5	0.5	0.5	
	GPIOH	1.5	1	1	0.5	
AHB	CRC	1.5	1	1	1	µA/MHz (f_{HCLK})
	FLASH	0(3)	0(3)	0(3)	0(3)	
	DMA1	10	8	6.5	8.5	
	RNG	5.5	1	0.5	0.5	
	TSC	3	2.5	2	3	
All enabled		283	225	222.5	212.5	µA/MHz (f_{HCLK})
PWR		2.5	2	2	1	µA/MHz (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is OFF for this measure.
3. Current consumption is negligible and close to 0 µA.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The simplified formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 63. R_{AIN} max for f_{ADC} = 16 MHz(1)

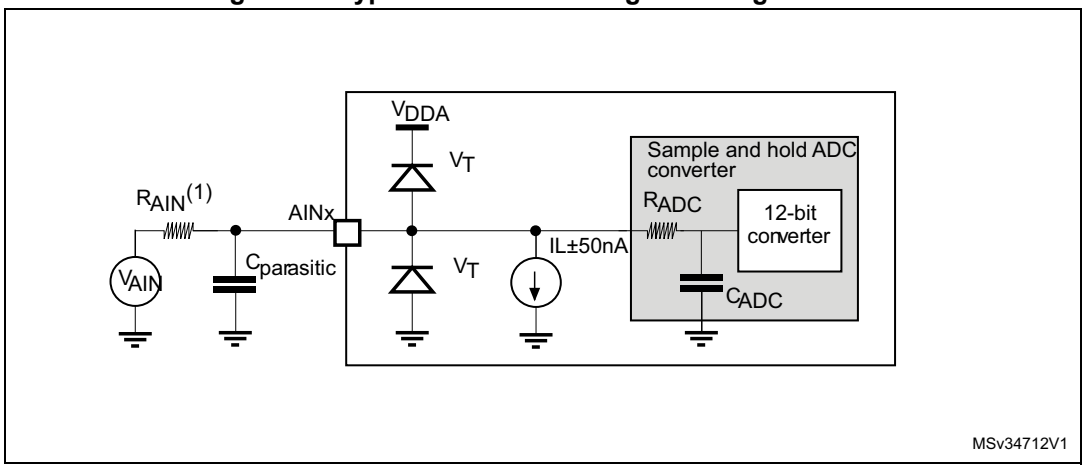
T_S (cycles)	t_S (µs)	R_{AIN} max for fast channels (kΩ)	R_{AIN} max for standard channels (kΩ)						
			V_{DD} > 2.7 V	V_{DD} > 2.4 V	V_{DD} > 2.0 V	V_{DD} > 1.8 V	V_{DD} > 1.75 V	V_{DD} > 1.65 V and T_A > -10 °C	V_{DD} > 1.65 V and T_A > 25 °C
1.5	0.09	0.5	< 0.1	NA	NA	NA	NA	NA	NA
3.5	0.22	1	0.2	< 0.1	NA	NA	NA	NA	NA
7.5	0.47	2.5	1.7	1.5	< 0.1	NA	NA	NA	NA
12.5	0.78	4	3.2	3	1	NA	NA	NA	NA
19.5	1.22	6.5	5.7	5.5	3.5	NA	NA	NA	< 0.1
39.5	2.47	13	12.2	12	10	NA	NA	NA	5
79.5	4.97	27	26.2	26	24	< 0.1	NA	NA	19
160.5	10.03	50	49.2	49	47	32	< 0.1	< 0.1	42

1. Guaranteed by design.

Table 64. ADC accuracy(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	1.65 V < V_{DDA} = V_{REF+} < 3.6 V, range 1/2/3	-	2	4	LSB
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	
EL	Integral linearity error		-	1.5	2.5	
ED	Differential linearity error		-	1	1.5	
ENOB	Effective number of bits		10.2	11		bits
	Effective number of bits (16-bit mode oversampling with ratio =256)(4)		11.3	12.1	-	
SINAD	Signal-to-noise distortion		63	69	-	dB
SNR	Signal-to-noise ratio		63	69	-	
	Signal-to-noise ratio (16-bit mode oversampling with ratio =256)(4)		70	76	-	
THD	Total harmonic distortion		-	-85	-73	

Figure 27. Typical connection diagram using the ADC

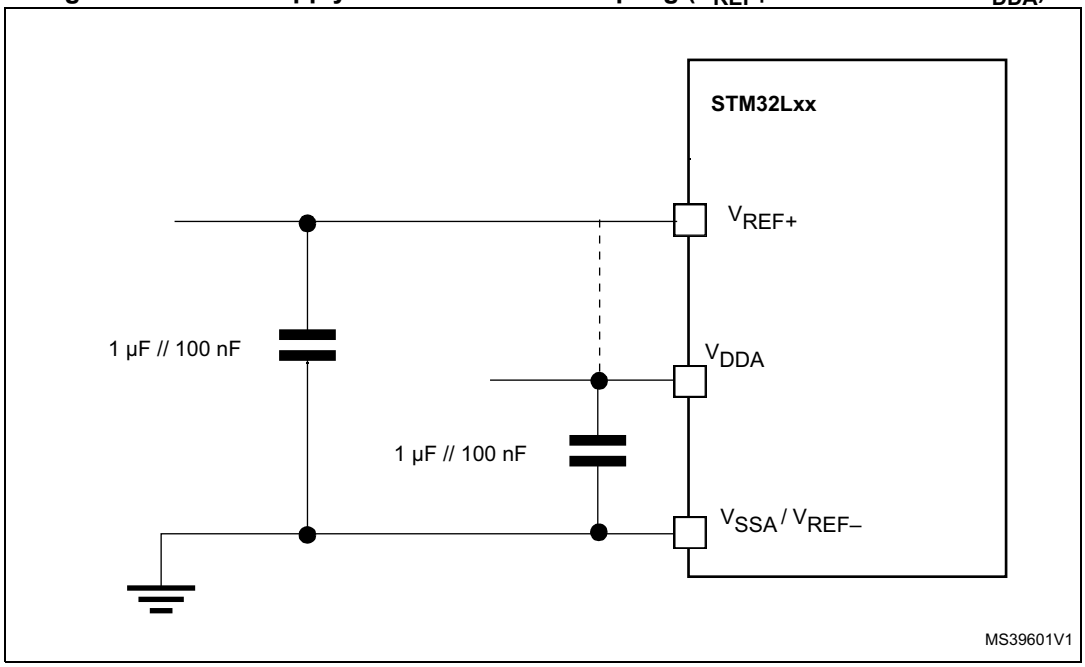


1. Refer to *Table 62: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 28* or *Figure 29*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 28. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



6.3.17 Temperature sensor characteristics

Table 66. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A - 0x1FF8 007B
TS_CAL2	TS ADC raw data acquired at temperature of 130 °C, V_{DDA}= 3 V	0x1FF8 007E - 0x1FF8 007F

Table 67. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	1.48	1.61	1.75	mV/°C
V_{130}	Voltage at 130°C ±5°C(2)	640	670	700	mV
$I_{DDA(TEMP)}$(3)	Current consumption	-	3.4	6	µA
t_{START}(3)	Startup time	-	-	10	µs
T_{S_temp}(4)(3)	ADC sampling time when reading the temperature	10	-	-	

1. Guaranteed by characterization results.
2. Measured at V_{DD} = 3 V ±10 mV. V130 ADC conversion result is stored in the TS_CAL2 byte.
3. Guaranteed by design.
4. Shortest sampling time can be determined in the application by multiple iterations.

6.3.18 Comparators

Table 68. Comparator 1 characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage	-	1.65		3.6	V
R_{400K}	R_{400K} value	-	-	400	-	kΩ
R_{10K}	R_{10K} value	-	-	10	-	
V_{IN}	Comparator 1 input voltage range	-	0.6	-	V_{DDA}	V
t_{START}	Comparator startup time	-	-	7	10	µs
td	Propagation delay(2)	-	-	3	10	
Voffset	Comparator offset	-	-	±3	±10	mV
$d_{Voffset}$/dt	Comparator offset variation in worst voltage stress conditions	V_{DDA} = 3.6 V, V_{IN+} = 0 V, V_{IN-} = V_{REFINT}, T_A = 25 °C	0	1.5	10	mV/1000 h
I_{COMP1}	Current consumption(3)	-	-	160	260	nA

1. Guaranteed by characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

6.3.19 Timer characteristics

TIM timer characteristics

The parameters given in the *Table 70* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 70. TIMx characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	16	MHz
Res_{TIM}	Timer resolution	-		16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM6, TIM21, and TIM22 timers.

6.3.20 Communications interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I^2C timing requirements are guaranteed by design when the I^2C peripheral is properly configured (refer to the reference manual for details). The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

All I^2C SDA and SCL I/Os embed an analog filter (see *Table 71* for the analog filter characteristics).