Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l053r8t3

- **Startup clock**

  After reset, the microcontroller restarts by default with an internal 2 MHz clock (MSI). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.

- **Clock security system (CSS)**

  This feature can be enabled by software. If an HSE clock failure occurs, the master clock is automatically switched to HSI and a software interrupt is generated if enabled.

  Another clock security system can be enabled, in case of failure of the LSE it provides an interrupt or wakeup event which is generated if enabled.

- **Clock-out capability (MCO: microcontroller clock output)**

  It outputs one of the internal clocks for external use by the application.

Several prescalers allow the configuration of the AHB frequency, each APB (APB1 and APB2) domains. The maximum frequency of the AHB and the APB domains is 32 MHz. See *Figure 2* for details on the clock tree.

3.6 Low-power real-time clock and backup registers

The real time clock (RTC) and the 5 backup registers are supplied in all modes including standby mode. The backup registers are five 32-bit registers used to store 20 bytes of user application data. They are not reset by a system reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month
- Two programmable alarms with wake up from Stop and Standby mode capability
- Periodic wakeup from Stop and Standby with programmable resolution and period
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 37 kHz)
- The high-speed external clock

3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions, and can be individually remapped using dedicated alternate function registers. All GPIOs are high current capable. Each GPIO output, speed can be slowed (40 MHz, 10 MHz, 2 MHz, 400 kHz). The alternate function configuration of I/Os can be locked if needed following a specific sequence in order to avoid spurious writing to the I/O registers. The I/O controller is connected to a dedicated IO bus with a toggling speed of up to 32 MHz.

Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 28 edge detector lines used to generate interrupt/event requests. Each line can be individually configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 51 GPIOs can be connected to the 16 configurable interrupt/event lines. The 12 other lines are connected to PVD, RTC, USB, USARTs, LPUART, LPTIMER or comparator events.

TIM21 and TIM22

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together and be synchronized with the TIM2, full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.18.2 Low-power Timer (LPTIM)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one shot mode
- Selectable software / hardware input trigger
- Selectable clock source
  - Internal clock source: LSE, LSI, HSI or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.18.3 Basic timer (TIM6)

This timer can be used as a generic 16-bit timebase. It is mainly used for DAC trigger generation.

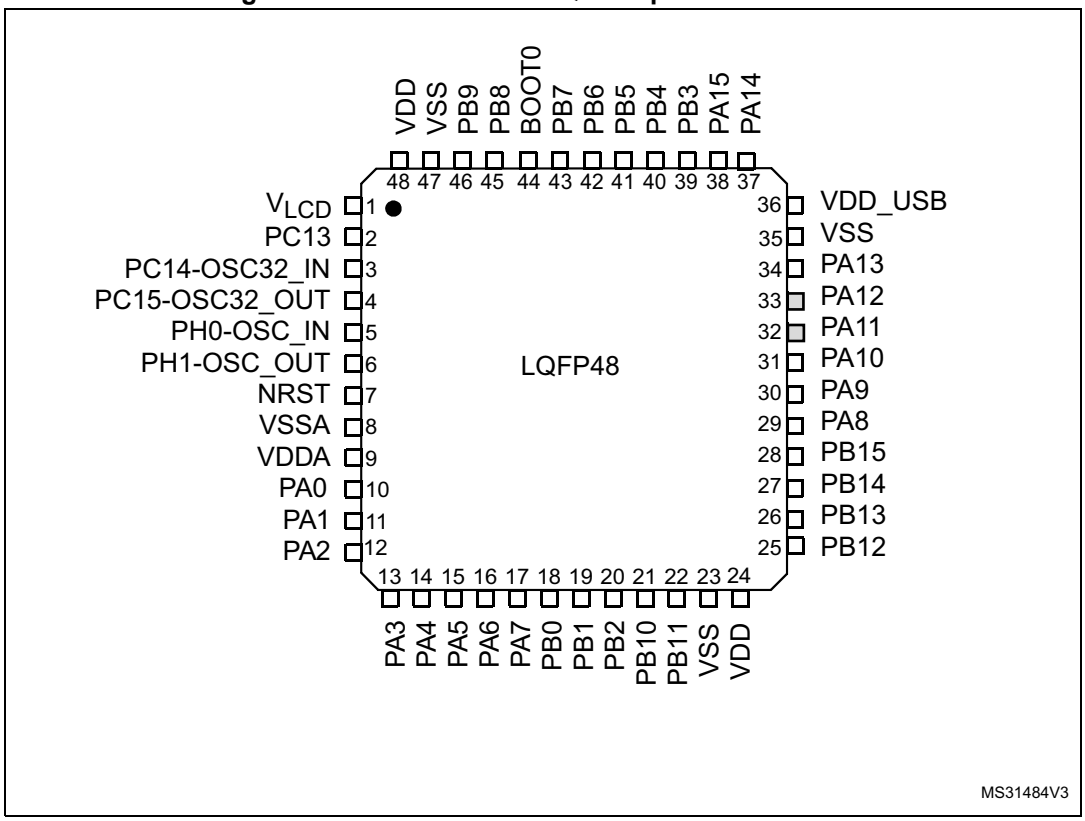
3.18.4 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches ‘0’.

3.18.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

Figure 5. STM32L053x6/8 LQFP48 pinout - 7 x 7 mm



1. The above figure shows the package top view.
2. I/O pin supplied by VDD_USB.

Table 14. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT	5 V tolerant I/O
	FTf	5 V tolerant I/O, FM+ capable
	TC	Standard 3.3V I/O
	B	Dedicated BOOT0 pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	

Table 15. STM32L053x6/8 pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64						
-	37	F6	PC6	I/O	FT	-	TIM22_CH1, LCD_SEG24, TSC_G8_IO1	-
-	38	E7	PC7	I/O	FT	-	TIM22_CH2, LCD_SEG25, TSC_G8_IO2	-
-	39	E8	PC8	I/O	FT	-	TIM22_ETR, LCD_SEG26, TSC_G8_IO3	-
-	40	D8	PC9	I/O	FT	-	TIM21_ETR, LCD_SEG27, USB_NOE, TSC_G8_IO4	-
29	41	D7	PA8	I/O	FT	-	MCO, LCD_COM0, USB_CRS_SYNC, EVENTOUT, USART1_CK	-
30	42	C7	PA9	I/O	FT	-	MCO, LCD_COM1, TSC_G4_IO1, USART1_TX	-
31	43	C6	PA10	I/O	FT	-	LCD_COM2, TSC_G4_IO2, USART1_RX	-
32	44	C8	PA11	I/O	FT	(2)	SPI1_MISO, EVENTOUT, TSC_G4_IO3, USART1_CTS, COMP1_OUT	USB_DM
33	45	B8	PA12	I/O	FT	(2)	SPI1_MOSI, EVENTOUT, TSC_G4_IO4, USART1_RTS_DE, COMP2_OUT	USB_DP
34	46	A8	PA13	I/O	FT	-	SWDIO, USB_NOE	-
35	47	D5	VSS	S		-	-	-
36	48	E6	VDD_USB	S		-	-	-
37	49	A7	PA14	I/O	FT	-	SWCLK, USART2_TX	-
38	50	A6	PA15	I/O	FT	-	SPI1_NSS, LCD_SEG17, TIM2_ETR, EVENTOUT, USART2_RX, TIM2_CH1	-
-	51	B7	PC10	I/O	FT	-	LPUART1_TX, LCD_COM4/LCD_SEG28/ LCD_SEG40	-

Table 17. Alternate function port B

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6
		SPI1/SPI2/I2S2/ USART1/ EVENTOUT/	I2C1/LCD	LPUART1/LPTIM /TIM2/SYS_AF/ EVENTOUT	I2C1/TSC	I2C1/TIM22/ EVENTOUT/ LPUART1	SPI2/I2S2/I2C2	I2C2/TIM21/ EVENTOUT
Port B	PB0	EVENTOUT	LCD_SEG5	-	TSC_G3_IO2	-	-	-
	PB1	-	LCD_SEG6	-	TSC_G3_IO3	LPUART1_RTS_ DE	-	-
	PB2	-	-	LPTIM1_OUT	TSC_G3_IO4	-	-	-
	PB3	SPI1_SCK	LCD_SEG7	TIM2_CH2	TSC_G5I_O1	EVENTOUT	-	-
	PB4	SPI1_MISO	LCD_SEG8	EVENTOUT	TSC_G5_IO2	TIM22_CH1	-	-
	PB5	SPI1_MOSI	LCD_SEG9	LPTIM1_IN1	I2C1_SMBA	TIM22_CH2	-	-
	PB6	USART1_TX	I2C1_SCL	LPTIM1_ETR	TSC_G5_IO3	-	-	-
	PB7	USART1_RX	I2C1_SDA	LPTIM1_IN2	TSC_G5_IO4	-	-	-
	PB8	-	LCD_SEG16	-	TSC_SYNC	I2C1_SCL	-	-
	PB9	-	LCD_COM3	EVENTOUT	-	I2C1_SDA	SPI2_NSS/I2S2_ WS	-
	PB10	-	LCD_SEG10	TIM2_CH3	TSC_SYNC	LPUART1_TX	SPI2_SCK	I2C2_SCL
	PB11	EVENTOUT	LCD_SEG11	TIM2_CH4	TSC_G6_IO1	LPUART1_RX	-	I2C2_SDA
	PB12	SPI2_NSS/I2S2_WS	LCD_SEG12	LPUART1_RTS_ DE	TSC_G6_IO2	-	I2C2_SMBA	EVENTOUT
	PB13	SPI2_SCK/I2S2_CK	LCD_SEG13	-	TSC_G6_IO3	LPUART1_CTS	I2C2_SCL	TIM21_CH1
	PB14	SPI2_MISO/I2S2_MCK	LCD_SEG14	RTC_OUT	TSC_G6_IO4	LPUART1_RTS_ DE	I2C2_SDA	TIM21_CH2
	PB15	SPI2_MOSI/I2S2_SD	LCD_SEG15	RTC_REFIN	-	-	-	-

2. V_{DD_USB} must respect the following conditions:

- When V_{DD} is powered-on ($V_{DD} < V_{DD\_min}$), V_{DD_USB} should be always lower than V_{DD}.
- When V_{DD} is powered-down ($V_{DD} < V_{DD\_min}$), V_{DD_USB} should be always lower than V_{DD}.
- In operating mode, V_{DD_USB} could be lower or higher V_{DD}.
- If the USB is not used, V_{DD_USB} must range from V_{DD_min} to V_{DD_max} to be able to use PA11 and PA12 as standard I/Os.

3. To sustain a voltage higher than V_{DD}+0.3V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_J max (see *Table 85: Thermal characteristics on page 123*).

Table 35. Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
I_{DD} (Stop)	Supply current in Stop mode	T_A = − 40 to 25°C	0.41	1	µA
		T_A = 55°C	0.63	2.1	
		T_A= 85°C	1.7	4.5	
		T_A = 105°C	4	9.6	
		T_A = 125°C	11	24(2)	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Guaranteed by test in production.

Figure 15. I_{DD} vs V_{DD}, at T_A= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive

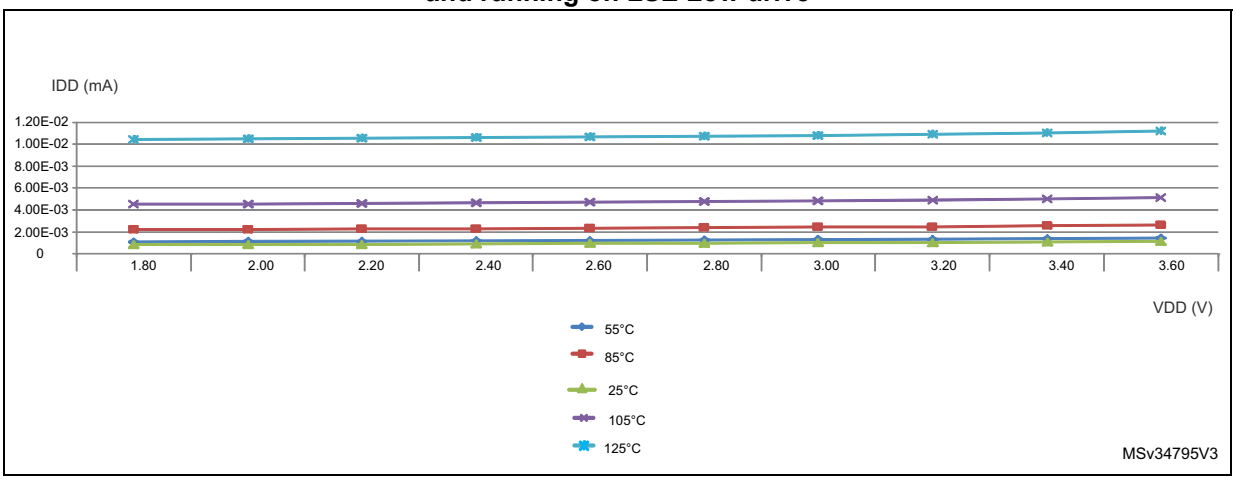


Figure 16. I_{DD} vs V_{DD}, at T_A= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF

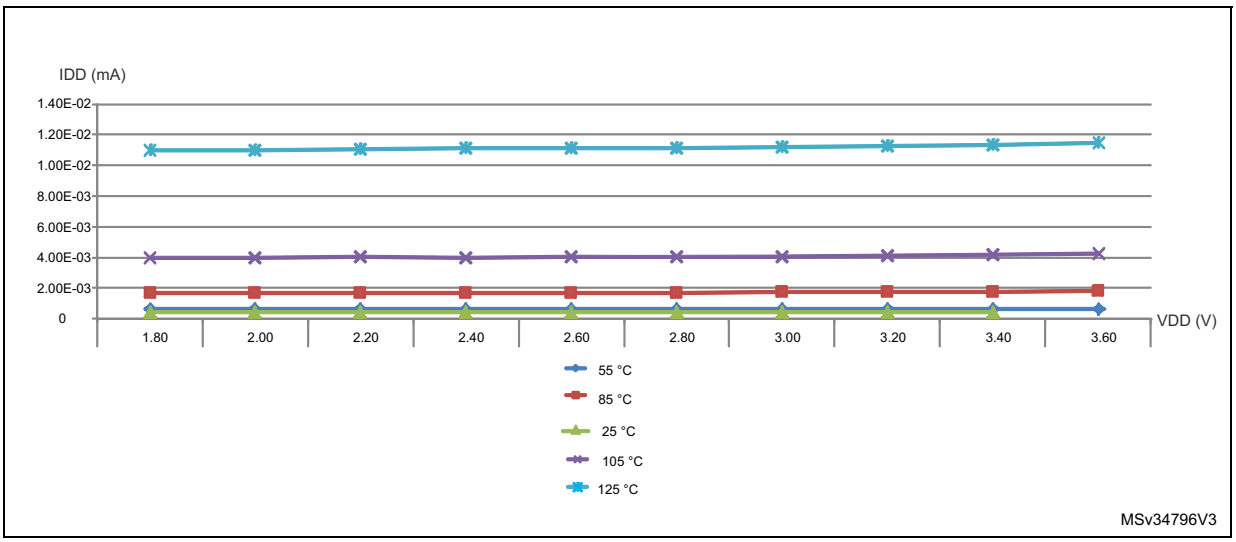


Table 38. Peripheral current consumption in Run or Sleep mode(1) (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
Cortex-M0+ core I/O port	GPIOA	3.5	3	2.5	2.5	µA/MHz (f_{HCLK})
	GPIOB	3.5	2.5	2	2.5	
	GPIOC	8.5	6.5	5.5	7	
	GPIOD	1	0.5	0.5	0.5	
	GPIOH	1.5	1	1	0.5	
AHB	CRC	1.5	1	1	1	µA/MHz (f_{HCLK})
	FLASH	0(3)	0(3)	0(3)	0(3)	
	DMA1	10	8	6.5	8.5	
	RNG	5.5	1	0.5	0.5	
	TSC	3	2.5	2	3	
All enabled		283	225	222.5	212.5	µA/MHz (f_{HCLK})
PWR		2.5	2	2	1	µA/MHz (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is OFF for this measure.
3. Current consumption is negligible and close to 0 µA.

Table 48. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤T_A ≤85 °C	-	±3	-	%
	MSI oscillator frequency drift V_{DD} = 3.3 V, − 40 °C ≤T_A ≤110 °C	MSI range 0	− 8.9	+7.0	
		MSI range 1	− 7.1	+5.0	
		MSI range 2	− 6.4	+4.0	
		MSI range 3	− 6.2	+3.0	
		MSI range 4	− 5.2	+3.0	
		MSI range 5	− 4.8	+2.0	
		MSI range 6	− 4.7	+2.0	
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤V_{DD} ≤3.6 V, T_A = 25 °C	-	-	2.5	%/V
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	

Table 48. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
$t_{STAB(MSI)}$(2)	MSI oscillator stabilization time	MSI range 0	-	40	µs
		MSI range 1	-	20	
		MSI range 2	-	10	
		MSI range 3	-	4	
		MSI range 4	-	2.5	
		MSI range 5	-	2	
		MSI range 6, Voltage range 1 and 2	-	2	
		MSI range 3, Voltage range 3	-	3	
$f_{OVER(MSI)}$	MSI oscillator frequency overshoot	Any range to range 5	-	4	MHz
		Any range to range 6	-	6	

1. This is a deviation for an individual part, once the initial frequency has been measured.
2. Guaranteed by characterization results.

6.3.8 PLL characteristics

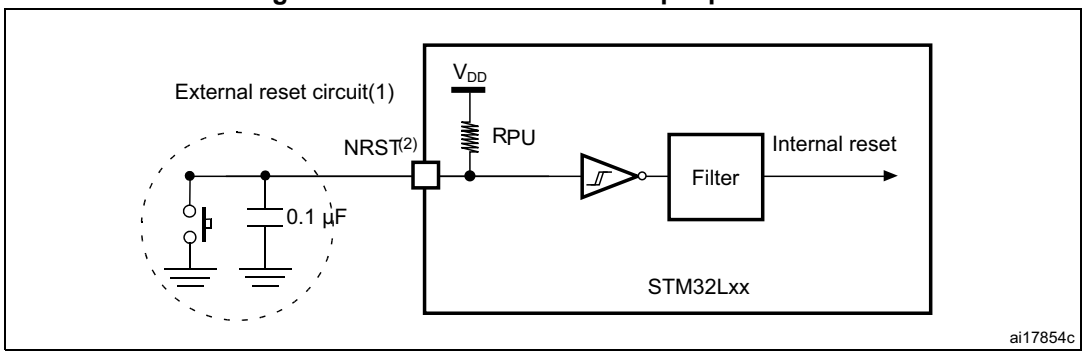
The parameters given in *Table 49* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 24*.

Table 49. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	2	-	24	MHz
	PLL input clock duty cycle	45	-	55	%
f_{PLL_OUT}	PLL output clock	2	-	32	MHz
t_{LOCK}	PLL input = 16 MHz PLL VCO = 96 MHz	-	115	160	µs
Jitter	Cycle-to-cycle jitter	-		±600	ps
I_{DDA}(PLL)	Current consumption on V_{DDA}	-	220	450	µA
I_{DD}(PLL)	Current consumption on V_{DD}	-	120	150	

1. Guaranteed by characterization results.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

Figure 25. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The external capacitor must be placed as close as possible to the device.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 61*. Otherwise the reset will not be taken into account by the device.

6.3.15 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 62* are derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 24: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 62. ADC characteristics

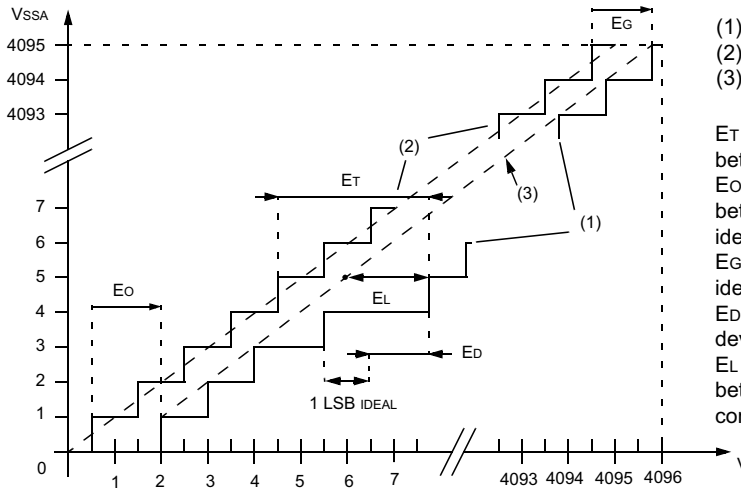
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	Fast channel	1.65	-	3.6	V
		Standard channel	1.75(1)	-	3.6	
V_{REF+}	Positive reference voltage	-	1.65		V_{DDA}	V
$I_{DDA\ (ADC)}$	Current consumption of the ADC on $V_{DDA}$and V_{REF+}	1.14 Msps	-	200	-	µA
		10 ksps	-	40	-	
	Current consumption of the ADC on V_{DD}(2)	1.14 Msps	-	70	-	
		10 ksps	-	1	-	
f_{ADC}	ADC clock frequency	Voltage scaling Range 1	0.14	-	16	MHz
		Voltage scaling Range 2	0.14	-	8	
		Voltage scaling Range 3	0.14	-	4	
f_S(3)	Sampling rate	12-bit resolution	0.01	-	1.14	MHz
f_{TRIG}(3)	External trigger frequency	f_{ADC} = 16 MHz, 12-bit resolution	-	-	941	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{REF+}	V
R_{AIN}(3)	External input impedance	See *Equation 1* and *Table 63* for details	-	-	50	kΩ
R_{ADC}(3)(4)	Sampling switch resistance	-	-	-	1	kΩ

Table 64. ADC accuracy(1)(2)(3) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	1.65 V < V_{REF+} < V_{DDA} < 3.6 V, range 1/2/3	-	2	5	LSB
EO	Offset error		-	1	2.5	
EG	Gain error		-	1	2	
EL	Integral linearity error		-	1.5	3	
ED	Differential linearity error		-	1	2	
ENOB	Effective number of bits		10.0	11.0	-	bits
SINAD	Signal-to-noise distortion		62	69	-	dB
SNR	Signal-to-noise ratio		61	69	-	
THD	Total harmonic distortion		-	-85	-65	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.12* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. This number is obtained by the test board without additional noise, resulting in non-optimized value for oversampling mode.

Figure 26. ADC accuracy characteristics



(1) Example of an actual transfer curve
(2) The ideal transfer curve
(3) End point correlation line

E_T = Total Unajusted Error: maximum deviation between the actual and ideal transfer curves.
E_O = Offset Error: maximum deviation between the first actual transition and the first ideal one.
E_G = Gain Error: deviation between the last ideal transition and the last actual one.
E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal ones.
E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

MS19880V2

Table 65. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL(2)	Differential non linearity(4)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	1.5	3	LSB
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	1.5	3	
INL(2)	Integral non linearity(5)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	2	4	
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	2	4	
Offset(2)	Offset error at code 0x800 (6)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	±10	±25	
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	±5	±8	
Offset1(2)	Offset error at code 0x001(7)	No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	±1.5	±5	
dOffset/dT(2)	Offset error temperature coefficient (code 0x800)	V_{DDA} = 3.3V V_{REF+}= 3.0 V T_A = 0 to 50 °C DAC output buffer OFF	-20	-10	0	µV/°C
		V_{DDA} = 3.3V V_{REF+}= 3.0 V T_A = 0 to 50 °C DAC output buffer ON	0	20	50	
Gain(2)	Gain error(8)	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	+0.1 / -0.2%	+0.2 / -0.5%	%
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	+0 / -0.2%	+0 / -0.4%	
dGain/dT(2)	Gain error temperature coefficient	V_{DDA} = 3.3V V_{REF+}= 3.0 V T_A = 0 to 50 °C DAC output buffer OFF	-10	-2	0	µV/°C
		V_{DDA} = 3.3V V_{REF+}= 3.0 V T_A = 0 to 50 °C DAC output buffer ON	-40	-8	0	
TUE(2)	Total unadjusted error	$C_L \leq 50$ pF, $R_L \geq 5$ kΩ DAC output buffer ON	-	12	30	LSB
		No R_{LOAD}, $C_L \leq 50$ pF DAC output buffer OFF	-	8	12	

I2S characteristics

Table 76. I2S characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 x 8K	256xFs (2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	15	ns
$t_{h(WS)}$	WS hold time	Master mode	11	-	
$t_{su(WS)}$	WS setup time	Slave mode	6	-	
$t_{h(WS)}$	WS hold time	Slave mode	2	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	0	-	
$t_{su(SD\_SR)}$		Slave receiver	6.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	18	-	
$t_{h(SD\_SR)}$		Slave receiver	15.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	77	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	8	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	18	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	1.5	-	

1. Guaranteed by characterization results.
2. 256xFs maximum value is equal to the maximum clock frequency.

*Note: Refer to the I2S section of the product reference manual for more details about the sampling frequency (Fs), f_{MCK}, f_{CK} and D_{CK} values. These values reflect only the digital peripheral behavior, source clock precision might slightly change them. DCK depends mainly on the ODD bit value, digital contribution leads to a min of (I2SDIV/(2*I2SDIV+ODD) and a max of (I2SDIV+ODD)/(2*I2SDIV+ODD). Fs max is supported for each mode/condition.*

Table 80. LCD controller characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit
I_{LCD}(1)	Supply current at V_{DD} = 2.2 V	-	3.3	-	µA
	Supply current at V_{DD} = 3.0 V	-	3.1	-	
R_{Htot}(2)	Low drive resistive network overall value	5.28	6.6	7.92	MΩ
R_L(2)	High drive resistive network total value	192	240	288	kΩ
V_{44}	Segment/Common highest level voltage	-	-	V_{LCD}	V
V_{34}	Segment/Common 3/4 level voltage	-	3/4 V_{LCD}	-	V
V_{23}	Segment/Common 2/3 level voltage	-	2/3 V_{LCD}	-	
V_{12}	Segment/Common 1/2 level voltage	-	1/2 V_{LCD}	-	
V_{13}	Segment/Common 1/3 level voltage	-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage	-	1/4 V_{LCD}	-	
V_0	Segment/Common lowest level voltage	0	-	-	
ΔVxx(3)	Segment/Common level voltage error T_A = -40 to 85 °C	-	-	±50	mV

1. LCD enabled with 3 V internal step-up active, 1/8 duty, 1/4 bias, division ratio= 64, all pixels active, no LCD connected.
2. Guaranteed by design.
3. Guaranteed by characterization results.

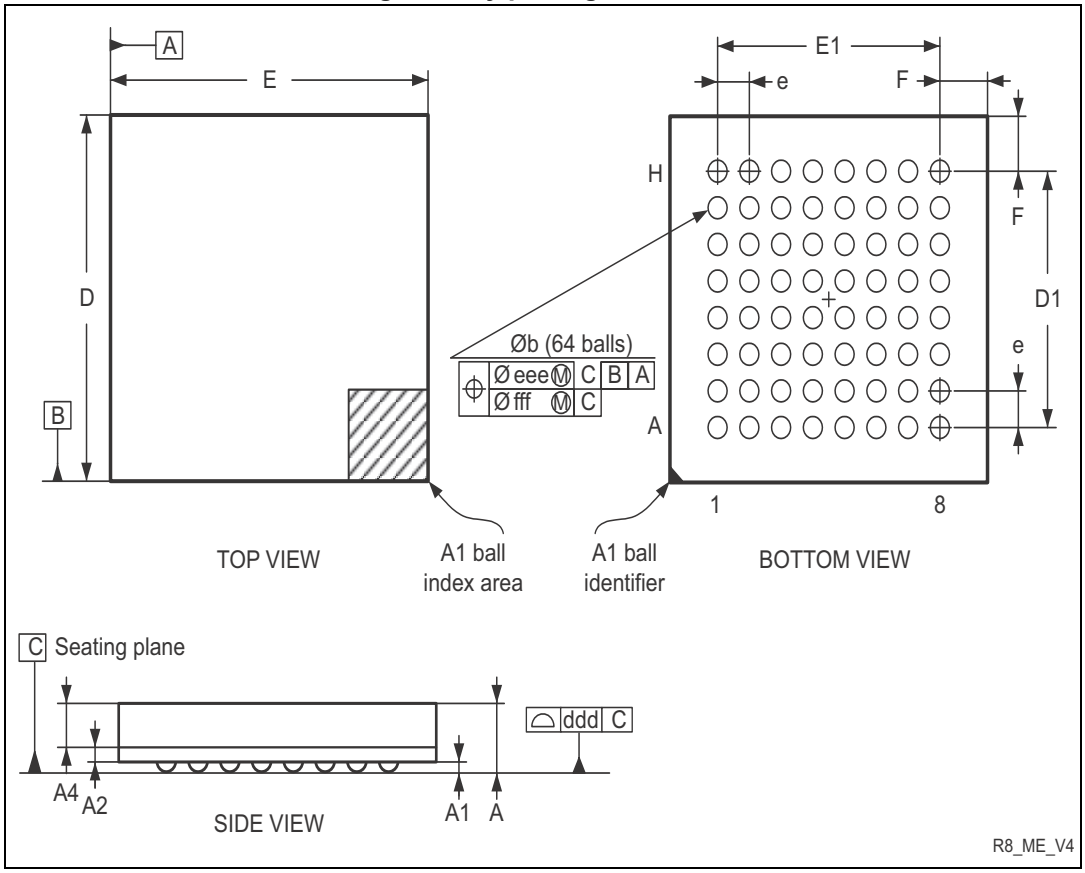
Table 81. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 TFBGA64 package information

Figure 40. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch thin profile fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 82. TFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch, thin profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.200	-	-	0.0472
A1	0.150	-	-	0.0059	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.600	-	-	0.0236
b	0.250	0.300	0.350	0.0098	0.0118	0.0138
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	-	3.500	-	-	0.1378	-
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	-	3.500	-	-	0.1378	-

7.4.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Table 87. Document revision history (continued)

Date	Revision	Changes
05-Sep-2014	4	Extended operating temperature range to 125 °C. Updated minimum ADC operating voltage to 1.65 V. Replaced USART3 by LPUART1 in *Table 15: STM32L053x6/8 pin definitions* and LPUART by LPUART1 in *Table 16: Alternate function port A*, *Table 17: Alternate function port B*, *Table 18: Alternate function port C*, *Table 19: Alternate function port D* and *Table 20: Alternate function port H*. Updated PA6 in *Table 16: Alternate function port A*. Updated temperature range in *Section 2: Description*, *Table 1: Ultra-low-power STM32L053x6/x8 device features and peripheral counts*. Updated P_D, $T_{A\ and}$ T_J to add range 3 in *Table 24: General operating conditions*. Added range 3 in *Table 51: Flash memory and data EEPROM characteristics*, *Table 52: Flash memory and data EEPROM endurance and retention*. Update note 1 in *Table 28: Current consumption in Run mode, code with data processing running from Flash*, *Table 30: Current consumption in Run mode, code with data processing running from RAM*, *Table 32: Current consumption in Sleep mode*, *Table 33: Current consumption in Low-power run mode*, *Table 34: Current consumption in Low-power sleep mode*, *Table 35: Typical and maximum current consumptions in Stop mode*, *Table 36: Typical and maximum current consumptions in Standby mode* and *Table 40: Low-power mode wakeup timings*. Updated *Figure 46: Thermal resistance* and removed note 1. Updated *Figure 14: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Low-power run mode, code running from RAM, Range 3, MSI (Range 0) at 64 KHz, 0 WS*, *Figure 15: IDD vs VDD, at TA= 25/55/ 85/105/125 °C, Stop mode with RTC enabled and running on LSE Low drive*, *Figure 16: IDD vs VDD, at TA= 25/55/85/105/125 °C, Stop mode with RTC disabled, all clocks OFF*. Updated *Table 36: Typical and maximum current consumptions in Standby mode*. Updated SYSCFG in *Table 38: Peripheral current consumption in Run or Sleep mode*. Updated *Table 39: Peripheral current consumption in Stop and Standby mode* and *Table 40: Low-power mode wakeup timings*. Updated ACC_{HSI16} temperature conditions in *Table 45: 16 MHz HSI16 oscillator characteristics*. Changed ambient temperature range in note 1 below *Table 46: HSI48 oscillator characteristics*. Updated $V_{F(NRST)}$ and $V_{NF(NRST)}$ in *Table 61: NRST pin characteristics*. Updated *Table 62: ADC characteristics* and *Table 64: ADC accuracy*. Added range 3 in *Table 86: STM32L053x6/8 ordering information scheme*.