Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l053r8t6d

2.1 Device overview

Table 1. Ultra-low-power STM32L053x6/x8 device features and peripheral counts

Peripheral		STM32L053C6	STM32L053R6	STM32L053C8	STM32L053R8
Flash (Kbytes)		32		64	
Data EEPROM (Kbytes)		2		2	
RAM (Kbytes)		8		8	
Timers	General-purpose	3		3	
	Basic	1		1	
	LPTIMER	1		1	
RTC/SYSTICK/IWDG/WWDG		1/1/1/1		1/1/1/1	
Communication interfaces	SPI/I2S	4(2)[1]/1		4(2)[1]/1	
	I^2C	2		2	
	USART	2		2	
	LPUART	1		1	
	USB/(VDD_USB)	1/(1)		1/(1)	
GPIOs		37	51[2]	37	51[2]
Clocks: HSE/LSE/HSI/MSI/LSI		1/1/1/1/1		1/1/1/1/1	
12-bit synchronized ADC Number of channels		1 10	1 16[2]	1 10	1 16[2]
12-bit DAC Number of channels		1 1		1 1	
LCD COM x SEG		1 4x18	1 4x32 or 8x28[2]	1 4x18	1 4x32 or 8x28[2]
Comparators		2		2	
Capacitive sensing channels		17	24[2]	17	24[2]
Max. CPU frequency		32 MHz			
Operating voltage		1.8 V to 3.6 V (down to 1.65 V at power-down) with BOR option 1.65 V to 3.6 V without BOR option			
Operating temperatures		Ambient temperature: –40 to +125 °C Junction temperature: –40 to +130 °C			
Packages		LQFP48	LQFP64, TFBGA64	LQFP48	LQFP64, TFBGA64

1. 2 SPI interfaces are USARTs operating in SPI master mode.
2. TFBGA64 has one GPIO, one LCD COM x SEG, one ADC input and one capacitive sensing channel less than LQFP64.

3.3 ARM® Cortex®-M0+ core with MPU

The Cortex-M0+ processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- a simple architecture that is easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family
- platform security robustness, with integrated Memory Protection Unit (MPU).

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to its embedded ARM core, the STM32L053x6/8 are compatible with all ARM tools and software.

Nested vectored interrupt controller (NVIC)

The ultra-low-power STM32L053x6/8 embed a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels and 4 priority levels.

The Cortex-M0+ processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- includes a Non-Maskable Interrupt (NMI)
- provides zero jitter interrupt option
- provides four interrupt priority levels

The tight integration of the processor core and NVIC provides fast execution of Interrupt Service Routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function that enables the entire device to enter rapidly stop or standby mode.

This hardware block provides flexible interrupt management features with minimal interrupt latency.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all scanned channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) can be internally connected to the ADC start triggers, to allow the application to synchronize A/D conversions and timers.

3.13 Temperature sensor

The temperature sensor (T_{SENSE}) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 6. Temperature sensor calibration values

Calibration value name	Description	Memory address
TSENSE_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3 V	0x1FF8 007A - 0x1FF8 007B
TSENSE_CAL2	TS ADC raw data acquired at temperature of 130 °C V_{DDA}= 3 V	0x1FF8 007E - 0x1FF8 007F

3.13.1 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and Comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. It enables accurate monitoring of the V_{DD} value (when no external voltage, V_{REF+}, is available for ADC). The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 7. Internal voltage reference measured values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at temperature of 25 °C V_{DDA} = 3 V	0x1FF8 0078 - 0x1FF8 0079

TIM21 and TIM22

TIM21 and TIM22 are based on a 16-bit auto-reload up/down counter. They include a 16-bit prescaler. They have two independent channels for input capture/output compare, PWM or one-pulse mode output. They can work together and be synchronized with the TIM2, full-featured general-purpose timers.

They can also be used as simple time bases and be clocked by the LSE clock source (32.768 kHz) to provide time bases independent from the main CPU clock.

3.18.2 Low-power Timer (LPTIM)

The low-power timer has an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / one shot mode
- Selectable software / hardware input trigger
- Selectable clock source
  - Internal clock source: LSE, LSI, HSI or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

3.18.3 Basic timer (TIM6)

This timer can be used as a generic 16-bit timebase. It is mainly used for DAC trigger generation.

3.18.4 SysTick timer

This timer is dedicated to the OS, but could also be used as a standard downcounter. It is based on a 24-bit downcounter with autoreload capability and a programmable clock source. It features a maskable system interrupt generation when the counter reaches ‘0’.

3.18.5 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 37 kHz internal RC and, as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

Table 11. STM32L053x6/8 I²C implementation (continued)

I2C features(1)	I2C1	I2C2
SMBus	X	-
Wakeup from STOP	X	-

1. X = supported.
2. See *Table 15: STM32L053x6/8 pin definitions on page 40* for the list of I/Os that feature Fast Mode Plus capability

3.19.2 Universal synchronous/asynchronous receiver transmitter (USART)

The two USART interfaces (USART1, USART2) are able to communicate at speeds of up to 4 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 driver enable (DE) signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. They also support SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode using baudrates up to 42 Kbaud.

All USART interfaces can be served by the DMA controller.

Table 12 for the supported modes and features of USART interfaces.

Table 12. USART implementation

USART modes/features(1)	USART1 and USART2
Hardware flow control for modem	X
Continuous communication using DMA	X
Multiprocessor communication	X
Synchronous mode(2)	X
Smartcard mode	X
Single-wire half-duplex communication	X
IrDA SIR ENDEC block	X
LIN mode	X
Dual clock domain and wakeup from Stop mode	X
Receiver timeout interrupt	X
Modbus communication	X
Auto baud rate detection (4 modes)	X
Driver Enable	X

1. X = supported.
2. This mode allows using the USART as an SPI master.

3.19.3 Low-power universal asynchronous receiver transmitter (LPUART)

The devices embed one Low-power UART. The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire

communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART has a clock domain independent from the CPU clock. It can wake up the system from Stop mode using baudrates up to 46 Kbaud. The Wakeup events from Stop mode are programmable and can be:

- Start bit detection
- Or any received data frame
- Or a specific programmed data frame

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

3.19.4 Serial peripheral interface (SPI)/Inter-integrated sound (I2S)

Up to two SPIs are able to communicate at up to 16 Mbits/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The USARTs with synchronous capability can also be used as SPI master.

One standard I2S interfaces (multiplexed with SPI2) is available. It can operate in master or slave mode, and can be configured to operate with a 16-/32-bit resolution as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When the I2S interfaces is configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

The SPIs can be served by the DMA controller.

Refer to *Table 13* for the differences between SPI1 and SPI2.

Table 13. SPI/I2S implementation

SPI features[1]	SPI1	SPI2
Hardware CRC calculation	X	X
I2S mode	-	X
TI mode	X	X

1. X = supported.

Table 15. STM32L053x6/8 pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP48	LQFP64	TFBGA64						
8	12	F1	VSSA	S	-	-	-	-
-	-	G1	VREF+	S	-	-	-	-
9	13	H1	VDDA	S	-	-	-	-
10	14	G2	PA0	I/O	TC	-	TIM2_CH1, TSC_G1_IO1, USART2_CTS, TIM2_ETR, COMP1_OUT	COMP1_INM6, ADC_IN0, RTC_TAMP2/WKUP1
11	15	H2	PA1	I/O	FT	-	EVENTOUT, LCD_SEG0, TIM2_CH2, TSC_G1_IO2, USART2_RTS_DE, TIM21_ETR	COMP1_INP, ADC_IN1
12	16	F3	PA2	I/O	FT	-	TIM21_CH1, LCD_SEG1, TIM2_CH3, TSC_G1_IO3, USART2_TX, COMP2_OUT	COMP2_INM6, ADC_IN2
13	17	G3	PA3	I/O	FT	-	TIM21_CH2, LCD_SEG2, TIM2_CH4, TSC_G1_IO4, USART2_RX	COMP2_INP, ADC_IN3
-	18	C2	VSS	S		-	-	-
-	19	D2	VDD	S		-	-	-
14	20	H3	PA4	I/O	TC	(1)	SPI1_NSS, TSC_G2_IO1, USART2_CK, TIM22_ETR	COMP1_INM4, COMP2_INM4, ADC_IN4, DAC_OUT
15	21	F4	PA5	I/O	TC	-	SPI1_SCK, TIM2_ETR, TSC_G2_IO2, TIM2_CH1	COMP1_INM5, COMP2_INM5, ADC_IN5
16	22	G4	PA6	I/O	FT	-	SPI1_MISO, LCD_SEG3, TSC_G2_IO3, LPUART1_CTS, TIM22_CH1, EVENTOUT, COMP1_OUT	ADC_IN6
17	23	H4	PA7	I/O	FT	-	SPI1_MOSI, LCD_SEG4, TSC_G2_IO4, TIM22_CH2, EVENTOUT, COMP2_OUT	ADC_IN7
-	24	H5	PC4	I/O	FT	-	EVENTOUT, LCD_SEG22, LPUART1_TX	ADC_IN14

5 Memory mapping

Figure 6. Memory map

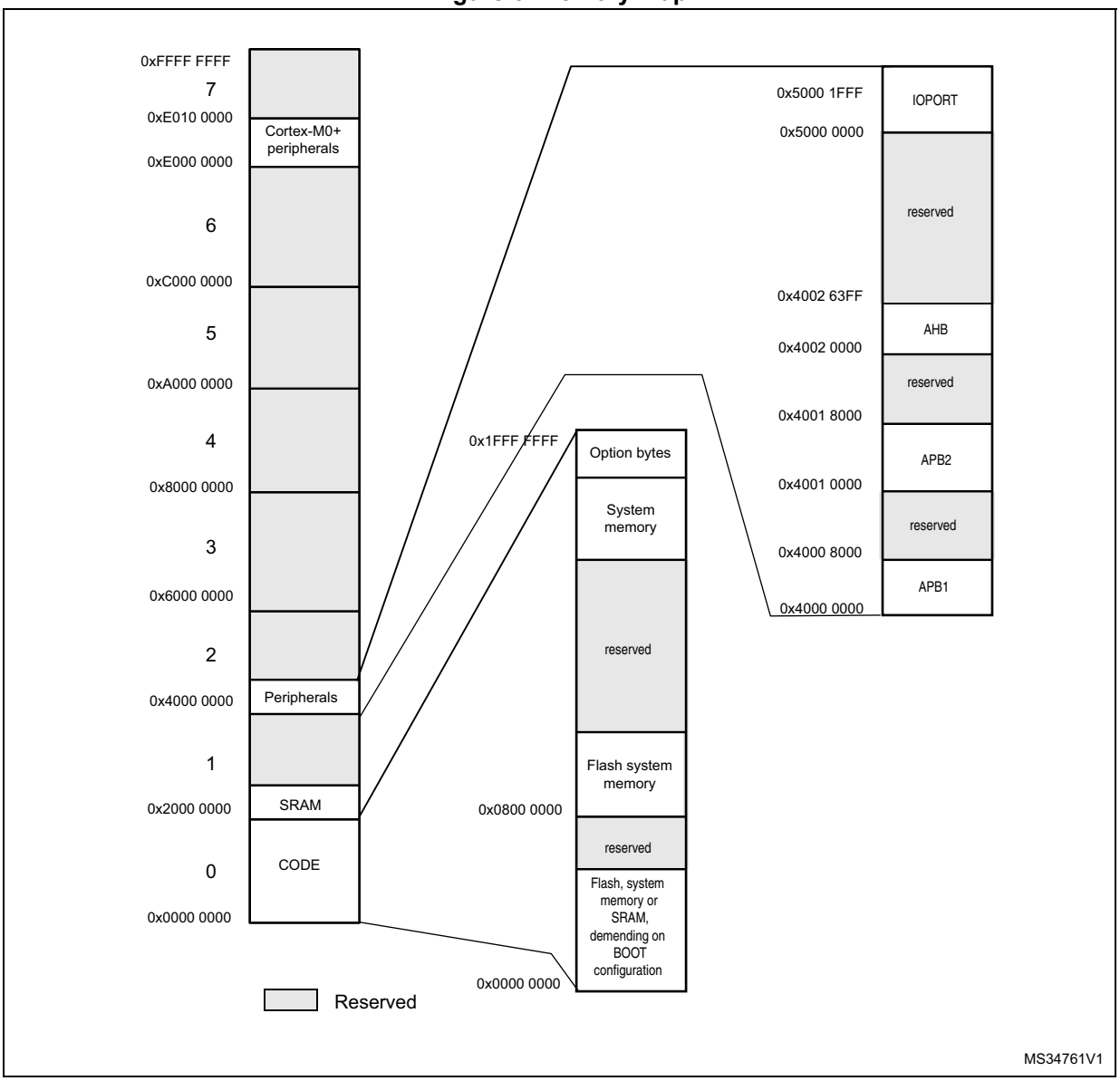


Table 28. Current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V VOS[1:0]=11	1 MHz	165	230	µA
				2 MHz	290	360	
				4 MHz	555	630	
			Range 2, V_{CORE}=1.5 V, VOS[1:0]=10,	4 MHz	0.665	0.74	mA
				8 MHz	1.3	1.4	
				16 MHz	2.6	2.8	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	1.55	1.7	
				16 MHz	3.1	3.4	
				32 MHz	6.3	6.8	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	36.5	110	µA
				524 kHz	99.5	190	
				4.2 MHz	620	700	
		HSI clock	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10,	16 MHz	2.6	2.9	mA
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	6.25	7	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 29. Current consumption in Run mode vs code type, code with data processing running from Flash

Symbol	Parameter	Conditions			f_{HCLK}	Typ	Unit
I_{DD} (Run from Flash)	Supply current in Run mode, code executed from Flash	$f_{HSE} = f_{HCLK}$ up to 16 MHz included, $f_{HSE} = f_{HCLK}/2$ above 16 MHz (PLL ON)(1)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	555	µA
				CoreMark		585	
				Fibonacci		440	
				while(1)		355	
				while(1), prefetch OFF		353	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	Dhrystone	32 MHz	6.3	mA
				CoreMark		6.3	
				Fibonacci		6.55	
				while(1)		5.4	
				while(1), prefetch OFF		5.2	

1. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 30. Current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	1 MHz	135	170	µA
				2 MHz	240	270	
				4 MHz	450	480	
			Range 2, V_{CORE}=1.5 ,V, VOS[1:0]=10	4 MHz	0.52	0.6	mA
				8 MHz	1	1.2	
				16 MHz	2	2.3	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	1.25	1.4	
				16 MHz	2.45	2.8	
				32 MHz	5.1	5.4	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	34.5	75	µA
				524 kHz	83	120	
				4.2 MHz	485	540	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	16 MHz	2.1	2.3	mA
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	5.1	5.6	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 31. Current consumption in Run mode vs code type, code with data processing running from RAM(1)

Symbol	Parameter	Conditions			f_{HCLK}	Typ	Unit
I_{DD} (Run from RAM)	Supply current in Run mode, code executed from RAM, Flash switched off	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	Dhrystone	4 MHz	450	µA
				CoreMark		575	
				Fibonacci		370	
				while(1)		340	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	Dhrystone	32 MHz	5.1	mA
				CoreMark		6.25	
				Fibonacci		4.4	
				while(1)		4.7	

1. Guaranteed by characterization results, unless otherwise specified.
2. Oscillator bypassed (HSEBYP = 1 in RCC_CR register).

Table 32. Current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK}	Typ	Max(1)	Unit
I_{DD} (Sleep)	Supply current in Sleep mode, Flash OFF	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	1 MHz	43.5	90	µA
				2 MHz	72	120	
				4 MHz	130	180	
			Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	4 MHz	160	210	
				8 MHz	305	370	
				16 MHz	590	710	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	370	430	
				16 MHz	715	860	
				32 MHz	1650	1900	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	18	65	
				524 kHz	31.5	75	
				4.2 MHz	140	210	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	16 MHz	665	830	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	1750	2100	
	Supply current in Sleep mode, Flash ON	f_{HSE} = f_{HCLK} up to 16 MHz included, f_{HSE} = f_{HCLK}/2 above 16 MHz (PLL ON)(2)	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	1 MHz	57.5	130	
				2 MHz	84	170	
				4 MHz	150	280	
			Range 2, CORE=1.5 V, VOS[1:0]=10	4 MHz	170	310	
				8 MHz	315	420	
				16 MHz	605	770	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	8 MHz	380	460	
				16 MHz	730	950	
				32 MHz	1650	2400	
		MSI clock	Range 3, V_{CORE}=1.2 V, VOS[1:0]=11	65 kHz	29.5	110	
				524 kHz	44.5	130	
				4.2 MHz	150	270	
		HSI16 clock source (16 MHz)	Range 2, V_{CORE}=1.5 V, VOS[1:0]=10	16 MHz	680	950	
			Range 1, V_{CORE}=1.8 V, VOS[1:0]=01	32 MHz	1750	2100	

1. Guaranteed by characterization results at 125 °C, unless otherwise specified.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in the following tables. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked OFF
  - with only one peripheral clocked on

Table 38. Peripheral current consumption in Run or Sleep mode(1)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
APB1	CRS	2.5	2	2	2	µA/MHz (f_{HCLK})
	DAC1	4	3.5	3	2.5	
	I2C1	11	9.5	7.5	9	
	I2C2	4	3.5	3	2.5	
	LCD1	4	3.5	3	2.5	
	LPTIM1	10	8.5	6.5	8	
	LPUART1	8	6.5	5.5	6	
	SPI2	9	4.5	3.5	4	
	USB	8.5	4.5	4	4.5	
	USART2	14.5	12	9.5	11	
	TIM2	10.5	8.5	7	9	
	TIM6	3.5	3	2.5	2	
	WWDG	3	2	2	2	
APB2	ADC1(2)	5.5	5	3.5	4	µA/MHz (f_{HCLK})
	SPI1	4	3	3	2.5	
	USART1	14.5	11.5	9.5	12	
	TIM21	7.5	6	5	5.5	
	TIM22	7	6	5	6	
	FIREWALL	1.5	1	1	0.5	
	DBGMCU	1.5	1	1	0.5	
	SYSCFG	2.5	2	2	1.5	

Table 38. Peripheral current consumption in Run or Sleep mode(1) (continued)

Peripheral		Typical consumption, V_{DD} = 3.0 V, T_A = 25 °C				Unit
		Range 1, V_{CORE}=1.8 V VOS[1:0] = 01	Range 2, V_{CORE}=1.5 V VOS[1:0] = 10	Range 3, V_{CORE}=1.2 V VOS[1:0] = 11	Low-power sleep and run	
Cortex-M0+ core I/O port	GPIOA	3.5	3	2.5	2.5	µA/MHz (f_{HCLK})
	GPIOB	3.5	2.5	2	2.5	
	GPIOC	8.5	6.5	5.5	7	
	GPIOD	1	0.5	0.5	0.5	
	GPIOH	1.5	1	1	0.5	
AHB	CRC	1.5	1	1	1	µA/MHz (f_{HCLK})
	FLASH	0(3)	0(3)	0(3)	0(3)	
	DMA1	10	8	6.5	8.5	
	RNG	5.5	1	0.5	0.5	
	TSC	3	2.5	2	3	
All enabled		283	225	222.5	212.5	µA/MHz (f_{HCLK})
PWR		2.5	2	2	1	µA/MHz (f_{HCLK})

1. Data based on differential I_{DD} measurement between all peripherals OFF an one peripheral with clock enabled, in the following conditions: f_{HCLK} = 32 MHz (range 1), f_{HCLK} = 16 MHz (range 2), f_{HCLK} = 4 MHz (range 3), f_{HCLK} = 64kHz (Low-power run/sleep), $f_{APB1} = f_{HCLK}$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral. The CPU is in Sleep mode in both cases. No I/O pins toggling. Not tested in production.
2. HSI oscillator is OFF for this measure.
3. Current consumption is negligible and close to 0 µA.

Table 48. MSI oscillator characteristics (continued)

Symbol	Parameter	Condition	Typ	Max	Unit
ACC_{MSI}	Frequency error after factory calibration	-	±0.5	-	%
$D_{TEMP(MSI)}$(1)	MSI oscillator frequency drift 0 °C ≤T_A ≤85 °C	-	±3	-	%
	MSI oscillator frequency drift V_{DD} = 3.3 V, − 40 °C ≤T_A ≤110 °C	MSI range 0	− 8.9	+7.0	
		MSI range 1	− 7.1	+5.0	
		MSI range 2	− 6.4	+4.0	
		MSI range 3	− 6.2	+3.0	
		MSI range 4	− 5.2	+3.0	
		MSI range 5	− 4.8	+2.0	
		MSI range 6	− 4.7	+2.0	
$D_{VOLT(MSI)}$(1)	MSI oscillator frequency drift 1.65 V ≤V_{DD} ≤3.6 V, T_A = 25 °C	-	-	2.5	%/V
$I_{DD(MSI)}$(2)	MSI oscillator power consumption	MSI range 0	0.75	-	µA
		MSI range 1	1	-	
		MSI range 2	1.5	-	
		MSI range 3	2.5	-	
		MSI range 4	4.5	-	
		MSI range 5	8	-	
		MSI range 6	15	-	
$t_{SU(MSI)}$	MSI oscillator startup time	MSI range 0	30	-	µs
		MSI range 1	20	-	
		MSI range 2	15	-	
		MSI range 3	10	-	
		MSI range 4	6	-	
		MSI range 5	5	-	
		MSI range 6, Voltage range 1 and 2	3.5	-	
		MSI range 6, Voltage range 3	5	-	

Table 62. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{ADC}(3)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(3)(5)	Calibration time	f_{ADC} = 16 MHz	5.2			µs
		-	83			$1/f_{ADC}$
$W_{LATENCY}$(6)	ADC_DR register write latency	ADC clock = HSI16	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr}(3)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2$ = 16 MHz	0.266			µs
		$f_{ADC} = f_{PCLK}/2$	8.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4$ = 8 MHz	0.516			µs
		$f_{ADC} = f_{PCLK}/4$	16.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI16}$ = 16 MHz	0.252	-	0.260	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI16}$	-	1	-	$1/f_{HSI16}$
t_S(3)	Sampling time	f_{ADC} = 16 MHz	0.093	-	10.03	µs
		-	1.5	-	160.5	$1/f_{ADC}$
t_{UP_LDO}(3)(5)	Internal LDO power-up time	-	-	-	10	µs
t_{STAB}(3)(5)	ADC stabilization time	-	14			$1/f_{ADC}$
t_{ConV}(3)	Total conversion time (including sampling time)	f_{ADC} = 16 MHz, 12-bit resolution	0.875	-	10.81	µs
		12-bit resolution	14 to 173 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. V_{DDA} minimum value can be decreased in specific temperature conditions. Refer to *Table 63: RAIN max for fADC = 16 MHz*.
2. A current consumption proportional to the APB clock frequency has to be added (see *Table 38: Peripheral current consumption in Run or Sleep mode*).
3. Guaranteed by design.
4. Standard channels have an extra protection resistance which depends on supply voltage. Refer to *Table 63: RAIN max for fADC = 16 MHz*.
5. This parameter only includes the ADC timing. It does not take into account register access latency.
6. This parameter specifies the latency to transfer the conversion result into the ADC_DR register. EOC bit is set to indicate the conversion is complete and has the same latency.

6.3.19 Timer characteristics

TIM timer characteristics

The parameters given in the *Table 70* are guaranteed by design.

Refer to *Section 6.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 70. TIMx characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	31.25	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 32 MHz	0	16	MHz
Res_{TIM}	Timer resolution	-		16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected (timer's prescaler disabled)	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	0.0312	2048	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 32 MHz	-	134.2	s

1. TIMx is used as a general term to refer to the TIM2, TIM6, TIM21, and TIM22 timers.

6.3.20 Communications interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm) : with a bit rate up to 100 kbit/s
- Fast-mode (Fm) : with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+) : with a bit rate up to 1 Mbit/s.

The I^2C timing requirements are guaranteed by design when the I^2C peripheral is properly configured (refer to the reference manual for details). The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDDIOx is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement (refer to *Section 6.3.13: I/O port characteristics* for the I2C I/Os characteristics).

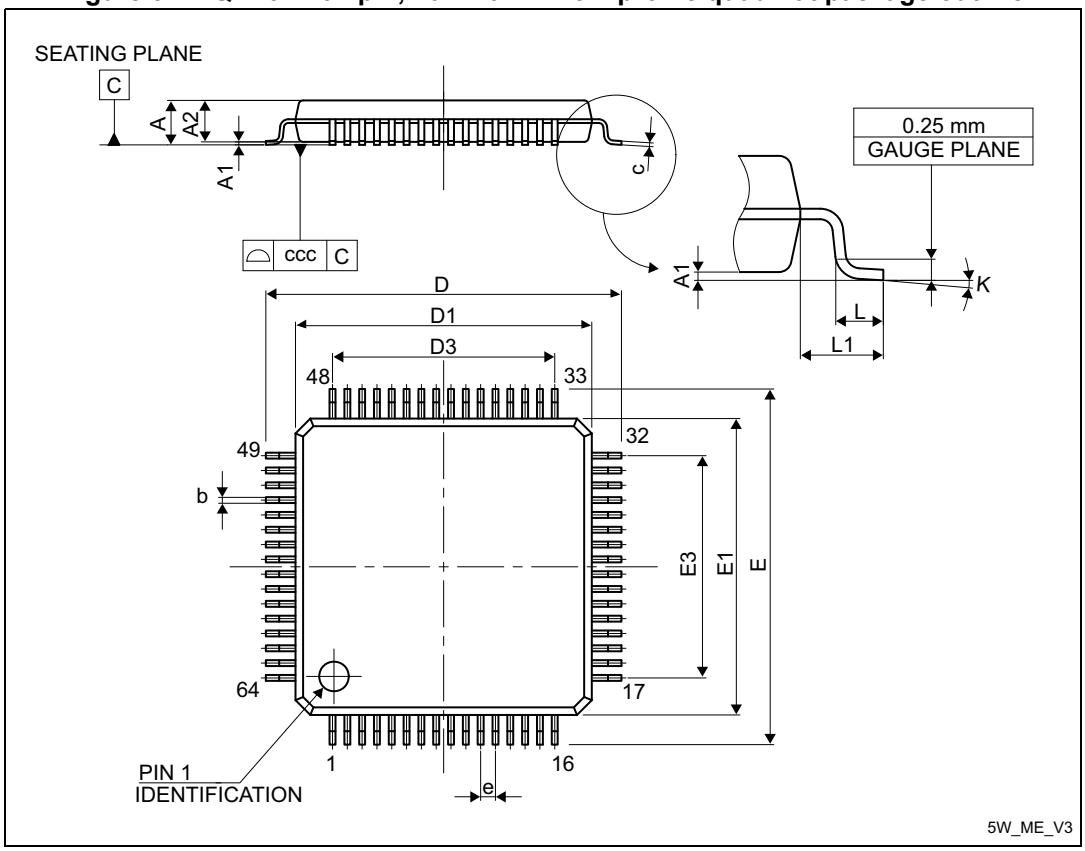
All I^2C SDA and SCL I/Os embed an analog filter (see *Table 71* for the analog filter characteristics).

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at www.st.com.* ECOPACK® is an ST trademark.

7.1 LQFP64 package information

Figure 37. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

7.4.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

Table 87. Document revision history (continued)

Date	Revision	Changes
25-Jun-2014	3	ADC now guaranteed down to 1.65 V. Cover page: updated core speed, added minimum supply voltage for ADC, DAC and comparators. Updated list of applications in *Section 1: Introduction*. Changed number of I2S interfaces to one in *Section 2: Description*. Updated RTC/TIM21 in *Table 5: STM32L0xx peripherals interconnect matrix*. Updated *Table 4: Functionalities depending on the working mode (from Run/active down to standby)*. Updated *Section 3.4.1: Power supply schemes*. Updated *Figure 4: STM32L053x6/8 TFBGA64 ballout - 5x 5 mm*. Updated V_{DDA} in *Table 24: General operating conditions*. Splitted Table *Current consumption in Run mode, code with data processing running from Flash* into *Table 28* and *Table 29* and content updated. Splitted Table *Current consumption in Run mode, code with data processing running from RAM* into *Table 30* and *Table 31* and content updated. Updated *Table 32: Current consumption in Sleep mode*, *Table 33: Current consumption in Low-power run mode*, *Table 34: Current consumption in Low-power sleep mode*, *Table 35: Typical and maximum current consumptions in Stop mode*, *Table 36: Typical and maximum current consumptions in Standby mode*, and added *Table 37: Average current consumption during Wakeup*. Updated *Table 38: Peripheral current consumption in Run or Sleep mode* and added *Table 39: Peripheral current consumption in Stop and Standby mode*. Updated *Table 46: HSI48 oscillator characteristics*. Removed note 1 below *Figure 19: HSE oscillator circuit diagram*. Updated t_{LOCK} in *Table 49: PLL characteristics*. Updated *Table 51: Flash memory and data EEPROM characteristics* and *Table 52: Flash memory and data EEPROM endurance and retention*. Updated *Table 60: I/O AC characteristics*. Updated *Table 62: ADC characteristics*. Updated *Figure 46: Thermal resistance* and added note 1.